AN3410
Application note

A 93% efficient LED driver solution for the US market

Introduction

This application note describes an LED driver that meets present requirements for the US market. It utilizes ST's L6564 power factor controller in an unconventional circuit to regulate the input power to a step-down switching regulator. The circuit also compensates for variations in LED voltage drop, to maintain the average output current in a tight band over a wide range of line voltage and LED characteristics. While the input current waveform is not perfectly sinusoidal, power factor and harmonic content are well within the requirements for the US commercial market. The form factor was designed to fit into the PAR38 envelope - the driver and LEDs can be used to replace 65 W incandescent floodlamps.

- Specifications:
  - Output current 350 mA +/-3% over 90 V-138 V line range
  - Load: 18 series-connected 1 W LEDs
  - Efficiency > 93%
  - Power factor > 0.97
  - Dimmer safe
  - Non-isolated
- ST devices:
  - L6564 transition-mode PFC controller
  - STD5NM50 FET
  - STTH1R04A fast recovery diode
  - TS321AILT low power op amp

Figure 1. Physical envelope

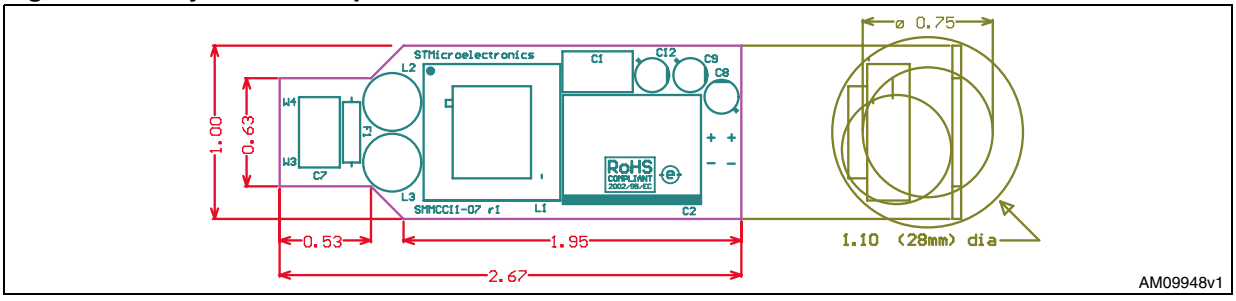
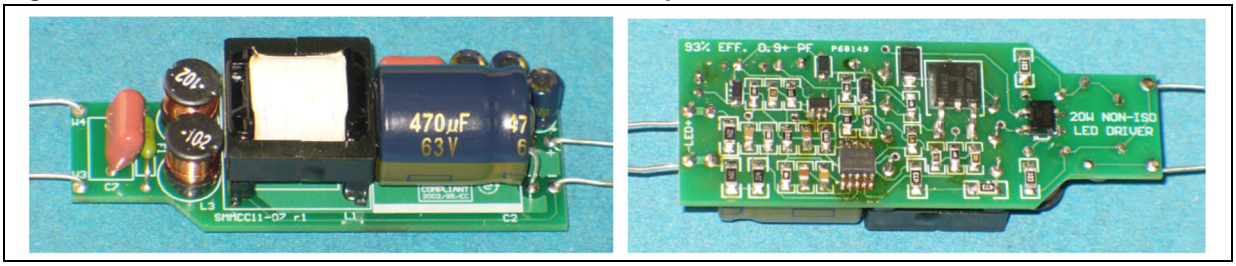


Figure 2. STEVAL-ILL041V1 demonstration board picture

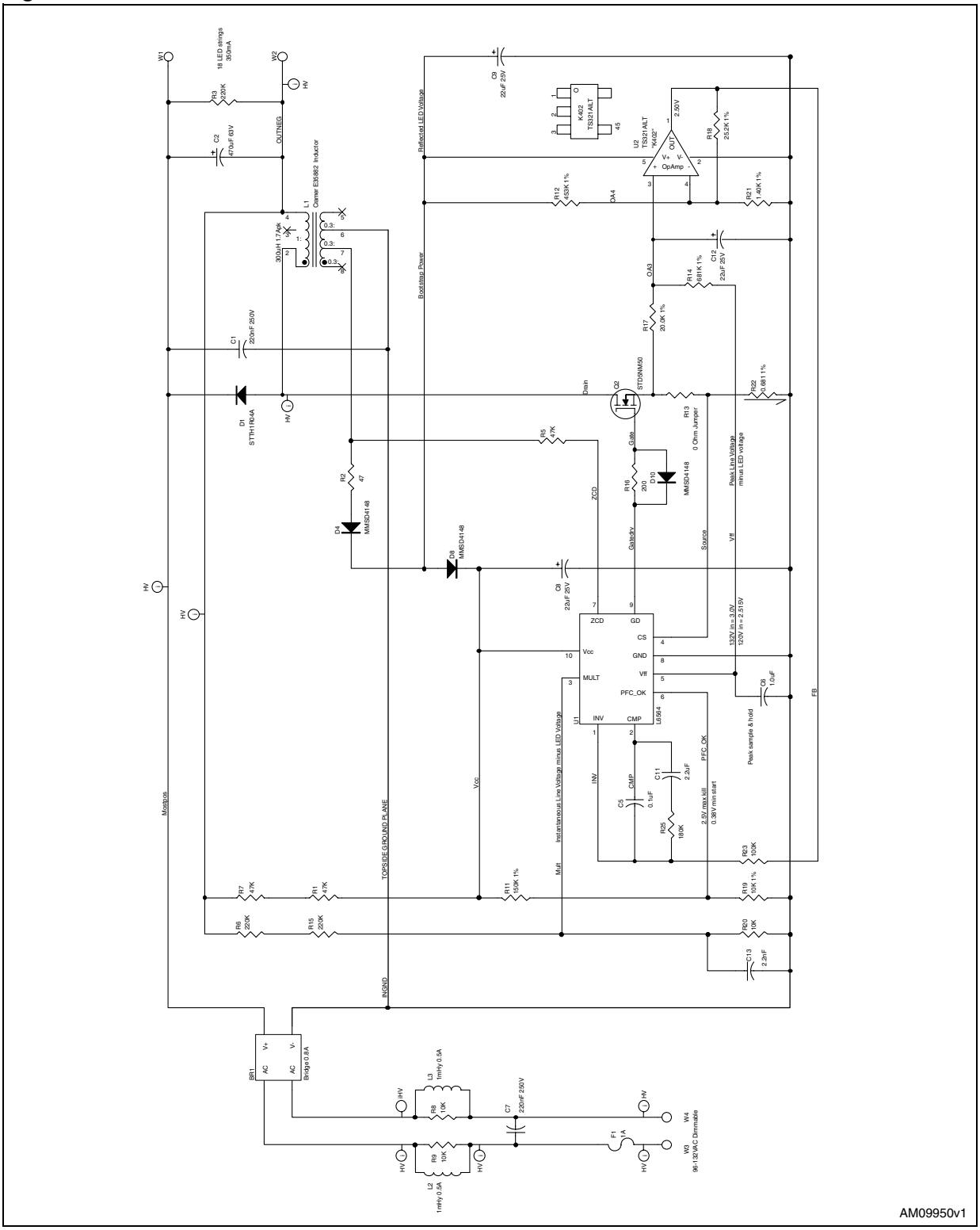


Contents

List of figures

1 Schematic diagram

Figure 3. Circuit schematic



2 Circuit description

2.1 Power components

C7, L2, and L3 provide filtering for conducted EMI. Bridge rectifier BR1 feeds the step-down (buck) switching regulator. The regulator appears inverted – the flywheel diode, D1, is connected to the positive rail instead of the negative. Q2 pulls the inductor input negative, rather than positive. Inductor L1 filters the PWM voltage into a triangle wave of current. C2 removes the high-frequency ripple and attenuates the 120 Hz component in the LED load.

Note that the buck regulator is not capable of supplying power to the load if the load voltage is greater than the input voltage. There are “flat spots” in the input current waveform around the input voltage zero crossings. Power factor remains excellent, even with this distortion.

2.2 Power factor controller operation

Startup

The circuit starts up with a trickle of current into C8 through R7. It takes about ¼ second to charge C8 to U1’s startup voltage. The trickle current adds to LED current, slightly improving circuit efficiency.

The startup timer in U1 starts the switching cycle by turning on Q2. Current in Q2 and L1 increases from zero to about 1400 mA at the peaks of the input sinewave. This current appears on R22 which drops about 1 volt max.

L1’s current continues to flow after Q2 turns off, instead flowing in D1. The current ramps toward zero, at which time D1 turns off. The FET drain voltage then begins to fall.

Quasi-resonant FET turn-on

L1 and stray capacitance then ring the voltage at D1’s anode down to about twice the LED voltage below the positive rail. When the ringing voltage turns up, U1 senses the end of L1’s discharge and turns on Q2 very close to the minimum ringing voltage, starting the next cycle. Current in L1’s upper winding therefore ramps between zero and twice the load current.

When Q2 turns on, D1 has already turned off, so Q2 never sees D1’s reverse recovery current.

Bootstrap power

Housekeeping power is supplied by the auxiliary (lower) winding on L1. The winding is connected through D4 so that the transformed LED voltage (positive) is applied to C9, which powers U2, and C8 which powers U1. R2 and C9 form a filter to remove ringing spikes due to leakage inductance.

The auxiliary (lower) winding on L1 has a turns ratio that puts about 15 V on C9 with the AC line applied. The voltage on C9 is proportional to the LED voltage. This will limit the number of series LEDs in the load to a relatively narrow range, set by the acceptable Vcc for U1 and U2.

The auxiliary winding also provides U1 with timing for the zero-current sensing function, through R5.

2.3 Controlling the LED average current

The control circuit works by controlling average input power. For this explanation, it is assumed that the power converter efficiency is constant over the range of line voltage and LED voltage. Therefore, average output power is also controlled.

Linear approximation of input power

Over a narrow range of line voltage, the sum of scaled average line voltage and scaled average line current closely approximates a constant power curve. If the sum is held constant, the input power can be held approximately constant by a feedback circuit.

Figure 4. Constant-power V-I curve and linear approximation

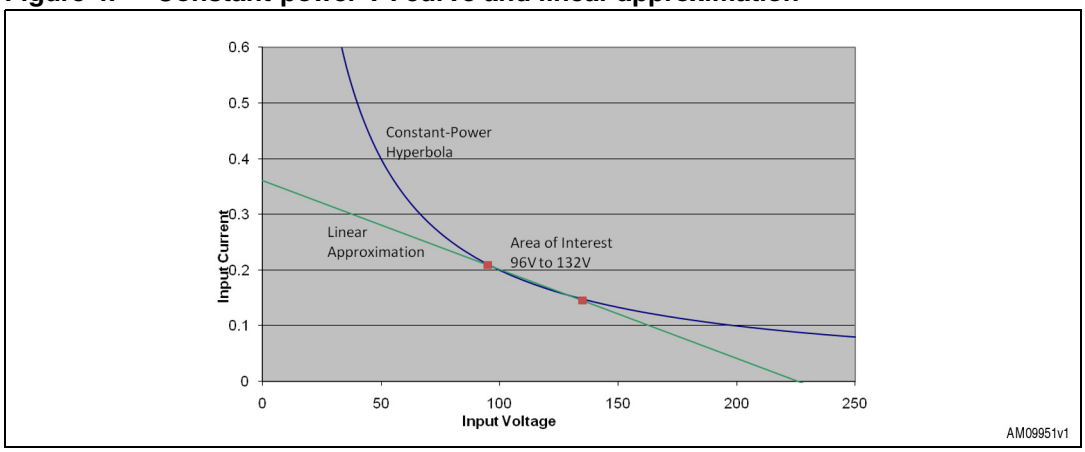
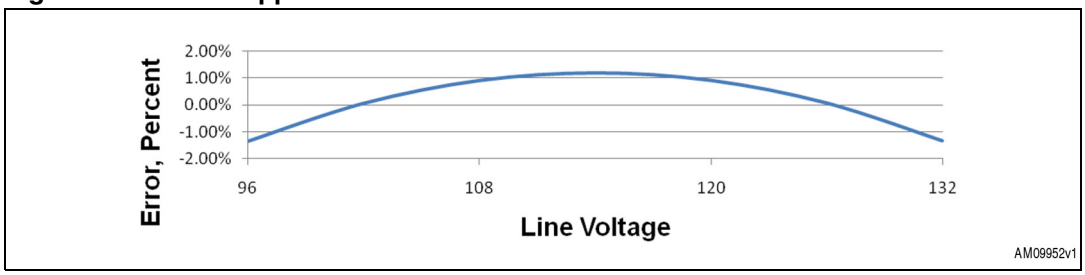


Figure 5 below shows the approximation's error over a typical line voltage range.

Figure 5. Linear approximation error



This will be explained in more detail later.

Obtaining the line voltage reference

In previous work it was found that the reference waveform for the inverted step-down switching regulator should be taken from the negative output terminal for best power factor.

This point gives a line current waveform that goes to zero around the zero crossings and rises (and falls) more rapidly than the line voltage sine wave. (The converter input current goes to zero when line voltage falls below the DC output voltage.) The resulting line current can be seen in the scope photos. It's ugly, but the power factor is excellent and THD is acceptable.

Average line voltage (minus the LED voltage) is derived from the peak voltage at the bottom of the LED string by R6, R15, and R20. U1 contains a precision peak detector, which places

the peak from this divider on C6. (Normally this voltage is used internally by the L6564 to adjust its multiplier gain to accommodate a wide line voltage range.)

Obtaining the line current (the controlled variable)

The vast majority of input current flows through R22, the sense resistor for the PFC-flyback converter. The average of the current in R22 and the average of the line voltage (minus the LED voltage) will be used in the power calculation.

Calculating the average power

Scaling and addition of voltage and current is done by R17 and R14. The AC noise present at their junction is removed by C12 - the DC voltage on C12 now represents the input power as calculated by the linear approximation. This voltage will be regulated by the slow PFC feedback loop.

Op amp U2 is wired as a non-inverting amplifier. The feedback loop requires only one inversion, supplied by the op amp in U1.

U2 performs three different functions:

- Derives a reference voltage from U1.
- Provides gain for the relatively low voltage on C12.
- Provides a point in the circuit to compensate for different LED voltages.

A DC reference voltage is derived from U1's inverting input. This point will always be at 2.5 V if the control loop is in steady-state, because there is no DC current path to any other voltage source. The reference voltage is delivered to U2's inverting input by divider R18-R21. The voltage divider R18-R21 also sets the DC gain for U2.

If this circuit acted alone, the input power would be (approximately) regulated to a fixed value, and the LED current would inversely track the LED voltage.

2.4 Setting the "DC" operating point

The control loop is to set the average current through R22 to deliver slightly more than the desired LED current when both the line voltage and LED voltage are at design center.

Deviations of line and LED voltage from this point will then cause smaller deviations of LED current.

The input current required is I_{LED} x V_{LED} / (V_{LINE} x efficiency). The straight-line approximation (of the constant-power curve) should give equal voltage from the average line voltage and the average input current.

The value of R22 is determined from the usual calculations (see ST's excellent application note AN1059, reference 1).

The average input current (in R22) can now be calculated from the design center line voltage, output power, and efficiency. At design center line voltage, LED current, and LED voltage, the average voltage appearing across R17 due to current from R14 must match the average voltage on R22.

Stirring in the LED voltage

Compensation for LED voltage changes follows two paths in this design:

- by direct subtraction of the LED voltage from the line voltage (path 1)
- from the transformed LED voltage on C9 through R12 (path 2).

Path 1

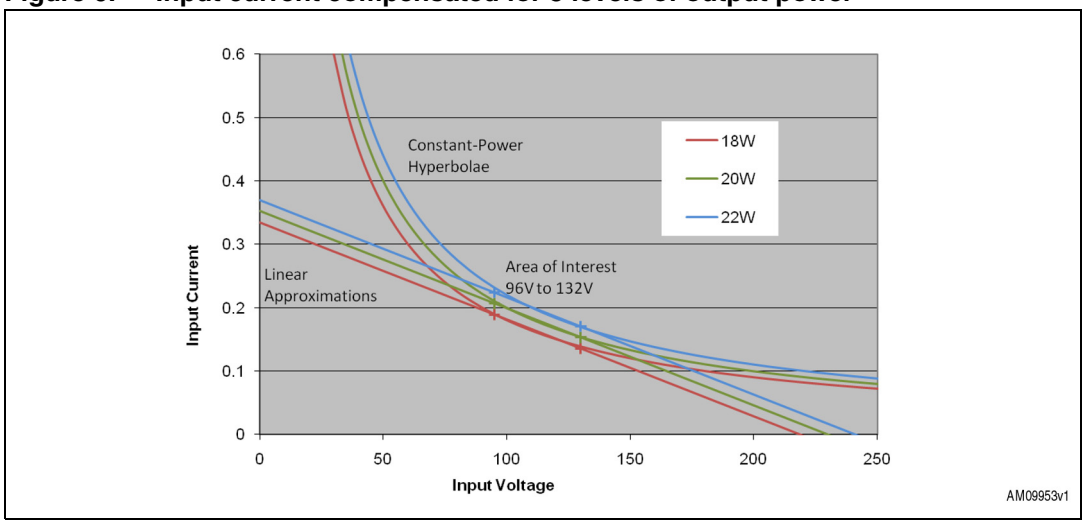
An increase of LED voltage will reduce the voltage at U1 pin 5. This reduces current through R14. The feedback loop will then call for more line current to compensate.

Path 2

The voltage compensation obtained from the 18-LED load is not quite sufficient to flatten the LED current over the expected range of LED voltage, so the second path through R12 is also implemented. The LED voltage (multiplied by L1's turns ratio) is available on D4's cathode, filtered by C9. Current proportional to this voltage is delivered to U2's inverting input by R12. The reference for the operating point is thus compensated by the LED voltage.

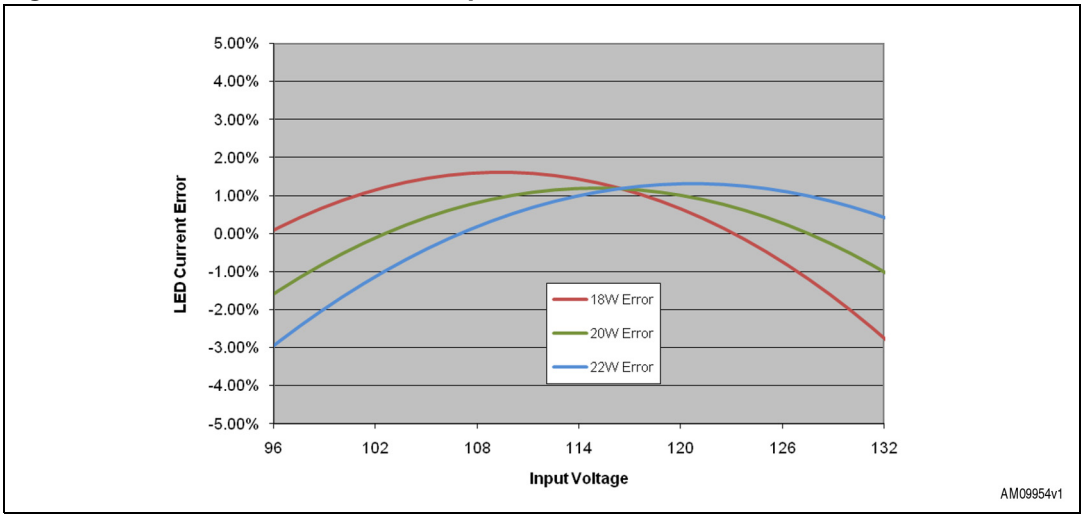
The figures below show the results of compensating the input current setting for load voltage.

Figure 6. Input current compensated for 3 levels of output power



In *Figure 6* the reference has been compensated by adding a current proportional to the LED voltage. Three levels of input power are shown, corresponding to LED voltages of 10% below nominal, nominal, and 10% above nominal. *Figure 7* below shows the error between the approximations and the ideal values.

Figure 7. Error for 3 levels of load power



Note that the curves coincide at the nominal line voltage, where LED voltage compensation is perfect. Also, for nominal LED voltage, line voltage compensation is at its best, +/-1.5%.

Over the entire range of line voltage (120 V +10%,-20%) and LED (+/-10%) voltage, the variation of LED current is less than 4.5% (+1.5%, -3%).

2.5 Designing the “DC” control loop

Finding values for the resistors in this loop is surprisingly easy.

(For this procedure, diode drops will be ignored for simplicity.)

Let us assume that the average LED current is to be 350 mA, and a string of 18 LEDs drops about 54.6 V. Output power is 18 watts. Input power will be assumed to be 20 W (90% efficiency, actually conservative).

Assume the input current and voltage waveforms are sine waves (power factor is high, so this is a good assumption).

The converter output current waveform is a triangle wave with an (assumed) rectified sinusoidal upper envelope, and a lower envelope at zero. The short-term average of the triangle wave is half its height. The rectified sinusoid has an average current of 63% of its peak current.

At the peak of the input voltage, the peak current delivered to the LEDs is therefore.

Equation 1

$$I_{led}PK = \frac{2 * I_{led}AVG}{0.63} = \frac{2 * 0.35A}{0.63} = 1.02A$$

We will allow some margin for the relatively slow fall time of the drain voltage due to the zero current detection, so the peak current will be slightly higher. We will design the inductor for 1.4 A peak current in the main winding. The L6564 control chip has an upper voltage limit on its current sense input of 1.08 V for linear operation. So the maximum value of R22 is

Equation 2

$$R22_{max} = \frac{1.08V}{1.4A} = 0.77\ Ohms$$

Select 0.681 Ω.

Average input current will be slightly lower than expected - the input voltage and current are assumed sinusoidal, and the average current will be 0.9 times the input rms current. So at the design center of 115 V, average input current is

Equation 3

$$I_{in}AVG = \frac{0.9 * P_{in}}{V_{in}RMS} = 0.156A$$

The bulk of this current flows in R22, so the average voltage on R22 is

Equation 4

$$V_{R22}AVG = 0.156\text{A} * 0.681\ \text{Ohms} = 0.106\text{V}$$

R17 serves two functions - it is part of the linear approximation calculation, and part of a low-pass filter that cleans up both the triangular FET drain current pulses and the 120 Hz envelope. A value of 20 kΩ has been selected somewhat arbitrarily.

At our nominal operating point, the average voltage developed on R17 due to line voltage must be equal to the average voltage at its lower end from R22. The current required is

Equation 5

$$\frac{0.106V}{20K} = 5.3\mu\text{A}$$

The L6564 Vff terminal connects internally to a precision peak detector. Its normal function, which will not be used, is to reduce the loop gain at high line voltages. However, the peak detector function gives us a buffered peak line voltage (minus LED voltage) reference.

If LED voltage is zero, the entire line voltage appears on divider R6-R15-R20. For nominal line, the peak voltage at U1's MULT input is

Equation 6

$$V_{pk}MULT = 115V * 1.414 * \frac{10K}{450K} = 3.61\ \text{V}$$

To provide the 5.3 µA needed by the linear compensator,

Equation 7

$$R14 = \frac{3.61V - 2 * 0.106V}{5.3\mu\text{A}} = 641K$$

We will use the nearest standard value, 649 kΩ.

We will now examine the LED voltage compensation, to determine the values of R12, R18, and R21.

If there is no LED voltage, there will be no reflected voltage from L1's auxiliary winding. (We will assume the circuit runs anyway) Therefore, R12 contributes no current. Since there is no output voltage there will be no output power, and since efficiency is assumed constant, no input power. Therefore, there will be no voltage on R22, and the only voltage on C12 will be the divided line peak voltage from C6. Divider R17-R14 will deliver 0.106 V to the non-inverting input of U2.

If the loop is balanced, the op amp output will be at exactly 2.5 V (so that the COMP terminal on U1 does not move). The op amp inputs will be at exactly the same voltage, 0.106 V.

To find the value of R21, we first arbitrarily select 25.2 kΩ for R18. R21's value is then

Equation 8

$$R21 = \frac{0.106V}{2.50V - 0.106V} * R18 = 1.115\ \text{k}\Omega$$

Use 1.10 kΩ.

Now we examine the operating points when the LEDs are at nominal voltage. The peak voltage at U1's Vff terminal will now be

Equation 9

$$V_{Vff} = (1.414 * 115V - 54V) * \frac{10K}{450K} = 2.41V$$

So at nominal input power (20 W) the average voltage applied to C12 and U2's non-inverting input is the voltage from R22 plus the divided voltage from R14 and R17:

Equation 10

$$V_{U2+} = 0.106V + (2.41V - 0.106V) * \frac{20K}{649K + 20K} = 0.175V.$$

R12 must be selected to deliver this voltage at U2's inverting input.

The equivalent voltage and resistance presented by U2's 2.50 V output and the R18-R21 divider is:

Equation 11

$$V_{th} = 2.5V * \frac{1.10K}{1.10K + 25.2K} = 0.104V$$

$$R_{th} = \frac{1.1K * 25.2K}{1.1K + 25.2K} = 1.054K$$

R12 must bring the voltage on U2's inverting input up to 0.175 V from 1.06 V when the reflected LED voltage is at its nominal value.

Neglecting diode and R2 drops, the voltage at the top of R12 is the LED voltage times the turns ratio of L1's auxiliary winding:

Equation 12

$$V_{reflected} = \frac{N_{aux}}{N_{led}} * V_{led} = 0.3 * 54.6V = 16.2V$$

R12 must provide enough current to bring the voltage up to 0.175V. The added voltage due to R12 must be 0.175 V - 0.104 V = 0.071 V.

R12's value is then

Equation 13

$$R12 = R_{th} * \frac{16.2V - 0.175V}{0.071V} = 238K.$$

We will use 240 kΩ.

Some trimming may be required to hit the 350 mA * 1.012 target to center the operating point in the error band.

In summary, the parts selected are:

- R22 0.681 Ω
- R17 20 kΩ
- R14 649 kΩ
- R18 25.2 kΩ
- R21 1.10 kΩ
- R12 240 kΩ

3 Control loop dynamics

The control loop is intentionally very slow, much slower than a normal PFC loop. The reason is that the eye perceives abrupt changes of light intensity as flashes.

The eye has an intensity control loop of its own, which adjusts the light falling on the retina by controlling the iris opening. The loop bandwidth is about ¼ Hz. If light level changes occur slower than this, they are not perceived as flashes. the iris can keep up with the change.

The LED driver control loop is set up as a continuous -20 dB/decade / 90 degrees lag system, which gives a response to perturbations having no overshoot.

The current control loop breakpoints are:

- A pole at zero frequency
- A pole at 0.35 Hz (R17-C12)
- A zero at 0.35 Hz (R25-C11)

A third pole at high frequency due to noise filter C5 (gain is well below unity at this corner - the pole is inconsequential).

The pole due to R17 and C12 is essential to the system – switching ripple and the 120 Hz envelope must be filtered. The R25-C11 zero cancels this pole, keeping the gain slope at -20 dB/decade.

There are two problems that affect the control loop:

- There is a second path in the system that gives positive feedback, the compensation for LED voltage. Fortunately, the voltage loop gain is low due to the low dynamic resistance of the LEDs, typically 1 Ohm per LED. Changes in the input power can only cause very small changes in the LED voltage.
- The R18-R21 voltage divider, necessary for the DC control scheme, gives considerable unnecessary loop gain.

Note that R23 provides a very handy single-point gain adjustment. Increasing its value reduces the gain of the entire loop. This is a good point for stability testing - it should be possible to reduce the value of R23 by a factor of 2 to 4 (6-12dB) before sustained (slow!) oscillation results.

Control loop transient response can be observed at startup (see *Figure 16*). The LED current rises rapidly (a nice transient), and the control loop takes over very smoothly. The LED current should not overshoot, and it should settle to its final level within 2 or 3 seconds.

Either excessive gain (overshoot) or unmatched time constants for the breakpoint networks R17-C12 and R25-C11 (lumps or dips in the startup waveforms) can cause strange behavior during startup.

Excessive gain can result in ringing or sustained oscillation - both are quite annoying.

Mismatched breakpoints can result in a dip or rise of output current about 1.5 seconds after the unit starts. The result is not too annoying, but it should be corrected - customers demand smooth operation.

4 Performance with LED loads

The unit was designed to source 350 mA into a string of 18 1 W LEDs. The project goal was to obtain the highest possible efficiency.

Table 1. Numeric data for 18-LED load

Line voltage	90 V	96 V	102 V	108 V	114 V	120 V	126 V	132 V	138 V
Input power, watts	20.5	20.77	20.82	20.61	20.51	20.46	20.31	19.95	19.48
Power factor	0.973	0.978	0.982	0.985	0.987	0.988	0.990	0.991	0.991
Output voltage	54.8	54.8	54.7	54.7	54.6	54.6	54.5	54.4	54.3
Output current, amps	0.348	0.353	0.355	0.352	0.351	0.35	0.348	0.342	0.334
Output power, watts	19.070	19.344	19.418	19.254	19.164	19.110	18.966	18.604	18.136
Efficiency%	93.03	93.14	93.27	93.42	93.44	93.40	93.38	93.26	93.10
Power loss, watts	1.429	1.425	1.401	1.355	1.345	1.350	1.344	1.345	1.343

5 Graphical data

Figure 8. LED current vs. line voltage for 18

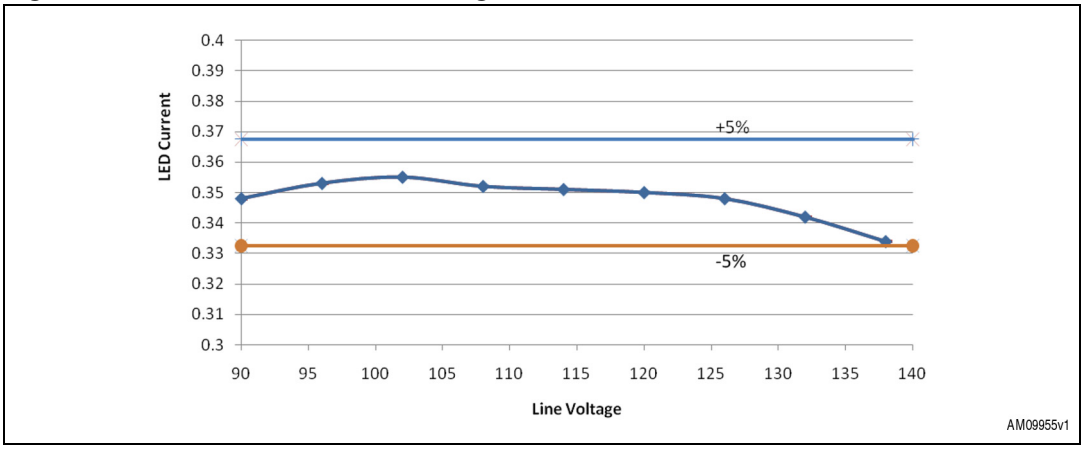


Figure 9. Power factor vs. line voltage

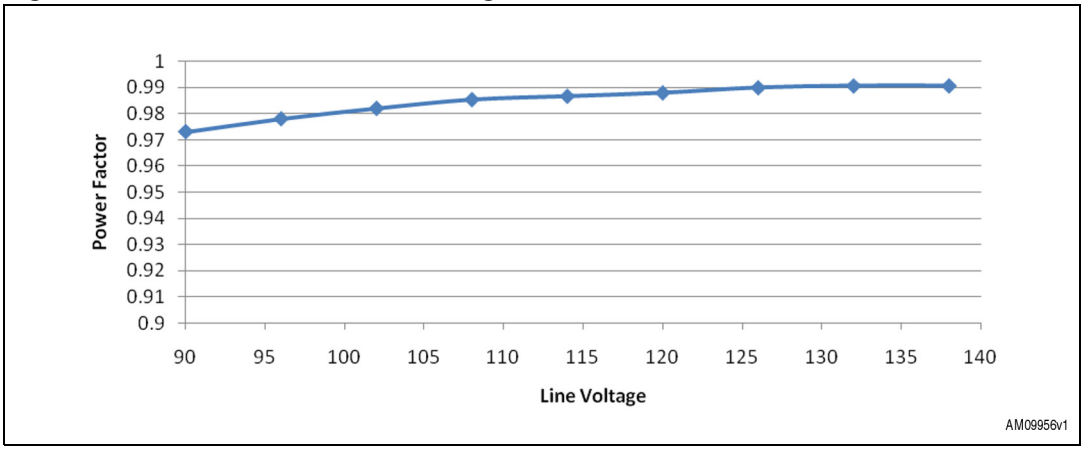


Figure 10. Efficiency vs. line voltage

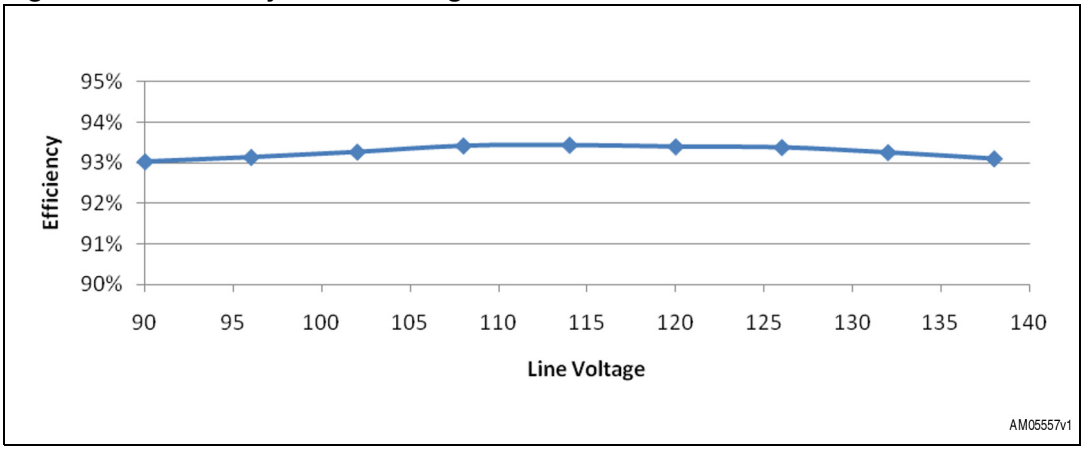
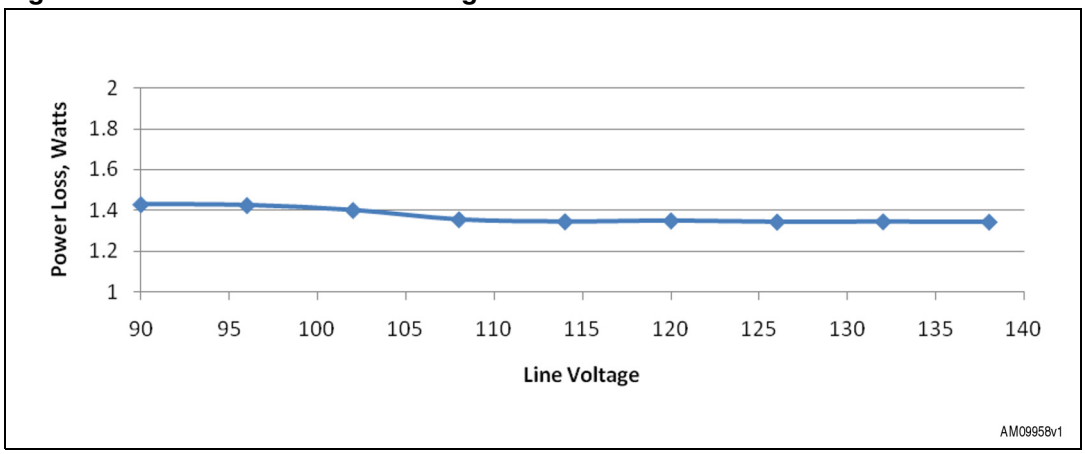


Figure 11. Power loss vs. line voltage



6 Waveforms

Trace colors:

- Yellow = line voltage, 50 V/div ref 0
- Magenta = line current, 100 mA/div ref 0
- Blue = LED voltage, 10 V/div ref -3 div
- Green = LED current, 100 mA/div ref -3 div

Figure 12. Waveforms at 96 V line

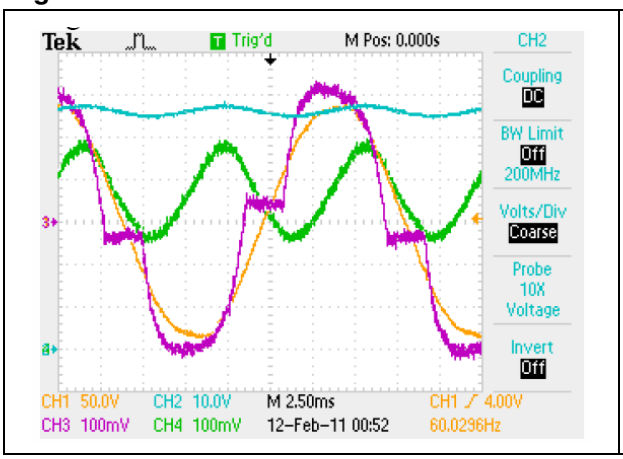


Figure 13. Waveforms at 108 V line

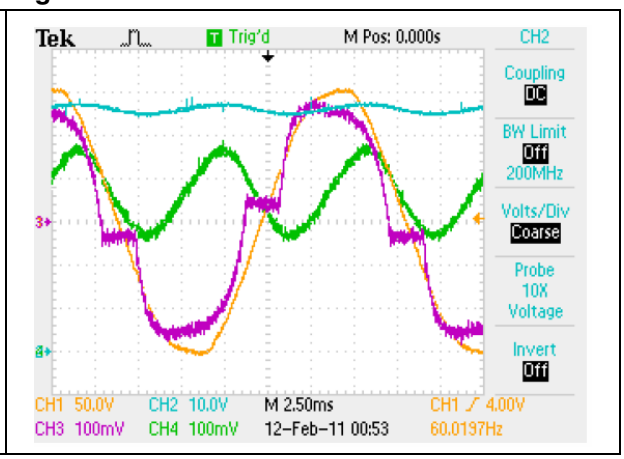


Figure 14. Waveforms at 120 V line

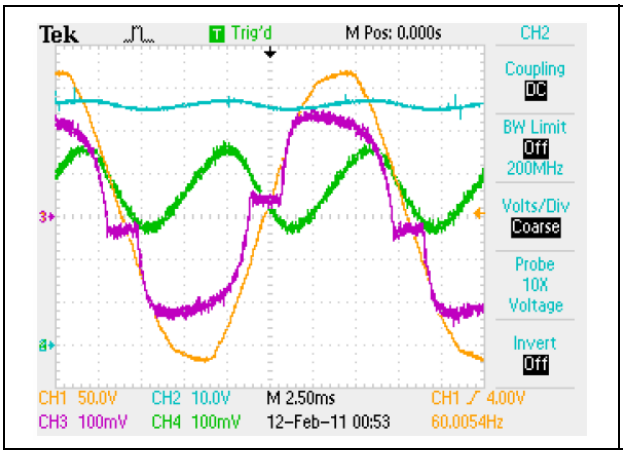
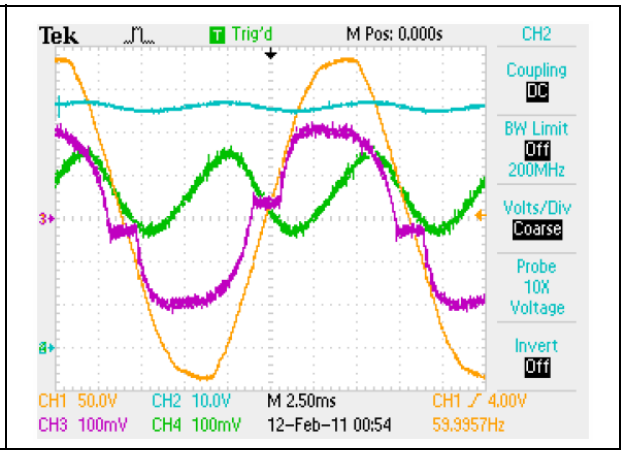


Figure 15. Waveforms at 132 V line



Note that the flat spot near the zero crossing becomes longer as the load voltage becomes a larger percentage of the line voltage (low line is worst). This will place an upper limit on the LED output voltage as waveform distortion reduces power factor. The design can be pushed to higher numbers of LEDs, up to the point where power factor or THD become limiting factors.

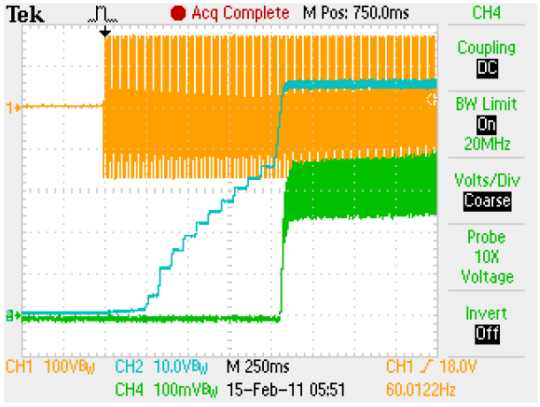
7 Startup

Startup scope photo - cold start, everything discharged, 7 LEDs, 120 V input.

Trace colors:

- Yellow AC line, 100 V/div, ref +2 div
- Blue LED voltage, 10 V/div, ref -3 div
- Green LED current, 100 mA/div, ref -3 div

Figure 16. Startup waveforms



This startup time is too long for some applications. Some circuitry should be added to increase the current limit during startup. An R-C series network could be added from U1 pin 1 to ground (pin 8). The network would have no effect once the feedback loop takes over – the voltage on pin 1 is stable at 2.5 V.

The time can also be reduced by reducing the value of R7, but this will reduce efficiency.

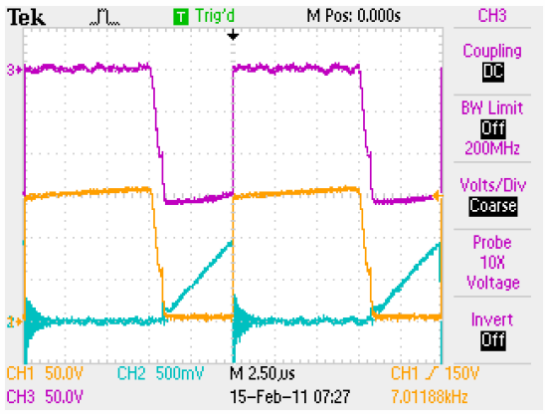
8 Component stress

This plot was taken near the peak of line voltage, where stresses are greatest.

Trace colors:

- Yellow Q2 drain voltage, 100 V/div, ref -3 div
- Blue Q2 drain current, 0.735 A/div, ref -3 div
- Magenta D1 diode voltage, 100 mA/div, ref -3 div

Figure 17. Component electrical stress



9 Thermal stress

It is not likely that the layout will be used as is by the customer. The temperatures below are for guidance only – measurements were taken after 30 minutes operation, in open air, on the workbench, in a 25.3 °C ambient, 120 V input, 18 LED load. The board axis was horizontal, board position vertical. L3 was above L2.

Table 2. Thermal stress

Component	Temperature
L2	40.3
BR1	62.4
Q2	52.5
L1	51.4
L3	46.1
U1	42.3
D1	59.3
C2	32.2

10 Conducted EMI

The following plots each show the maximum of 3 successive sweeps (peak hold).

Figure 18. Conducted EMI, line 1

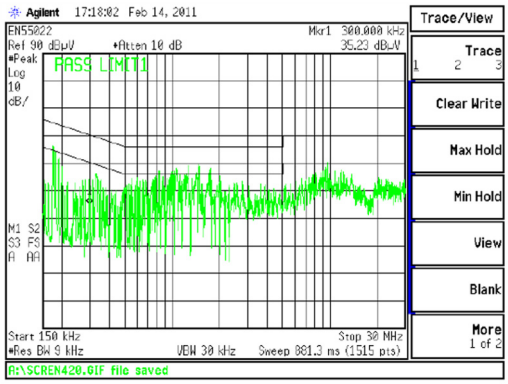
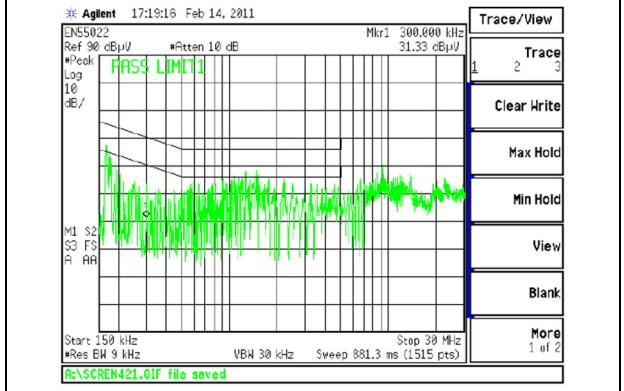


Figure 19. Conducted EMI, line 2



This unit should pass average and quasi-peak testing as is. If difficulties are encountered, the values of C7 and C1 can be increased at the expense of reduced power factor.

11 PC layout

Figure 20. Top side foil

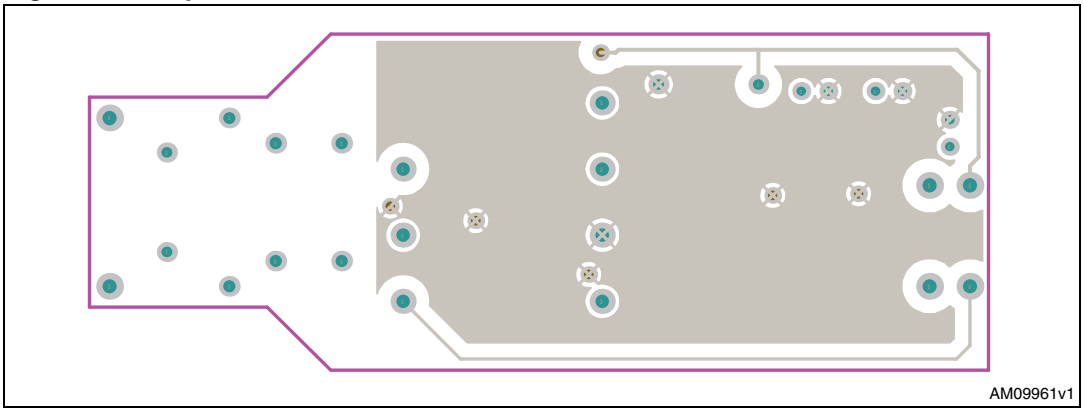


Figure 21. Top side placement

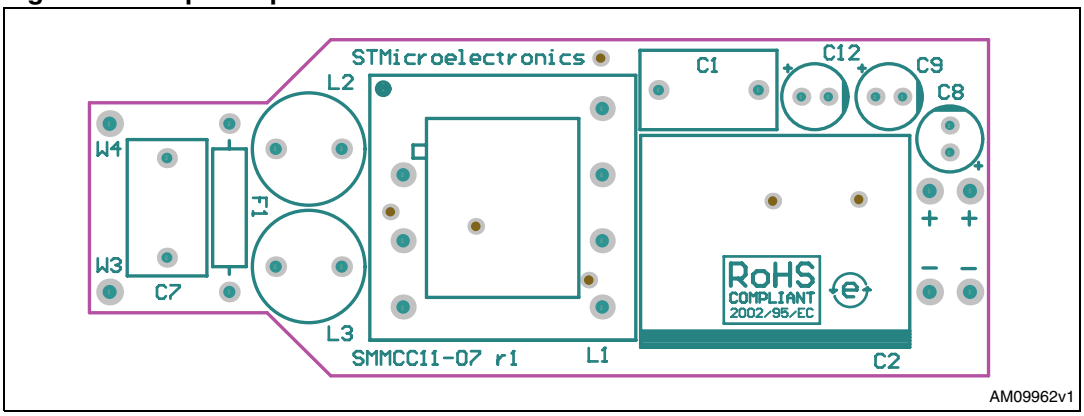


Figure 22. Bottom side layout

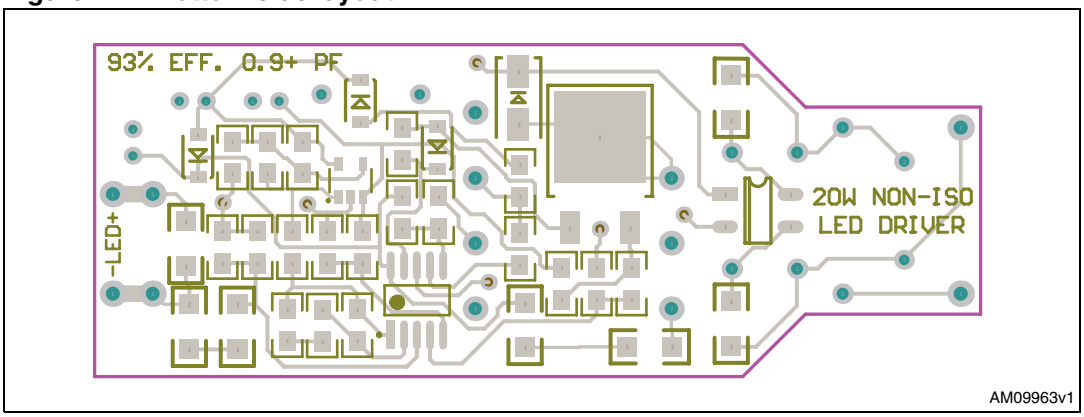
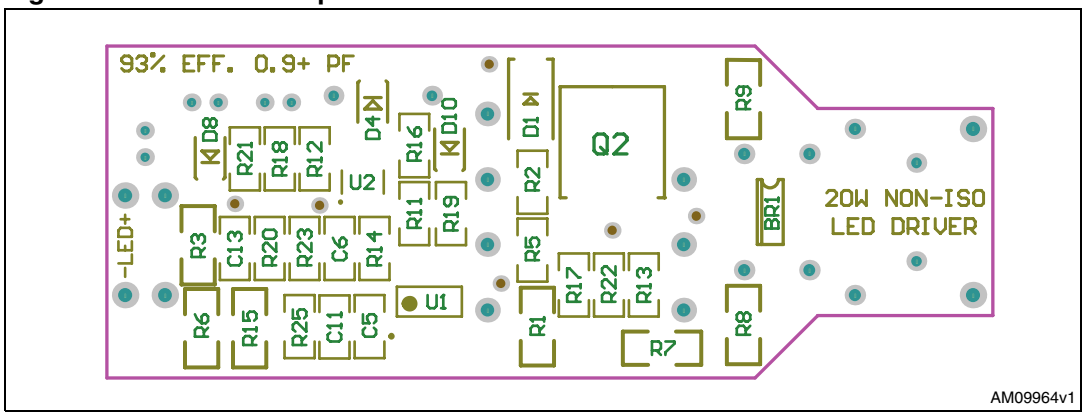


Figure 23. Bottom side placement



12 Bill of materials

Table 3. BOM

Designator	Comment	Description	Footprint	Manufacturer	Vendor
BR1	Bridge 0.8 A	1A DIP bridge	RH0x	Diodes Inc HD06	Digi-Key HD06DICT-ND
C1, C7	220 nF 250 V	Capacitor	BOXSDLWH7.5 -0.6-10.3-6-10.8	Panasonic ECQ-E2224KB	Digi-Key P10971-ND
C2	470 µF 63 V	Capacitor	CEH16x20 mm	Panasonic EEU-FC1J471	Digi-Key P10352-ND
C5	0.1 µF	Capacitor	0805	0805 X7R	
C6	1.0 µF	Capacitor	0805	Murata GRM21BR71C105MA01L	Digi-Key 490-1692-1-ND
C8, C9, C12	22 µF 25 V	Capacitor	CEV5MMP	Panasonic EEA-FC1E220	Digi-Key FC series P11213-ND
C11	2.2 µF	Capacitor	0805	0805 Z5V	
C13	2.2 nF	Capacitor	0805	0805 X7R	
D1	STTH1R04A	Diode	SMA	ST STTH1R04A	
D4, D8, D10	MMSD4148	Diode	SOD-123	Fairchild MMSD4148	Digi-Key MMSD4148-ND
F1	1 A	Fuse	RES0.5	Littelfuse 0251001.MXL	Digi-Key F2313-ND
L1	Cramer E35882 inductor		Shulin EF-20 bobbin	Cramer E35882 Inductor	
L2, L3	1 mHy 0.5 A	Inductor	INDUC9MMVERT	Wurth 744 772 102	
Q2	STD5NM50	FET N-CHAN	D-PAK	ST STD5NM50	
R1, R7	47 kΩ	Resistor	1206	1206 5%	
R2	47 Ω	Resistor	0805	0805 5%	
R3, R6, R15	220 kΩ	Resistor	1206	1206 5%	
R5	47 kΩ	Resistor	0805	0805 5%	
R8, R9	10 kΩ	Resistor	1206	0805 5%	
R11	150 kΩ 1%	Resistor	0805	0805 1%	
R12	453 kΩ 1%	Resistor	0805	0805 1%	
R13	0 Ω jumper	Resistor	0805	0805 000	
R14	681 kΩ 1%	Resistor	0805	0805 1%	
R16	200 Ω	Resistor	0805	0805 5%	
R17	20.0 kΩ 1%	Resistor	0805	0805 1%	
R18	25.2 kΩ 1%	Resistor	0805	0805 1%	

Table 3. BOM (continued)

Designator	Comment	Description	Footprint	Manufacturer	Vendor
R19	10 kΩ 1%	Resistor	0805	0805 1%	
R20	10 kΩ	Resistor	0805	0805 1%	
R21	1.40 kΩ 1%	Resistor	0805	0805 1%	
R22	0.681 Ω 1%	Resistor	0805	0805 1%	
R23	100 kΩ	Resistor	0805	0805 5%	
R25	180 kΩ	Resistor	0805	0805 5%	
U1	L6564	Transition mode PFC controller	SSOP10	ST L6564	
U2	TS321AILT	Low power op amp in SOT23-5L	SOT-23-5L	ST TS321AILT	Digi-Key 497-8093-1-ND

13 References

1. “Design equations of high-power-factor flyback converters based on the L6561” (AN1059)
2. L6561 PFC controller datasheet
3. L6562 PFC controller datasheet
4. L6562A PFC controller datasheet
5. L6564 PFC controller datasheet
6. STD5NM50 datasheet
7. STTH1R04A datasheet
8. “Low-cost LED driver for an A19 lamp” (AN3256)

14 Revision history

Table 4. Document revision history

Date	Revision	Changes
05-Sep-2011	1	Initial release.