2 Efficiency measurement

Table 1 shows the overall efficiency, measured at 230 V - 50 Hz and 115 V - 60 Hz input voltage and different loads.

At 115 V_{AC} and full load the overall efficiency is 90.96%. It increases up to 93.38% at 230 V_{AC}, confirming that this reference design is suitable for high-efficiency power supplies. The efficiency has been measured at 25%, 50%, 75% and 100%, and the average efficiency according to the ES-2 standard has been calculated. As shown in *Table 1* it is very high at both nominal mains.

Table 1. STEVAL-ILL053V1 evaluation board: overall efficiency vs. load

Load	230 V - 50 Hz					115 V - 60 Hz				
	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	P_{IN} [W]	Eff. [%]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	P_{IN} [W]	Eff. [%]
25% load	47.58	0.689	32.8	37.87	86.57%	47.59	0.689	32.8	37.87	86.58%
50% load	47.57	1.378	65.6	71.66	91.48%	47.58	1.378	65.6	72.93	89.90%
75% load	47.56	2.008	95.5	102.96	92.75%	47.56	2.001	95.2	105.0	90.64%
100% load	47.55	2.708	128.8	137.6	93.38%	47.56	2.703	128.6	141.33	90.96%
Average efficiency					91.04%					89.52%

The measured output voltage at different load conditions is also shown in *Table 1*. As visible, the voltage is very stable over the entire output load range.

The measured efficiency is shown in *Figure 3*, while *Figure 4* shows the efficiency at maximum load over the entire AC input voltage mains range.

Figure 3. STEVAL-ILL053V1 evaluation board: efficiency vs. load

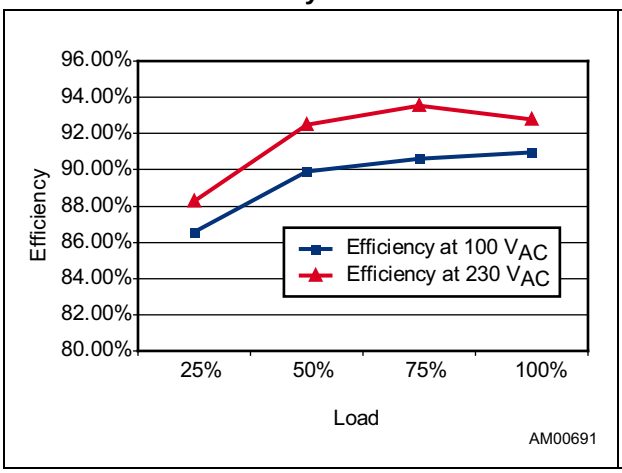
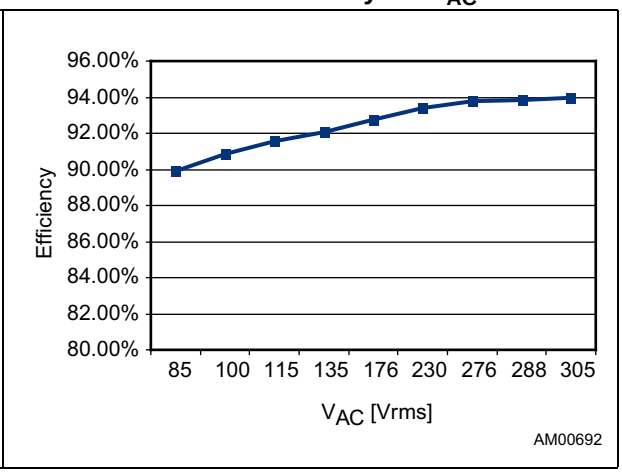


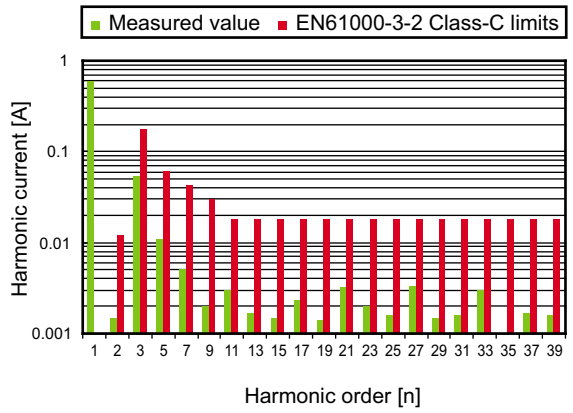
Figure 4. STEVAL-ILL053V1 evaluation board: full-load efficiency vs. V_{AC}



3 Input current harmonics measurement

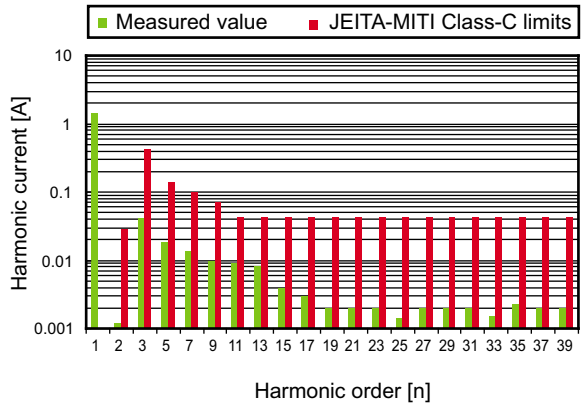
One of the main purposes of a PFC precondition is the correction of input current distortion, decreasing the harmonic contents below the limits of the relevant regulations. Therefore, this evaluation board has been tested according to the European norm EN61000-3-2 Class-C and Japanese norm JEITA_MITI Class-C both relevant to lighting equipment, at full load and nominal input voltage mains. The measurements are shown in *Figure 5* and *Figure 6*.

Figure 5. STEVAL-ILL053V1 evaluation board: compliance to EN61000-3-2 Class-C standard



V_{IN} = 230 V_{AC} - 50 Hz, P_{IN} = 138.8 W
THD = 8.70%, PF = 0.976

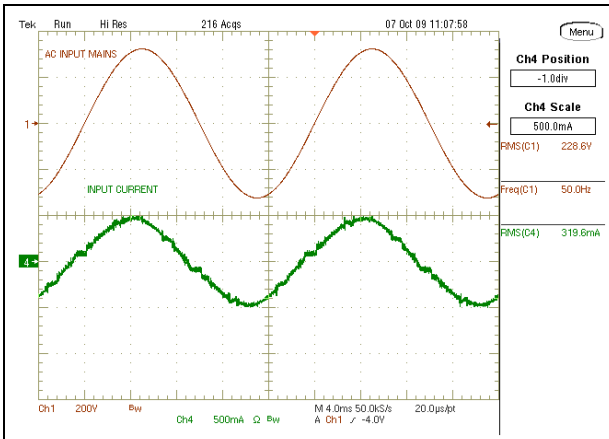
Figure 6. STEVAL-ILL053V1 evaluation board: compliance to JEITA-MITI Class-C standard



V_{IN} = 100 V_{AC} - 50 Hz, P_{IN} = 141.3 W
THD = 3.31%, PF = 0.994

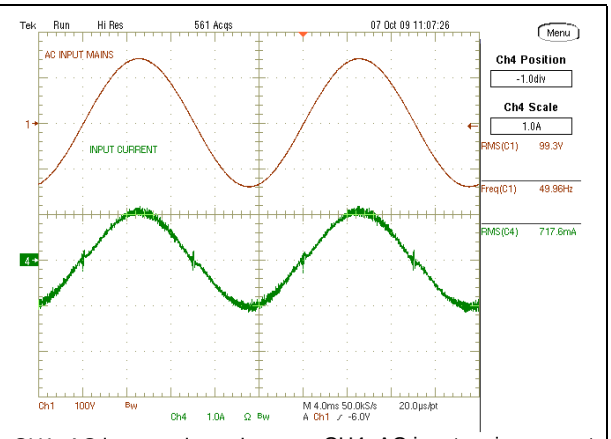
For user reference, waveforms of the input current and voltage at nominal input voltage mains during full-load operation are shown in *Figure 5* and *Figure 6*. *Figure 7* and *Figure 8* give the input current and voltage at nominal input voltage mains 50% load, showing that in spite of the wide input voltage range, the current waveform shape is still good.

Figure 7. STEVAL-ILL053V1 evaluation board: input current waveform at 230 V - 50 Hz - 65 W load



CH1: AC input mains voltage CH4: AC input mains current

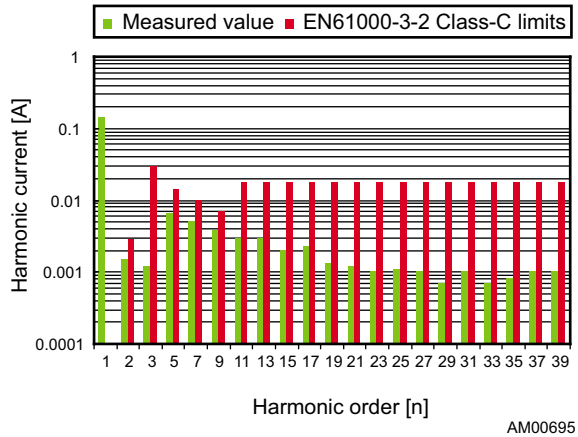
Figure 8. STEVAL-ILL053V1 evaluation board: input current waveform at 100 V - 50 Hz - 65 W load



CH1: AC input mains voltage CH4: AC input mains current

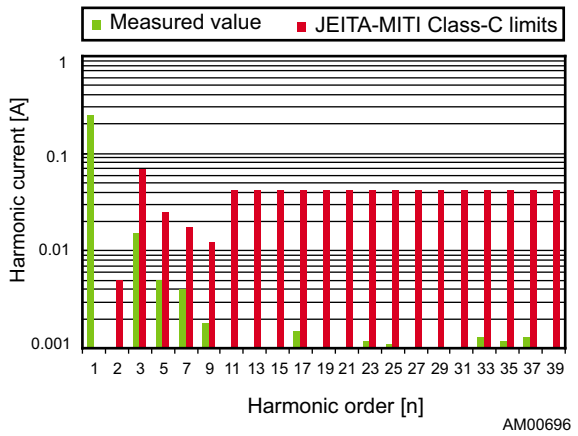
As confirmed by the previous graphs, the circuit also shows its ability to reduce the harmonics well below the limits of EN61000-3-2 Class-C regulation not only at full load but also at a significantly lower load. The input current harmonics measurement at 25 W (minimum input power to be compliant with the previously mentioned rules is 25 W) shows that even if the power supply is working from its typical operating region, it is still compliant with the EN61000-3-2 Class-C limits. Test results are shown in *Figure 9* and *Figure 10*.

Figure 9. STEVAL-ILL053V1 evaluation board: compliance to EN61000-3-2 Class-C standard



V_{IN} = 230 V_{AC} - 50 Hz, P_{IN} = 25 W
THD = 11.80%, PF = 0.697

Figure 10. STEVAL-ILL053V1 evaluation board: compliance to JEITA-MITI Class-C standard



V_{IN} = 100 V_{AC} - 50 Hz, P_{IN} = 25 W
THD = 6.65%, PF = 0.92

The “Power Factor” (PF) and the “Total Harmonic Distortion” (THD) versus load variations have been measured too and the results are shown in *Figure 11* and *Figure 12*. As visible, the Power Factor remains close to unity and the Total Harmonic Distortion is very low throughout the input voltage mains.

Figure 11. STEVAL-ILL053V1 evaluation board: Power Factor vs. output power

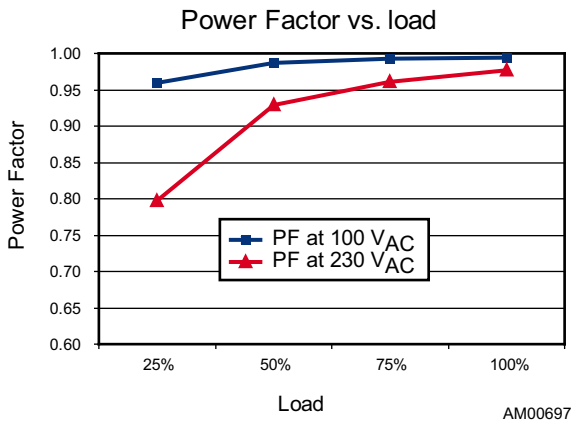
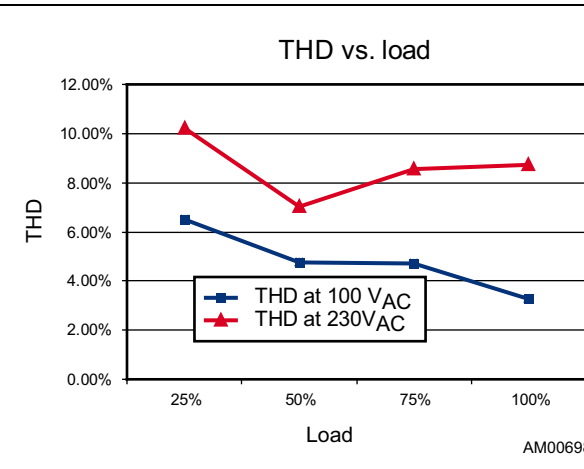


Figure 12. STEVAL-ILL053V1 evaluation board: Total Harmonic Distortion vs. output power



4 Functional check

4.1 PFC circuit

In *Figure 13* and *Figure 15* some waveforms relevant to the PFC stage have been captured during full load operation at nominal 230 V_{AC} and 115 V_{AC}. In both figures it is visible that the envelope of the CS pin (#4) waveforms of the L6562AT is in phase with the MULT pin (3#) and has same sinusoidal shape, demonstrating the proper functionality of the PFC stage. It is also possible to measure the peak-to-peak value of the voltage ripple superimposed on the PFC output voltage due to the low value of the PFC output capacitors. In *Figure 14* and *Figure 16* the details of some waveforms at the switching frequency are shown.

Figure 13. STEVAL-ILL053V1 evaluation board: PFC stage and L6562AT waveforms at 230 V - 50 Hz - full load

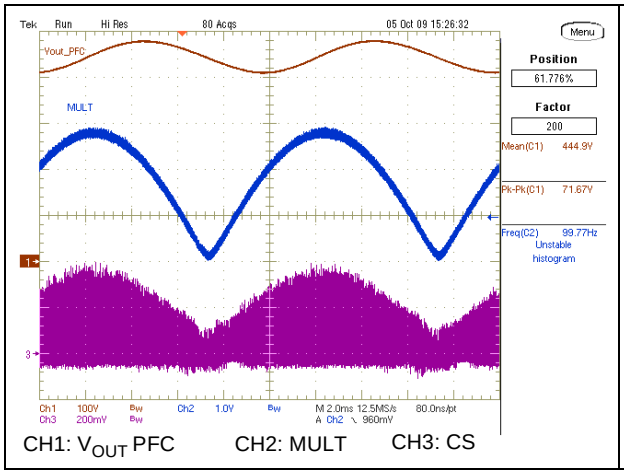


Figure 14. STEVAL-ILL053V1 evaluation board: PFC stage and L6562AT waveforms at 230 V - 50 Hz - full load - detail

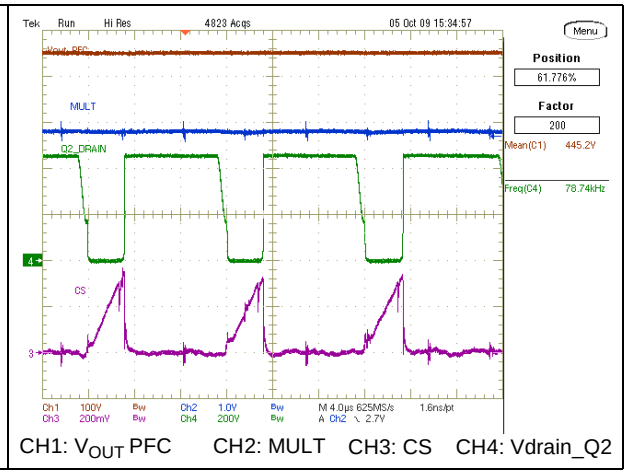


Figure 15. STEVAL-ILL053V1 evaluation board: PFC stage and L6562AT waveforms at 115 V - 60 Hz - full load

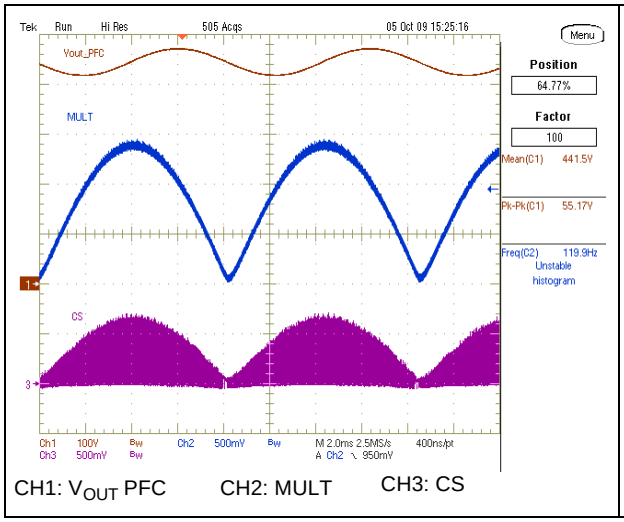
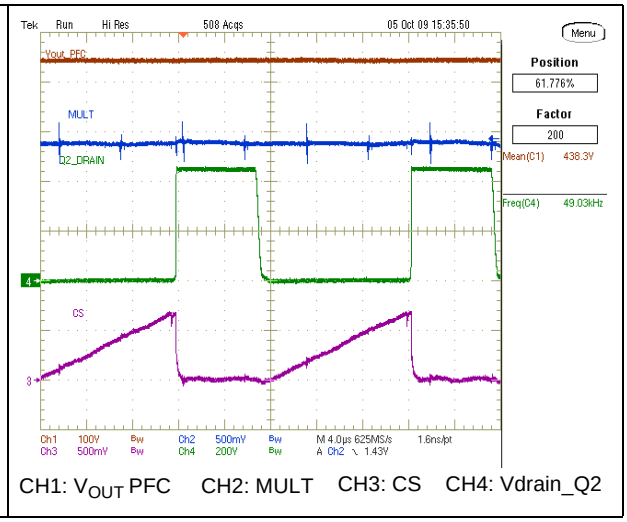


Figure 16. STEVAL-ILL053V1 evaluation board: PFC stage and L6562AT waveforms at 115 V - 60 Hz - full load - detail



4.2 Half-bridge resonant LLC circuit

The following figures show waveforms relevant to the resonant stage during steady-state operation. The resonant stage switching frequency is about 100 kHz, in order to have a good trade-off between transformer losses and dimensions.

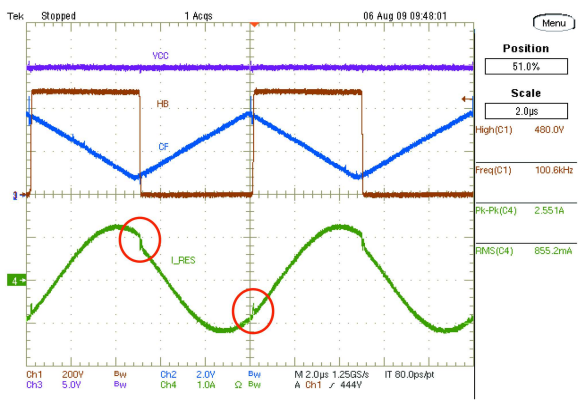
The LLC converter has been designed to operate at nominal voltage and full load at the resonance frequency, but due to the PFC output voltage ripple at twice the mains frequency, it is driven slightly above and below the resonant tank frequency, according to the instantaneous value of the PFC output voltage.

In *Figure 17* some waveforms relevant to the resonant stage ZVS operation are shown. We note that both MOSFETs are turned on when resonant current is flowing through their body diodes and drain-source voltage is almost zero, thus achieving good efficiency because the turn-on losses are negligible. The HB MOSFET voltage de-rating and low operating temperature allow increasing the board's MTBF.

The current flowing in the resonant tank is sinusoidal. In *Figure 17* we note a slight asymmetry of operating modes by each half portion of the sine wave. The half cycle is working at resonant frequency while the other one is working above the resonant frequency. This is due to a small difference between each half-secondary leakage inductance of the transformer reflected to the primary side, providing the two slightly different resonant frequencies. This phenomenon is typically due to a different coupling of the transformer secondary windings and, in this case, it is not an issue. The slight asymmetry is also visible in *Figure 18* where the small ringing appearing on both secondary rectifiers anode voltage indicates that for a short time the rectifiers are not conducting. This demonstrates that during the half cycle the circuit is working below the resonant frequency, while during the following half cycle it is working at the resonant frequency.

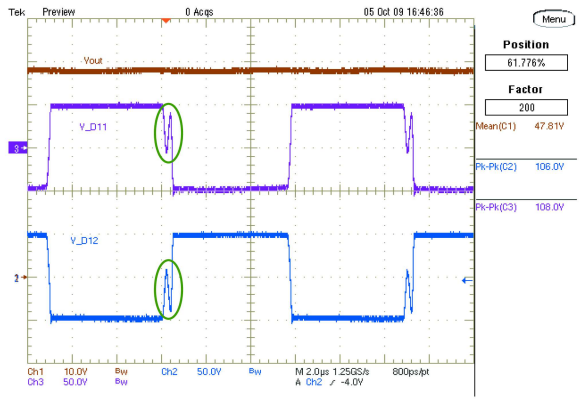
In *Figure 18* we also note the rectifier operating voltage and its margin with respect to the maximum reverse voltage (V_{RRM}). This de-rating with respect to the rectifiers V_{RRM} guarantees good reliability of the output rectifiers, increasing the board's total MTBF.

Figure 17. STEVAL-ILL053V1 evaluation board: primary side LLC waveforms at 115 V - 60 Hz - full load



CH1: HB voltage
CH2: CF pin voltage
CH3: V_{CC}
CH4: res. tank current

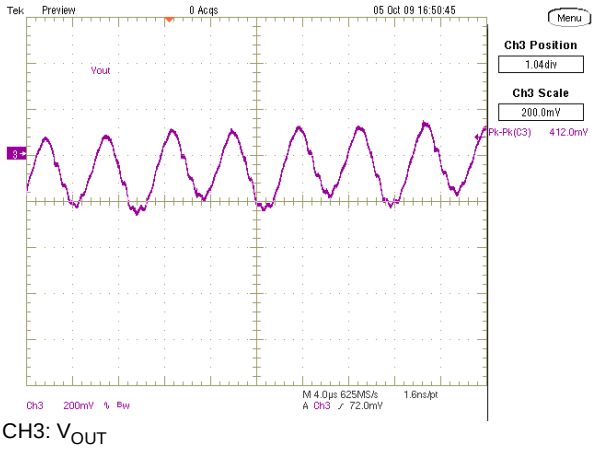
Figure 18. STEVAL-ILL053V1 evaluation board: secondary side LLC waveforms at 230 V- 50 Hz - full load



CH1: V_D12
CH2: V_D12
CH3: V_{OUT}

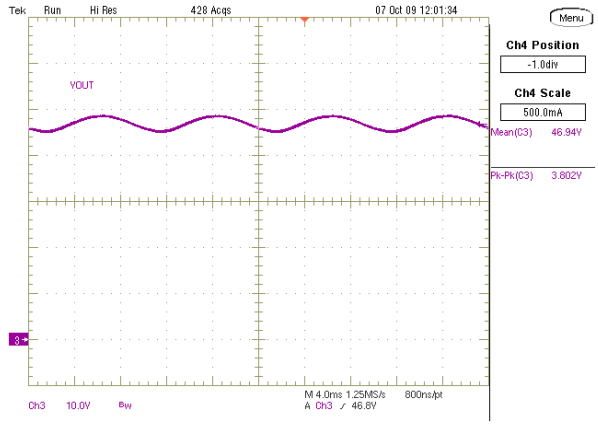
In *Figure 19* the high-frequency ripple has been measured. As visible the ripple and noise at switching frequency is very limited, thanks to the low EMI generated by both stages. In *Figure 20* the low-frequency ripple has been measured too. We note that the peak-to-peak value is not very low because of the low output capacitances but it doesn't affect the application. In fact the converters regulating the current flowing in each LED strip can reject the ripple without any problem.

Figure 19. STEVAL-ILL053V1 evaluation board: high frequency ripple on output voltage at 115 V - 60 Hz - full load



CH3: V_{OUT}

Figure 20. STEVAL-ILL053V1 evaluation board: low frequency ripple on output voltage at 115 V - 60 Hz - full load



CH3: V_{OUT}

4.3 Dynamic load operation

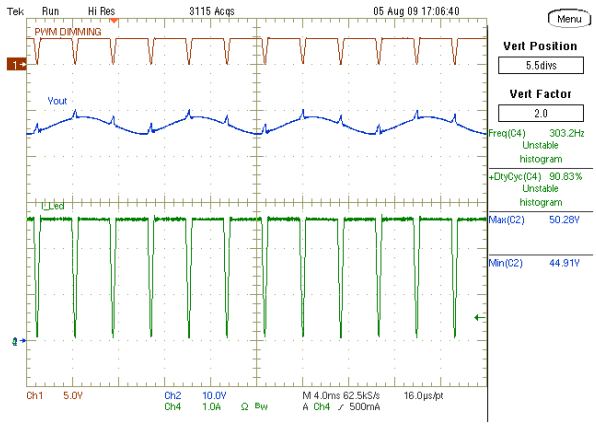
The waveforms shown in *Figure 21* and *Figure 22* pertain to the evaluation board during the operation of supplying converters dedicated to power LED strips with constant current.

In both figures it is possible to see the output voltage modulation during operation with variable load due to the dimming of the LED current by PWM. For both measurements, the dimming frequency has been chosen at 300 Hz, a typical value for dimming.

In *Figure 21* the converter's output current was 2.6 A and the dimming duty cycle was 90%, thus very close to the converter's nominal output power. The output voltage has two modulations. One is due to the rejection of the PFC output voltage ripple already measured in *Figure 20* where the voltage variation due to the LED current dimming is superimposed. The peak-to-peak variation is 5.37 V but it doesn't present any problem for the load since the converters reject the modulation.

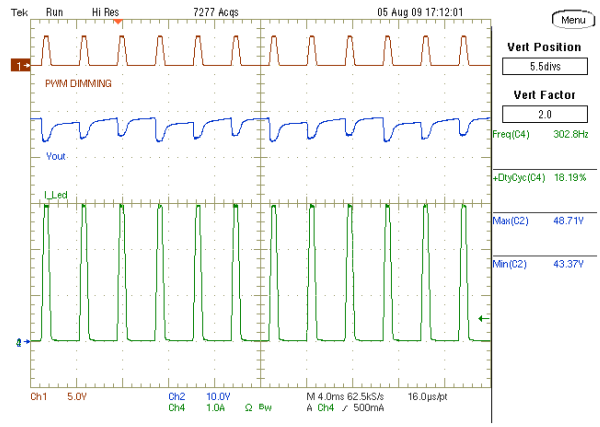
In *Figure 22* instead the converter has been checked at light load, so the peak output current was 3 A and the dimming duty cycle was 15%, for an output power of 21 W. Even in this case, the peak-to peak modulation doesn't present any issue for the downstream current regulators and the board still works correctly.

Figure 21. STEVAL-ILL053V1 evaluation board: output voltage variation driving a CC LED converter - PWM = 90%



CH1: PWM dimming signal
CH4: SMPS output current
CH2: V_{OUT}

Figure 22. STEVAL-ILL053V1 evaluation board: output voltage variation driving a CC LED converter - PWM = 15%



CH1: PWM dimming signal
CH4: SMPS output current
CH2: V_{OUT}

Please note that for correct operation with LED strips, the board needs additional capacitors connected on the +48 V output bus. The board has not been equipped with all of the capacitors necessary for correct operation with LEDs, but only with minimum capacitance to allow board operation in order to optimize the system cost and reliability. The additional capacitors needed are intended to be placed close to each LED strip current regulator, thus filtering the EMI generated by these. In several cases, in fact, the power supply is placed at the base of the lighting pole while the LED current regulators are located on top, in the lamp. The long connection wiring between the power supply and the converters can act as an antenna radiating EMI. Thus local filtering minimizes the radiated EMI.

The capacitance to be added to the 48 V bus for correct operation with LEDs is around 40 µF. In order to not affect the board MTBF, we suggest using the same type of capacitors already used on the power supply board.

4.4 Overcurrent and overvoltage protection

The L6599AT is equipped with a current sensing input (pin #6, ISEN) and a dedicated overcurrent management system. The current flowing in the resonant tank is detected and the signal is fed into the ISEN pin. It is internally connected to a first comparator, referenced to 0.8 V, and to a second comparator referenced to 1.5 V. If the voltage externally applied to the pin exceeds 0.8 V, the first comparator is tripped, causing an internal switch to be turned on and discharging the soft-start capacitor C24 (CSS).

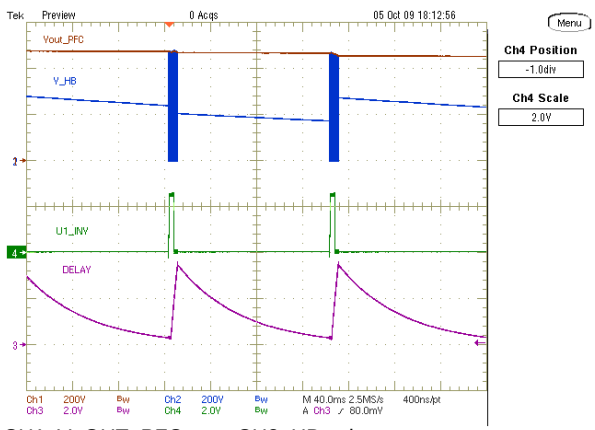
Under output short-circuit, this operation results in a nearly constant peak primary current.

With the L6599AT the designer can program externally the maximum time that the converter is allowed to run overloaded or under short-circuit conditions. Overloads or short-circuits lasting less than the set time will not cause any other action, hence providing the system with immunity to short duration phenomena. If, instead, the overload condition persists, a protection procedure is activated that shuts down the L6599AT. In case of continuous overload or short-circuit, it will result in continuous intermittent operation with a user-defined duty cycle.

This function is implemented with the DELAY pin (#2), by means of a capacitor C21 and the parallel resistor R32 connected to ground. As the voltage on the ISEN pin exceeds 0.8 V, the first OCP comparator, in addition to discharging CSS, turns on an internal 150 µA current generator that via the DELAY pin charges C21. As the voltage on C21 is 3.5 V, the L6599AT stops switching and the PFC_STOP pin (#9) is pulled low, turning off also the PFC stage via the L6562AT pin#1 (INV). The internal generator is also turned off, so that C21 will now be slowly discharged by R32. The IC will restart once the voltage on C21 is less than 0.3 V. Additionally, if the voltage on the ISEN pin reaches 1.5 V for any reason (e.g. transformer saturation), the second comparator will be triggered, the L6599AT will shut down and the operation will be resumed after recycling of the V_{CC}. In this evaluation board the intervention of the second level comparator will latch the operation of the L6599AT and the PFC_STOP pin (#9) will stop the PFC. Both controllers will no longer be powered by V_{CC} and the latch will be removed and then a new startup cycle will take place. This sequence continues until the short is removed.

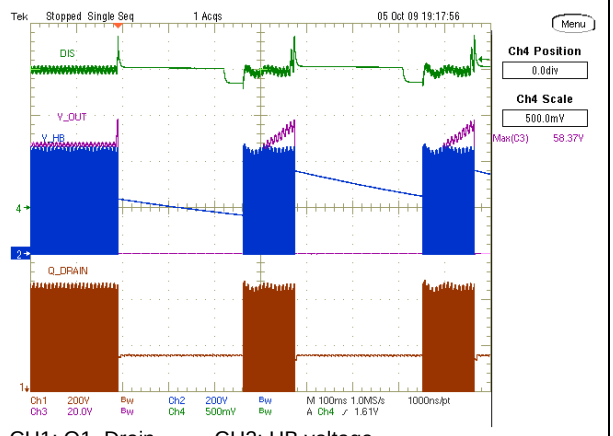
Figure 23 shows the operation of the DELAY pin and the consequent hiccup mode operation of the board during short-circuit operation. Thanks to the narrow operating time with respect to the off-time, the average output current as well as the average primary current are limited. This will avoid converter overheating and consequent failures. Removing the short allows the board to resume normal operation.

Figure 23. STEVAL-ILL053V1 evaluation board: short-circuit at 115 V_{AC} - 60 Hz - full load



CH1: V_OUT_PFC CH2: HB voltage
CH3: DELAY pin CH4: U1 pin INV

Figure 24. STEVAL-ILL053V1 evaluation board: open loop at 115 V_{AC} - 60 Hz - 65 W load



CH1: Q1_Drain CH2: HB voltage
CH3: V_{OUT} CH4: DIS pin

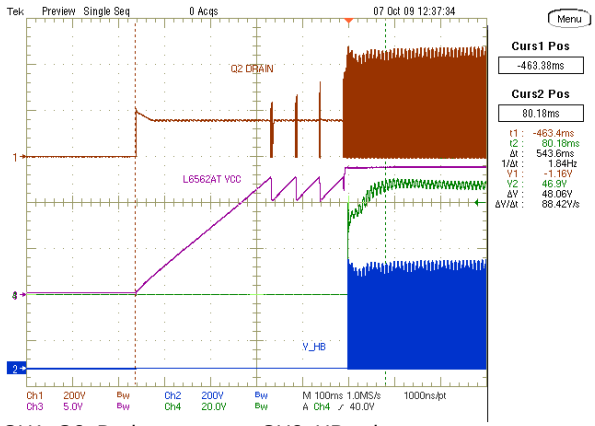
Figure 24 shows the operation of the evaluation board during “open loop” operation by the LLC stage. The open loop operation provides an increase also of the auxiliary voltage that will trigger the L6599AT pin #9 (DIS) protection pin via the Zener diode D17. As a consequence, the L6599AT will shut down, stopping the operation. The L6599AT will activate also the PFC_STOP pin (#9) that will stop the PFC too, thus both controllers will no longer be powered by V_{CC}. Once V_{CC} drops below the UVLO, the latch is removed and then a new startup cycle will take place. This sequence continues until the open loop is removed.

4.5 Converter startup

Figure 25 and *Figure 27* show the converter startup. We note that at 115 V_{AC} the converter begins operation in ~300 ms, while at 230 V_{AC} it takes around 150 ms. This is the time

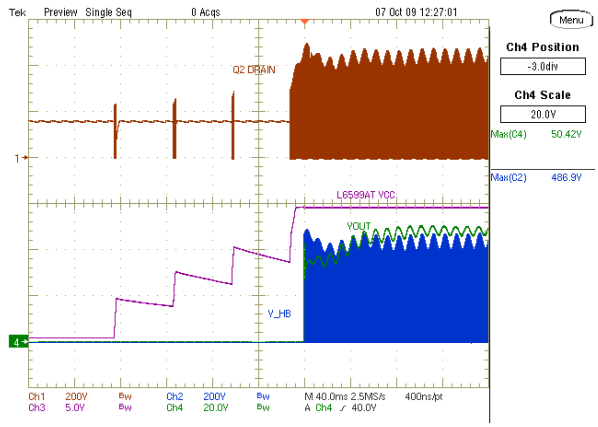
needed to charge the V_{CC} to the L6562AT turn-on voltage. Thus the L6562AT starts switching and the PFC output voltage starts increasing. Once the PFC output voltage reaches the enable level set via the L6599AT LINE pin, even the LLC stage starts switching and the output voltage rises up to the nominal level. The V_{CC} is initially supplied by the PFC coil charge pump, and then once the L6599AT starts operating, the V_{CC} is also provided by the LLC transformer auxiliary winding. The details of converter sequencing can be found in *Figure 26* and *Figure 28*.

Figure 25. STEVAL-ILL053V1 evaluation board: wake-up at 115 V_{AC} - 60 Hz - full load



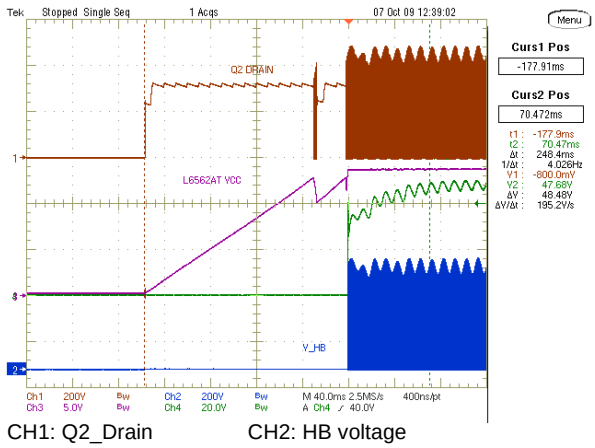
CH1: Q2_Drain CH2: HB voltage
CH3: L6562AT V_{CC} CH4: V_{OUT}

Figure 26. STEVAL-ILL053V1 evaluation board: sequencing at 115 V_{AC} - 60 Hz - full load



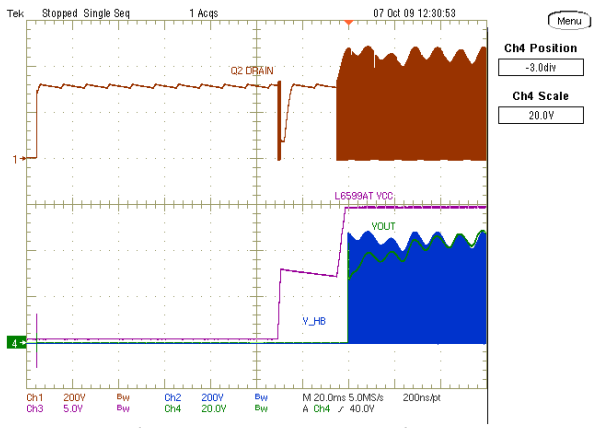
CH1: Q2_Drain CH2: HB voltage
CH3: L6599AT V_{CC} pin CH4: V_{OUT}

Figure 27. STEVAL-ILL053V1 evaluation board: wake-up at 230 V_{AC} - 50 Hz - full load



CH1: Q2_Drain CH2: HB voltage
CH3: L6562AT V_{CC} CH4: V_{OUT}

Figure 28. STEVAL-ILL053V1 evaluation board: sequencing at 230 V_{AC} - 60 Hz - full load



CH1: Q2_Drain CH2: HB voltage
CH3: L6599AT V_{CC} pin CH4: V_{OUT}

Figure 25 through *28* show a correct startup of the board using an active load, with only the capacitors for the 48 V populating the board. Powering current regulators with LEDs may cause the board to show an incorrect startup, with output voltage going up and down and LEDs flashing. As already explained in *Section 4.3*, the board needs an additional 40 µF capacitance on the +48 V.

5 Thermal map

In order to check the design reliability, a thermal mapping by means of an IR camera was done. Here below the thermal measures of the board, component side, at nominal input voltage are shown. Some pointers visible on the pictures have been placed across key components or components showing high temperature. The ambient temperature during both measurements was 27 °C. We note that the PFC part has a different temperature depending on the input mains, while the components of the resonant stage are working at a temperature independent of the mains input voltage.

Figure 29. Thermal map at 115 V_{AC} - 60 Hz - full load - PCB top side

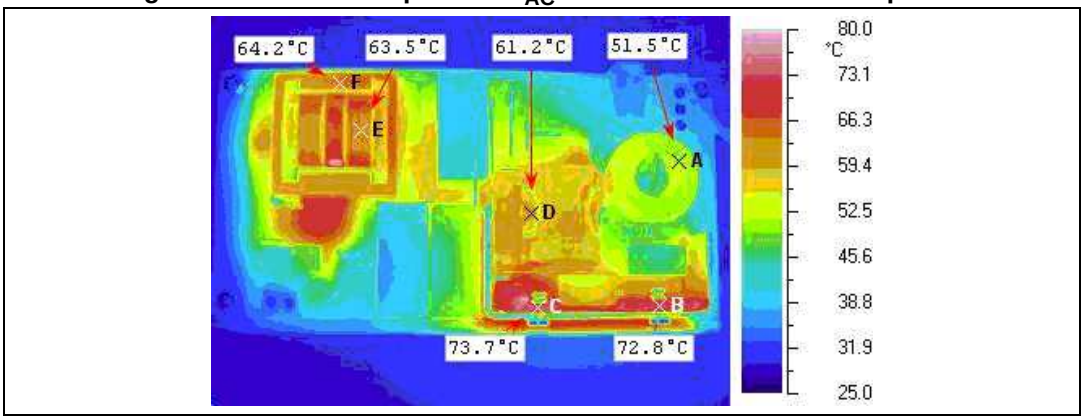


Figure 30. Thermal map at 230 V_{AC} - 50 Hz - full load - PCB top side

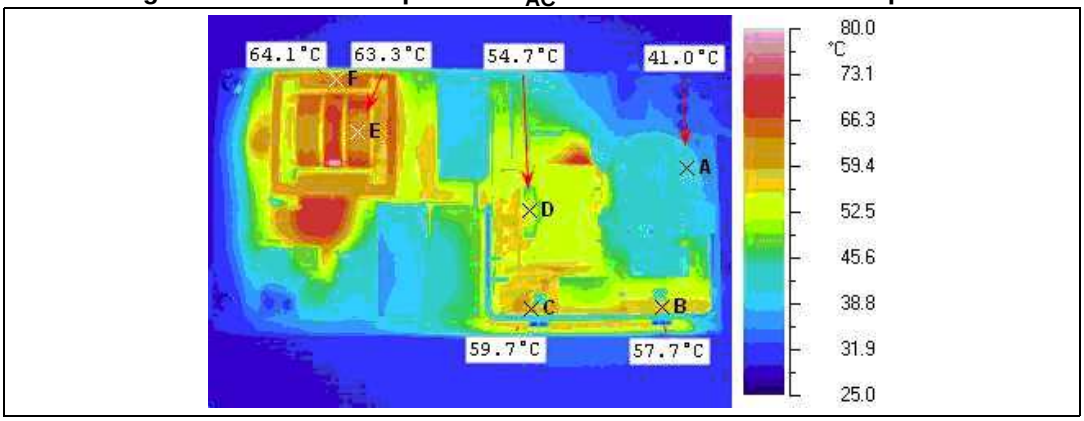


Table 2. Thermal maps reference points - PCB top side

Point	Reference	Description
A	L2	EMI filtering inductor
B	D3	Bridge rectifier
C	Q2	PFC MOSFET
D	L1	PFC inductor
E	T1	Resonant power transformer - winding
F	T1	Resonant power transformer - ferrite core

Figure 31. Thermal map at 115 V_{AC} - 60 Hz - full load - PCB bottom side

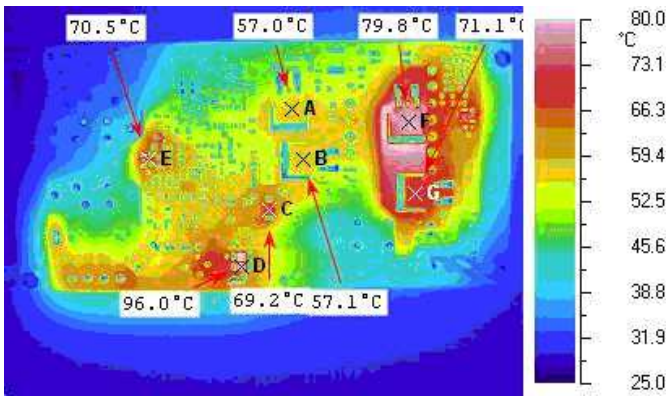


Figure 32. Thermal map at 230 V_{AC} - 50 Hz - full load - PCB bottom side

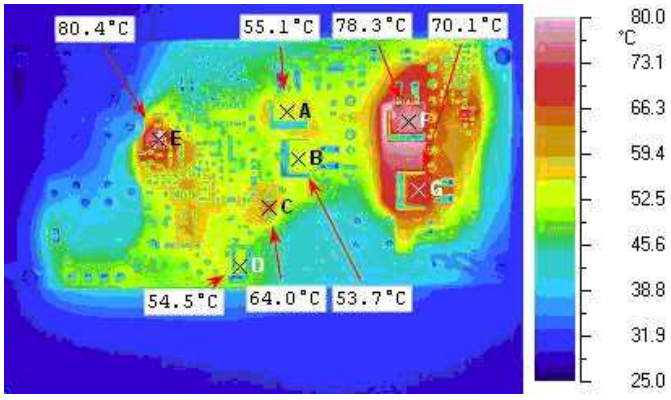


Table 3. Thermal maps reference points - PCB bottom side

Point	Reference	Description
A	Q4	LLC resonant HB MOSFET
B	Q5	LLC resonant HB MOSFET
C	D2	PFC output diode
D	R33 and R34	PFC sense resistors
E	Q1	V_{CC} voltage regulator
F	D12	Output rectifier
G	D11	Output rectifier

6 Conducted emission precompliance measurement

Figure 33 to *Figure 36* show the average measurement of the conducted noise at full load and nominal mains voltages for both wires, line and neutral. The limits on the diagrams are the EN55022 Class-B norms. As visible on the diagrams, in all test conditions the measurements are well below the limits.

Figure 33. CE average measurement at 115 V_{AC} and full load - phase wire

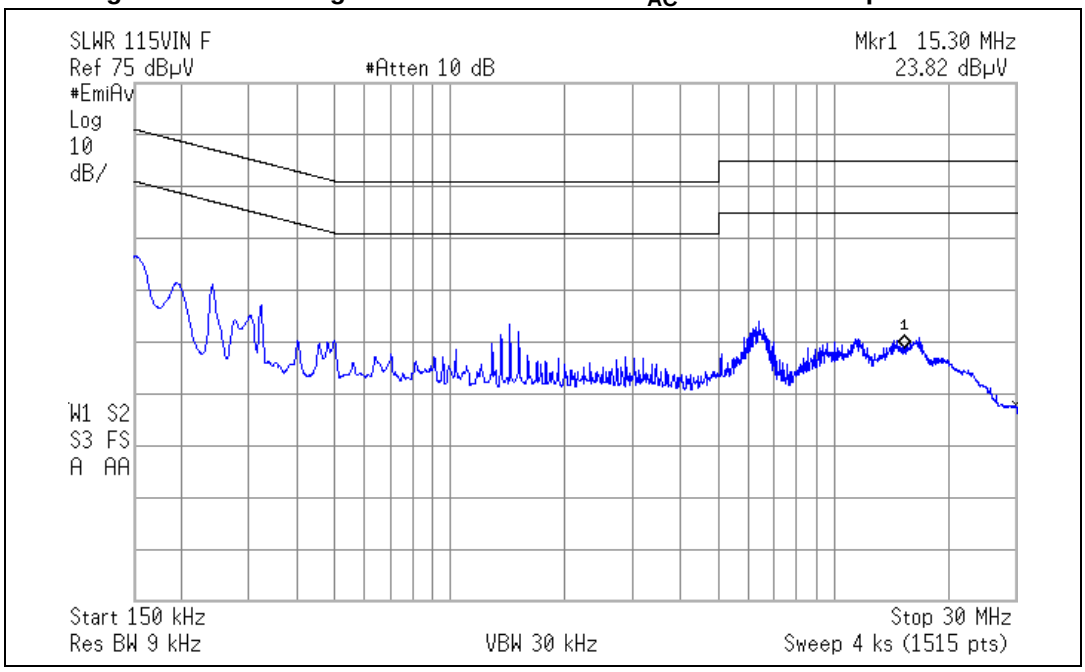


Figure 34. CE average measurement at 115 V_{AC} and full load - neutral wire

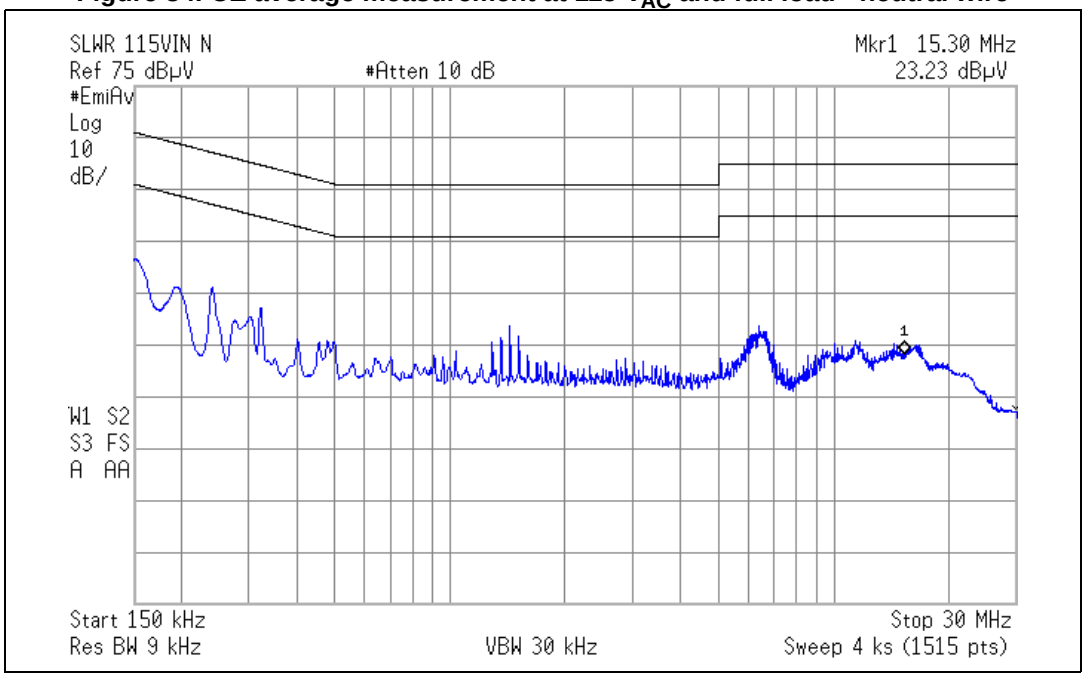


Figure 35. CE average measurement at 230 V_{AC} and full load - phase wire

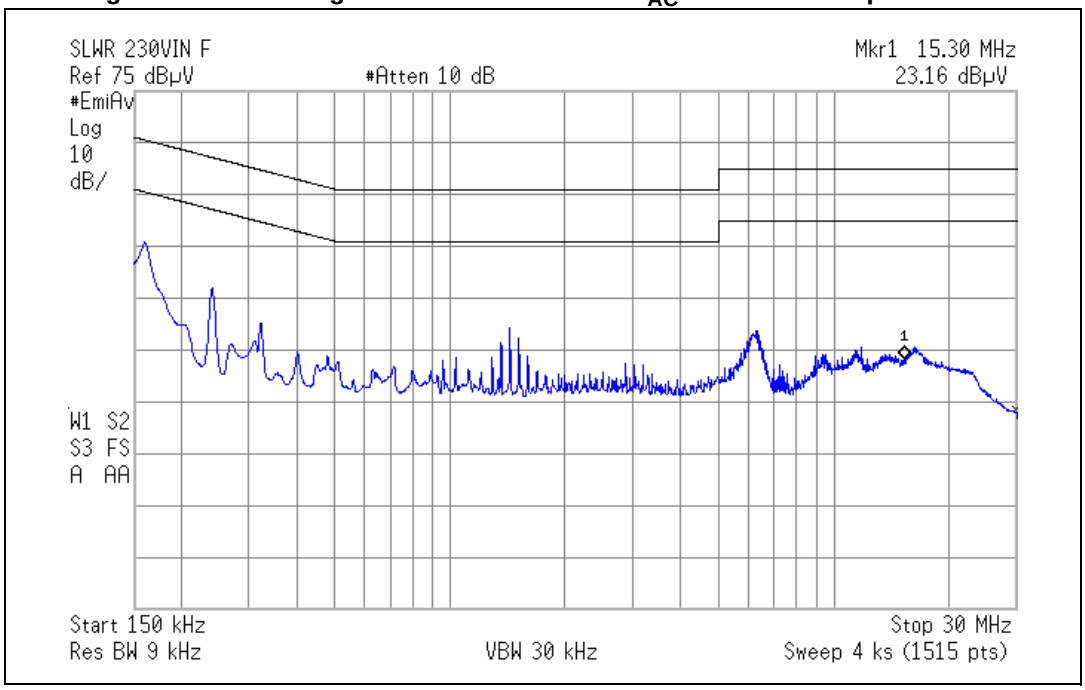


Figure 36. CE average measurement at 230 V_{AC} and full load - neutral wire