

AN4578 Application note

16-channels LED driver with independent PWM dimming control based on LED7708

Introduction

The LED7708 has been specifically designed to supply several LEDs starting from a single low voltage rail. It integrates a boost controller, sixteen current generators and a 4-wires serial interface. The boost controller regulates the output voltage in an adaptive way, according to the LEDs need, resulting in improved overall efficiency. All the current generators are 40 V rated, allowing the LED7708 to drive several LEDs in series on each channel. The channels can be put in parallel for higher output current. The brightness of the LEDs is controlled by using the serial interface. A selectable 12 bit or 16 bit gray scale brightness control allows independent PWM on each channel. A programmable on chip dimming oscillator is provided for external circuitry simplification. The device has dedicated pins to lock synchronized with other devices (master or slave) for noise reduction in multi-device applications. The LED7708 implements basic protections (OVP, OCP and thermal shutdown) as well as LED array protection. It can detect and manage open-LED and shorted-LED faults and different fault-management options are available in order to cover most of applications needs.

This document is intended as a reference guide for getting started with the LED7708 LED driver by means of the STEVAL-ILL035V1 board and a minimum of equipment, basically a DC power supply and a PC.

A general step-by-step component selection procedure is also provided in case a particular application involving the LED7708 in boost configuration has to be designed or cannot directly satisfied by the optional settings of the STEVAL-ILL035V1 evaluation board.



Figure 1. STEVAL-ILL035V1 evaluation board

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1 STEVAL-ILL035V1 evaluation board

The purpose of the STEVAL-ILL035V1 evaluation board is to provide an application example of a compact LED backlight driver using the LED7708 device.

The board is equipped with a LED7708 LED driver and the surrounding components (setting resistors, loop compensation network, power components related to the boost converter section) plus an STM32 microcontroller section to easily control all the features via a USB connection.

The output voltage required by the LED strings connected to the outputs is derived from a single input rail and continuously adjusted to minimize the voltage drop (and power dissipation) across the channels. The brightness of each LED string is independently controlled with a 12 or 16 bit PWM dimming through the serial interface.

A programmable fault detection and management circuitry can be set to automatically disconnect faulty channels without the need for the host controller intervention.

The board has been designed as a reference application for medium/large LCD panel backlight drivers, but is suitable for any application involving several LEDs arranged in strings (e.g. advertisement panels, street signage, gaming, etc.).

Table 1 summarizes the main features of the STEVAL-ILL035V1 evaluation board.

Parameter	Conditions	Value
Minimum input voltage		12 V
Maximum input voltage		24 V
Output voltage		32.2 V ÷ 43.4 V
Output OVP threshold		48.6 V
Boost section switching	FSW pin connected to LDO3	600 kHz
frequency	FSW trimmer	200 kHz ÷ 1 MHz
Dimming frequency range		60 Hz ÷ 6 kHz
Minimum dimming on-time		10 µs
Output (LED) current		20 mA x 16 ch
Output current accuracy (respect to nominal value)	0.6 V ≤ VCHx ≤ 1 V,	±2% typ. (±3% max)
Maximum channel to channel output current mismatch	(ICHx = 20 mA)	±2% typ.

Table 1. STEVAL-ILL035V1 board specifications summary



1.1 STEVAL-ILL035V1 schematic







Figure 3. STM32 controller





Figure 4. Connector





Figure 5. JTAG adapter (separated PCB)

1.2 STEVAL-ILL035V1 bill of material (BOM)

Item	Reference	Description	Package	Value	Part number
1	CON1	20 pins male header SIL 90°			5-826631-0
2	CON3	Mini USB connector			6510-0516121
3	CON2	10x2 female connector 90°			89883-410LF
4	CON4	5x2 female connector			6233-10235321
5	C1,C2	Ceramic, 50 V, X7R, 20%	SMD 1206	4u7	GJ831CR71H475 KA12L
6	C3	Aluminium, 32V, 8mm		68u	32SEPF68M
7	C4,C5	Ceramic, 50 V, X7R, 20%	SMD 1206	4u7	GJ831CR71H475 KA12L
	C7,C8	Tantalum 50V		4u7	594D475X9050C
0	C6,C9			NC	2T

Table 2. Bill of material



ltem	Reference	Description	Package	Value	Part number	
9	C18			100p		
10	C11,C12,C13, C14, C38			1u		
11	C10,C21,C24, C25, C26 C27,C28,C29, C32, C33, C34,C35,C36, C37	Ceramic, 25V , X5R, 5%	SMD 0603	100n		
12	C15,C16,C19			NC		
13	C17			4n7		
14	C20			220n		
15	C23,C22	Tantalum, 10V	SMA	10u	T491A106K010A T	
16	C30,C31	Ceramic, 25V, NP0, 5%	SMD 0603	10p		
17	D1	Schottky 601/ 1A	SMA	STPS1L60A		
18	D2	Scholiky, ouv, TA	SWA	STPS1L60A	STESTLOOA	
19	D3	Red LED			KP-2012SRC- PRV	
20	D4	Blue LED			KP-2012PBC-A	
21	D5	Red LED	SMD 0805		KP-2012SRC- PRV	
22	D6	Yellow LED			KP-2012SYC	
23	D7					
24	D8	Red LED			KP-2012SRC- PRV	
25	D9	-				
26	F1	Fuse	SMD 1206	200mA	0466.200NR	
27	J1,J2,J3,J4,J5, J6,J7,J8,J9,J10, J11,J12	Test point	hole 1.2mm			
28	L1	custom_7x7	7x7mm	10u	PCMB062D- 100MS-11	
29	L2	Ferrite bead, 300Ω, 3A	SMD 0805	0R	7427-9203130	
30	PB1					
31	PB2	Buchbutton			430453031836	
32	PB3	FUSHDULLON				
33	PB4				434123025816	
34	Q1	Power MOSFET	SO8	STS5NF60	STS5NF60	

Table 2. Bill of material (continued)



Item	Reference	Description	Package	Value	Part number
35	R1			120k	
36	R2	Resistor, 1%, 0 125W	SMD 0603	3k3	
37	R3	0.12011		0R	
38	R4	Sensing resistor	SMD 1206	R050	RLT1632-4-R050- FNH-11
39	R5			1R	
40	R6			220k	
42	R16			30k	
43	R12,R21,R22, R23,R24, R25,R26			1k	
44	R13			60k	
45	R14	Resistor. 1%.		100k	
46	R15	0.125W	SMD 0603	68k	
47	R17			27k	
48	R18			680k	
49	R19			120k	
50	R27,R28,R29			100R	
51	R20			10k	
52	R32,R33			100k	
53	R30			330k	
54	R31			22k	
55	SW1			strip 3	
56	SW2			Strip 5	
57	SW3			tin-drop 3+1	
58	SW4	Jumper selector		tin-drop 3	
59	SW5				
60	SW6			tin-drop 2	
61	SW7			tin-drop 3	

Table 2. Bill of material (continued)



Item	Reference	Description	Package	Value	Part number
62	TP1,TP2,TP3, TP4,TP5,TP6, TP7,TP8,TP9, TP10,TP11, TP12,TP13, TP14,TP15, TP16,TP17, TP18,TP19, TP20,TP21, TP20,TP21, TP22,TP23, TP24,TP25, TP26,TP27, TP28,TP29, TP30,TP31,TP3 2	Test point (white)	hole 1mm		200-202
63	U1	LED driver	VFQFPN7x7_48	LED7708	LED7708
64	U2	3V3 Linear regulator	SOT-23	LK11233	LK112M33TR
65	U3	USB protector	SOTT-123-6L	USBUF02W6	USBUF02W6
66	U4	Microcontroller	LQFP-48	STM32F103C6T6	STM32F103C6T6
67	Y1	Crystal resonator	FQ7050B	8MHz	FQ7050B-8.000

 Table 2. Bill of material (continued)

1.3 STEVAL-ILL035V1 printed circuit board

Figure 6. STEVAL-ILL035V1 PCB top view







Figure 7. STEVAL-ILL035V1 PCB bottom view

1.4 Board connectors and switches

The STEVAL-ILL035V1 evaluation board has a set of connectors, test points and switches that makes easy interfacing it to the measurement equipment. The following tables summarize the function of each board terminal and test point.

Terminal	Description		
VIN	Input voltage, positive terminal		
VIN2	Second input voltage, positive terminal. The second input voltage id designed to supply the device from an input voltage lower than the main rail reducing the power consumption due to the internal linear regulator.		
GND	Reference ground		
CH1 CH16	Driver output		
SYNC	Boost converter synchronization output		
FSW	Switching frequency selection / synchronization input.		
GSSY	Grey scale synchronization output		
GSCK	Gray scale clock I/O		
XFLT	Fault signal, open drain output		
VBOOST	Boost regulator output voltage		

|--|



Test point	Description
LDO3	Internal 3.3 V linear regulator output
VDR	Gate driver supply
VFB	Output voltage feedback for the boost controller
COMP	Trans-conductance amplifier output
VSI	Serial interface (SI) core and digital I/O buffers supply input
LREN	3.3 V linear regulator enable
GSSY	Gray-Scale Synchronization output
DIN	Serial interface data input
DOUT	Serial interface data output
DCLK	Serial interface data clock
LE	Serial interface latch enable
GSCK	Grey-scale clock I/O
ЮК	Used for extended output voltage regulation in multi-device applications. Used by slave devices to request a higher output voltage to the master.
XVOK	Used for extended output voltage regulation in multi-device applications. Used by a slave devices to request an output voltage reduction to the master.
XOVF	Used for extended output voltage regulation and fault management in multi-device applications. It is used to inform slave devices that the maximum output voltage has been reached.
XMSK	This signal is used for extended output voltage regulation &fault management in multi-device applications. It is used to avoid incorrect fault detection by forcing slave devices to ignore LED-short detection during output voltage steering.
CH1,,CH16	Driver outputs



Switch	Function	Default position
SW1	This switch selects the supply rail for the LED7708. The power dissipation of the LED7708 can be reduced by providing a lower voltage at the VIN pin of the chip (VIN2 terminal). If the switch is in the default position, the supply rail is the same of the power section of the boost converter (VIN terminal).	Upper (dot)
SW2	This switch selects the digital interface supply voltage (VSI pin). In the default position the VSI is connected to the supply rail of the MCU, otherwise the VSI pin is connected to the LDO3 of the LED7708.	Upper (dot)
SW3	This multi-position switch is used, in conjunction with the VFB pin setting, to select the best output voltage swing for a given LED array.	Center and right pads connected (VMIN to GND)
SW4	This switch is used to connect the ISETL pin of the LED7708 to the R14 resistor (programmable low-level LED biasing current) or to LDO3 (default position, no low-level LED biasing current).	Center and right pads connected (dot)
SW5	This switch is used to connect the FSW pin of the LED7708 to LDO3 (default, 660kHz fixed the switching frequency) or to R15 (programmable switching frequency). When an external synchronization clock at the FSW terminal is provided, the central pad of the switch should be left floating.	Center and right pins connected (dot)
SW6	If this switch is closed the internal dimming oscillator is disabled and the GSCK pin becomes the clock input. If this switch is left open the dimming frequency is set by a resistor connected between FOSC pin to ground.	Closed
SW7	This switch is used to send back to the MCU the serial data output (DOUT) of the last device connected to the serial bus chain. When other boards are connected to the CON3 expansion connector, the center pad must be connected to the right one. If the board is used stand-alone, the default position (dot) must be selected.	Center and left pins connected (dot)

Table 5. STEVAL-ILL035V1	board switches	description



2 STEVAL-ILL035V1 control tool

The purpose of the STEVAL-ILL035V1 control tool is providing an easy way to understand and discover all the functionalities of LED7708. This section explains how to install the control tool software and how it is structured.

2.1 Control tool installation

To correctly install the control tool software the user has to follow the procedure suggested in the InstallShield Wizard. In the following screenshot is shown the first pop up window of the installation tool.

(LedDriver GUI7708 - InstallShield	d Wizard	1
		Welcome to the InstallShield Wizard for LedDriver GUI7708 The InstallShield Wizard will install LedDriver GUI7708 on your computer. To continue, click Next.	
		< Back Next > Cancel	

Figure 8. Initial install shield

At the end of the control tool installation, the installation software searches all the necessary drivers.

If the required drivers are not present onto the PC, the driver installation wizard is automatically launched. *Figure 8* shows a screenshot of the related popup window.



ſ	Device Driver Installation Wizard	
	Welcome to the Device Driver Installation Wizard! This wizard helps you install the software drivers that some computers devices need in order to work.	
	To continue, click Next.	

Figure 9. Device drivers installation window

At the end of the installation procedure, the STMicroelectronics folder should appear into the "Program Files(x86)" folder in the PC's hard disk. The folder contains the following sub-folders:

- 1. "firmware" folder. In this folder is saved all the firmware downloaded on the microcontroller placed on STEVAL-ILL035V1 board.
- 2. "st vcp driver". In this folder is saved the Virtual-COM driver.
- 3. "LED_SDK.dll" and "PL_001.dll", the implemented library used for the correct operation of the control tool.
- 4. "LEDDriverGUI.exe", the executable file of the graphic user interface.

2.2 Control tool features

With a double click on the executable file "LEDDriverGUI", the following window should appear.





Figure 10. LED7708 control tool main window

In the following paragraphs will be described accurately all the components of the control tool:

- Tabs
- Shortcuts
- Settings, boost output, grey scale clock groups
- Continuous status reading
- Write and read control registers groups
- Channel status and channels control groups

2.2.1 Control tool tabs

On the control tool are presents three different tabs:

- 1. "File"
- 2. "Mode"
- 3. "Help"

The first tab, "File", like shown in the *Figure 11*, allows connecting and disconnecting the STEVAL-ILL035V1 to the PC.

It allows also, with the command "Exit", to close the GUI.



Figure 11. File tab

ST LED7708 Evaluation Tool GUI
File Mode Help Connect Disconnect Exit

The second tab, "Mode", like shown in the *Figure 12*, allows selecting the demo mode.

Figure 12. Mode tab

ST LEE	07708 Evalu	uation Tool GUI	10 (Ball)	
<u>F</u> ile	Mode	<u>H</u> elp		
	Der	mo Mode		

Selecting the "demo mode" tabs appear a new window, reported in the following picture.

Figure 13. Demo mode GUI



Pressing one of the buttons in the "play demo" group and then the "start" button the user activates one of the demos implemented to show all the functionalities of the device.

Pressing the "enable" button the user activates the automatically controls, realized on the MCU, of the open and short circuits on the LED chains.

The last tab, "help", opens the pop up window "about box" on which are described all information related to the software and firmware development.



Figure 14. About popup box

2.2.2 Shortcuts

On the control tool are presents three shortcuts:

- 1. "Connect button"
- 2. "Disconnect button"
- 3. "Demo mode"

The first button, shown in the following figure, allows connecting the PC to the STM32 placed on the board.

Figure 15. "Connect button" shortcut

ST LED7708 Evaluation Tool GUI	And in case of	Autor Autor Autor	Autority Autority	
Mode Help				
LED 7708				

The second button, shown in the following figure, allows disconnecting the PC to the STM32 placed on the board.

Figure 16. "Unconnect button" shortcut

C ST LED7/08 Evaluation Tool GUI	Autor Autor Autor Autor Autor
File Made Help	J

The last button, shown in the following figure, allows opening the demo page of the control tool.

Figure 17.	"Demo	mode"	shortcut
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2.2.3 "Settings" group

In the "setting" groups, shown in the following figure, are implemented two different buttons:



- 1. "LREN"
- 2. "Default"

				All March 1
Mode <u>H</u> elp				
stings Bo	St Output Gray Scale Cloc	Source (MCL)	Status Reading DEVCFG1 CHSTA CHSEL	GSLAT
REN 1 Default VB	sost 32.8 V Frequency	8.00 MHz		
REN 1 Default VB	oost 32.8 V Gray Scale Cloo ✓ Edemai Frequency	Source (MCU) 8:00 MHz	DEVCFG1 CHSTA CHSEL	G

The LREN pin of the LED7708 enables the 3.3 V linear regulator when high. This pin is connected to an I/O pin of the MCU and can be directly controlled by acting on the corresponding pushbutton of the GUI:

- Setting "LREN" button to 0 the device is turned off.
- Setting "LREN" button to 1 the device is turned on.

Pressing the "default" button, the MCU turns-on the LED7708 and writes the configurations register (DEVCFG0, DEVCFG1, GSLAT and CHSEL) with the default values reported in the following tables.

Table 6. DEVORGO configuration register and default setting						
Bit	Position	Attribute	Description			
DEN	0	R/W	1	Device ON		
EDMI	1	R	0	Valid data on CHSTA		
OVFW	2	R	0	Regulation DAC in range		
OTAF	3	R	0	Die temp < 120 °C		
OCAD	4	R/W	1	Open channels auto-disconnected		
SCAD	5	R/W	1	Shorted channels auto-disconnected		
CFP	6	R	0	no protection occurred		
RWAS	7	R/W	0	300mV regulation window		
DTS0	8	R/W	1	LED short detection threshold		
DTS1	9	R/W	0	LED short detection threshold		
GSME	10	R/W	1	Gray-scale dimming mode		
CRS	11	R/W	0	lower current range (20 mA-45 mA)		
OVRS	12	R	0	Output voltage not optimized		
OVRE	13	R/W	1	Output voltage regulation enabled		
SDMS	14	R/W	0	No slaves devices		
DEST	15	R/W	0	FIFO loaded into DEVCFG0		

DEVCFG0 configuration register

Table 6. DEVCFG0 configuration register and default setting



DEVCG1	configuration	register
--------	---------------	----------

Table 7. DEVCFG1 configuration register and default setting

Bit	Position	Attribute		Description
ADJ0	0	R/W	0	Current gain adjust
ADJ1	1	R/W	0	Current gain adjust
ADJ2	2	R/W	0	Current gain adjust
ADJ3	3	R/W	0	Current gain adjust
ADJ4	4	R/W	0	Current gain adjust
ADJ5	5	R/W	0	Current gain adjust
CGRS	6	R/W	1	Range 2 selected
LAT16	7	R/W	0	Dimming latency
LAT17	8	R/W	0	Dimming latency
BDFS	9	R/W	0	16 x16 bit format brightness
BRLS	10	R/W	0	16 bit resolution
DTIN	11	R/W	0	Dimming cycle on phase first
DASS	12	R/W	0	Brightness data immediately updated at the falling edge of LE
DSYS	13	R/W	0	GSSY pin is pulse output
CSRD	14	R/W	0	Continuous status reading disabled
DEST	15	R/W	1	FIFO loaded into DEVCFG1



Bit	Position	Attribute	Description			
DEN	0	R/W	1	Device ON		
EDMI	1	R	0	Valid data on CHSTA		
OVFW	2	R	0	Regulation DAC in range		
OTAF	3	R	0	Die temp < 120 °C		
OCAD	4	R/W	1	Open channels auto-disconnected		
SCAD	5	R/W	1	Shorted channels auto-disconnected		
CFP	6	R	0	no protection occurred		
RWAS	7	R/W	0	300mV regulation window		
DTS0	8	R/W	1	LED short detection threshold		
DTS1	9	R/W	0	LED short detection threshold		
GSME	10	R/W	1	Gray-scale dimming mode		
CRS	11	R/W	0	lower current range (20 mA-45 mA)		
OVRS	12	R	0	Output voltage not optimized		
OVRE	13	R/W	1	Output voltage regulation enabled		
SDMS	14	R/W	0	No slaves devices		
DEST	15	R/W	0	FIFO loaded into DEVCFG0		

GSLAT configuration register

Table 8. GSLAT configuration and default setting

CHSEL configuration register

Bit	Position	Attribute		Description
LAT0	0	R/W	0	Dimming latency
LAT1	1	R/W	0	Dimming latency
LAT2	2	R/W	0	Dimming latency
LAT3	3	R/W	0	Dimming latency
LAT4	4	R/W	0	Dimming latency
LAT5	5	R/W	0	Dimming latency
LAT6	6	R/W	0	Dimming latency
LAT7	7	R/W	0	Dimming latency
LAT8	8	R/W	0	Dimming latency
LAT9	9	R/W	0	Dimming latency
LAT10	10	R/W	0	Dimming latency
LAT11	11	R/W	0	Dimming latency
LAT12	12	R/W	0	Dimming latency

 Table 9. CHSEL configuration register and default setting



	Table 5. Office Configuration register and default setting						
Bit	Position	Attribute	Description				
LAT13	13	R/W	0	Dimming latency			
LAT14	14	R/W	0	Dimming latency			
LAT15	15	R/W	0	Dimming latency			

Table 9. CHSEL configuration register and default setting

Note: For a more detailed description of the configuration registers and the function of each bit, refer to the device datasheet.

2.2.4 "Boost output" group

The "Boost output" group monitors the output voltage of the device. The output voltage is cyclically sampled by the MCU and its value is shown in the related box of the GUI.



Figure 19. "Boost output group"

2.2.5 "Gray scale clock" group

In the "gray scale clock" group it is possible to define the source of the high-frequency dimming clock, i.e. the internal oscillator of the LED7708 (see FOSC pin) or a dedicated pin of the MCU (external source).

By default the gray scale clock is provided by the MCU and the FOSC pin must bet accordingly (i.e. SW6 must be closed). From the drop-down menu the user could choose the dimming clock frequency.



Figure 20. "Grey scale clock group"

In case the internal oscillator of the LED7708 is used, the SW6 switch must be opened and the R16 resistor calculated for the desired frequency:

Equation 1

 $f_{GSCK} = \frac{K_{OSC}}{R_{FOSC}} = \frac{4 \times 10^{11}}{30000} = 13.3 MHz$

Where R_{FOSC} =R16 in the STEVAL-ILL035V1 evaluation board.



Of course all switches and/or components modifications must be performed after removing all the power supply rails.

2.2.6 "Continuous status reading" group

In the "continuous status reading" group is shown the content of the internal registers. The content of the DEVCFG0, DEVCFG1, CHSEL, CHSTA and GSLAT is automatically loaded into the shift register of the serial interface after the brightness data has been moved to the buffer. This feature has to be activated through the CSR bit of the DEVCFG0 register and operates only with 1x192-bit and 1x256 bit data formats (see the LED77068 datasheet for more details).

The commands necessary to set that kinds of data format will be analyzed in the followings paragraphs.

In the following picture is shown the results of continuous status reading. As it's easy to see the content of the internal registers is reported in the white boxes.



Figure 21. "Continuos status reading group"

2.2.7 "Write control registers" group

The "write controls registers" group has been implemented to have a very easy interface to change the content of the internal registers of the LED7708.

As highlighted in *Figure 22*, three rows of buttons belong to this group: DEVCFG0, DEVCFG1 and GSLAT registers. Once the register to be modified has been select through the selection tag on the left, the content can be changed by acting on ach single bit. The hexadecimal value is automatically updated. When the final value has been fixed, it can be sent to the destination register by clicking on the "write" pushbutton.

As visible in *Figure 22*, there are three different colors for the buttons: grey, light blue and white. Pushbuttons white highlighted are read only type and cannot be modified.



Figure 22. "Write control registers group"



On the left of button lines there are three white boxes. On the white boxes there is the hexadecimal conversion of internal register bit status.

In order to prevent undesired corruption of critical bits during operation, the CRS & SDMS bits of the DEVCFG0 register and the DSYS bit of the DEVCFG1 register are locked when the DEN bit of the DEVCFG0 register is asserted. The GUI reminds this by disabling the related buttons when the DEN bit is asserted.

2.2.8 "Read control registers" group

This group consists of two rows dedicated to the reading of the DEVCFG0 and DEVCFG1 registers. Once one of the two has been selected through the selection tag on the left, its content is read and shown in the right side after the "read" push button has been pressed. The hexadecimal value is also provided.



Figure 24 shows the content of the two registers after both have been read. It can be noticed that the read-only bits are red or green highlighted to easily identify abnormal operation or faulty conditions. The OVRS bit of the DEVCFG0 register, in particular, is red-highlighted when the output voltage is being regulated: this is a normal behavior as the output voltage is continuously adjusted if the OVRE is high. Therefore subsequent readings of the DEVCFG0 could show a different status of the OVRS bit because of a different sampled value. The status of the EDME read-only bit depends on the value of the OVRS one and this dependence is remarked by yellow-highlighting the former.





2.2.9 "Channels status" group

This group is dedicated to the reading of the channels' status.

Each bit of this register shows the status of the corresponding channel. After the error detection sequence takes place, the channels which have an excessive voltage drop (LED short circuit) or that are unable to regulate the nominal current (open channels) are tagged as faulty and the related CHSTA bits are asserted.



Figure 25. "Channel status group" showing three channels subject to faulty condition



The bit status has the following meaning;

- 1 \rightarrow The corresponding LED channel is active (green-highlighted)
- $0 \rightarrow A$ faulty condition has been detected (red-highlighted)

To refresh the bit status of the LED channels the user should click the "Read" pushbutton. Faulty channels can still be active or automatically disabled according to the OCAD & SCAD bits of the DEVCFG1 register.

Once a bit of the CHSTA has been asserted, it still remains high also in case the faulty condition has been removed and the related channel operates normally (no autodisconnection enabled). To clear the CHSTA register the DEN bit of the DEVCFG0 register has to be toggled.

Because of the active channels are selected through the CHSEL register, the disabled channels are gray-highlighted to remind the user the active ones.

2.2.10 "Channels control" group

This group, as shown in *Figure 26*, consists of 16 check boxes, 16 sliders and some pushbuttons. The check boxes directly act on the CHSEL register, allowing the user to select the active channels. To quickly assert or clear the full CHSEL register, the "All-on/off" toggling pushbutton is provided.

Moving up and down the sliders the user can modify the brightness of each channel by changing the dimming PWM duty cycle. Every time the position of a slider is modified, the content of the brightness registers is updated by means of a sequence of write operations over the serial interface.



Figure 26. "Channels contro group"

At the bottom of every slider there is a text box showing the PWM duty cycle in percentage.

To provide the user a quick way to set all the channels to the same brightness, a scroll down set of predefined brightness levels is available.



3 Getting started with STEVAL-ILL035V1 evaluation board

In the following section is described the recommended equipment to get started with the STEVAL-ILL035V1 board and to analyze all the LED7708 features by using the graphic user interface.

Figure 27 shows how to connect the STEVAL-ILL035V1 evaluation board to the DC power supply and the LED strings.



Figure 27. Basic connection of the STEVAL-ILL035V1

3.1 Recommended equipment

The on-board MCU section is capable of controlling all the functionalities of the LED7708 by applying the required signals and reading back some voltages and signals.

For a quick evaluation of the LED7708, just a DC power supply and a PC with USB connectivity are needed. For a more detailed analysis of the LED7708 performance, conventional lab equipment (digital multi meters, oscilloscope, etc.) is recommended.

3.2 Configuration

The STEVAL-ILL035V1 evaluation board allows the user to select different options by acting on a set of jumpers and switches (see *Table 6*).

In the following figure are shown the switches configuration that should be obtained on the STEVAL-ILL035V1 evaluation board.





Figure 28. Default switches configuration

3.3 Quick startup

The following step by step sequences are provided as a guideline to quickly connect the STEVAL-ILL035V1 board to the PC and evaluate the LED7708 performance.

- 1. Working in a ESD-protected environment is highly recommended. Check all wrist straps and mat earth connections before handling the STEVAL-ILL035V1 evaluation board.
- 2. Check all the switches are set according to *Figure 28*.
- 3. Connect a 12 V±10% (3A current capability) power supply to the STEVAL-ILL035V1 evaluation board (VIN & GND terminals).
- 4. Connect a suitable set of LED strings (e.g. 16 x 10 white-LEDs capable of handling at least 20 mA) between the VBOOST & CHx terminals of the CON1 connector. In case LEDs to be driven with more than 85 mA, the outputs of the LED7708 can be connected in parallel (max. 8 channels in parallel for 2 outputs).
- 5. Connect the STEVAL-ILL035V1 board to the PC by using a USB cable. The yellow "LINK" LED should light after a while: if not, maybe the STM32 virtual COM port driver has to be installed on the PC.
- 6. Launch the STEVAL-ILL035V1 control tool (*Figure 29*).





7. Click on the "Connect" button.

Figure 30. Connect button



8. A new window "Serial port selection" pop-up appears. Select from the drop-down menu the serial port on which the evaluation board is connected. Once selected the correct serial port, press the "Select" button.





9. If the STEVAL-ILL035V1 demo-board id found at the selected COM port, the message shown in *Figure 32* should appear. Press "OK" button to proceed.





Figure 32. Successful connection message

If the board is not found at the specified COM port, the message of *Figure 33* is shown. In this case it is necessary press "OK" button, disconnect the USB cable from the PC, reconnect it and then restart the procedure (go back to point 7).





10. Turn-on the power supply: the value of the input voltage appears in the "Vboost" textbox because of the fly wheeling diode of the boost converter. Press the "Default" button (*Figure 34*) to configure the LED7708 as per default settings.





As soon as the device is turned-on, the output voltage "Vboost" increases to the correct output voltage.

11. To quickly set all channels to the same brightness, select the full-scale (100%) value in the drop-down menu of the "Channels control" panel.



Figure 35. Channels control panel



As a result all the connected LED strings are powered up and supplied with the maximum current that is selected by the R13 resistor. To set a different brightness for each channel, act on the sliders.



4 Step by step design

The following section focuses on the step by step design of an application example. A dedicated design spread sheet is available for quickly calculate the value of the external components for a given application. In this section the basic calculations are shown, while some results are directly extracted from the spread sheet in order to keep simple the step by step design procedure.





4.1 Application example

The following specifications refer to a typical application where the LED7708 is asked to drive 10 strings of 20, 20 mA rated white LEDs starting from a single 12V supply rail:



- 1. Input voltage range: VIN,min = 10.8V, VOUT,MAX = 13.2 V.
- 2. Number of used channels: NCH = 16.
- 3. Number of LEDs for each string: NLED = 10.
- 4. Channel current during the on-phase: ICH,on = 20 mA.
- 5. Channel current during the off-phase: ICH, off = 5 μ A.
- 6. Minimum LED forward voltage: VF,min = 2.8 V.
- 7. Maximum LED forward voltage: VF,MAX = 3.6 V.
- 8. Operating ambient temperature: $TA = 50 \degree C$.
- 9. Minimum LED operating temperature: TLED,min = -20 °C.
- 10. Maximum LED operating temperature: TLED,MAX = +100 °C.
- 11. Boost converter switching frequency: fsw = 600 kHz.
- 12. Selected dimming frequency: fDIM = 120 Hz.
- 13. Selected dimming resolution (12 or 16-bit): N = 16.
- 14. Selected data format (16x16-bit, 1x192-bit or 1x256-bit): 16x16-bit

4.2 Components selection

The step by step design of an LED7708 base application is quite simple. One of the points requiring particular attention is the calculation of the output voltage swing, which depends on the characteristics of the LEDs and their operating conditions.

4.2.1 Setting the VMIN pin and the output divider

The output voltage swing is determined by the VMIN pin setting and the output divider connected to the VFB pin. Because of the output voltage basically depends on the forward voltage of the LEDs, two factors have to be taken into account. The first is the spread of the nominal forward voltage; the second is the dependence of the former on the temperature. In practice a sort of averaging naturally occurs when connecting several LEDs in series, but a robust design should consider the worst cases. Therefore, the minimum expected output voltage is given by the following equation:

Equation 2

$$V_{LED,min} = N_{LED} \cdot V_{F,min} + \frac{dV_F}{dT} \cdot (T_A + T_{LED,MAX}) + V_{CH,MASTER} = 27.9 V$$

Where $dV_F/dT = -0.006$ V/K, is the gradient that considers the voltage variation due to the temperature and VCH,MASTER = 0.6V, is the voltage drop on the current generator present on every LED channels.

Similarly, the expected maximum output voltage is given by:

Equation 3

$$V_{LED,MAX} = N_{LED} \cdot V_{F,MAX} + \frac{dV_F}{dT} \cdot \left(T_A + T_{LED,MIN}\right) + V_{CH,MASTER} = 36.6 V$$

The target of this design step is setting the output divider and the resistor at the VMIN pin to match, with some margin, the output voltage swing achievable by the LED7708 to the actual one required by the LED strings.

The mean output voltage is simply calculated as



Equation 4

 $V_{LED,MEAN} = \frac{V_{OUT,MAX} + V_{OUT,min}}{2} = 32.2V$

And can be used to calculate the output divider ratio:

Equation 5

 $K_{DIV,calc} = \frac{V_{FB,MID}}{V_{LED,MEAN}}$

Where V_{FB,MID} is the half scale reference voltage of the LED7708, i.e. the middle level of the internal DAC of the output regulation circuitry (refer to the datasheet for more details). The setting of the VMIN pin determines the OVP threshold (V_{FB,OVP}), the reference voltage swing (V_{FB,min} and V_{FB,MAX}) and the value of the half scale reference V_{FB,MID}:

Table 10. Internal reference voltage swing and OVP threshold versus VMIN pin	setting
--	---------

VMIN pin setting	GND	VCC	220 kΩ	Float
V _{FB,OVP} (V)	1.300	1.132	1.011	0.795
V _{FB,MAX} (V)	1.161	0.992	0.872	0.655
V _{FB,MID} (V)	1.010	0.841	0.721	0.504
V _{FB,min} (V)	0.861	0.692	0.572	0.355

Depending on the setting of the VMIN pin, the output divider ratio can assume four values (*Equation 5*).

Table 11	. Output volt	age divider rat	tio versus	VMIN pin setting
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VMIN pin setting	GND	VCC	220 kΩ	Float
K _{DIV,CALC}	0.0314	0.0261	0.0224	0.0156

Each of the above calculated output divider ratios leads to different output voltage swings and OVP levels at the output (*Equation 6* and *Equation 7*).

Equation 6

 $\Delta V_{OUT} = \frac{V_{FB,MAX} - V_{FB,min}}{K_{DIV,calc}}$

Equation 7

 $V_{OUT,OVP} = \frac{V_{FB,OVP}}{K_{DIV,calc}}$

Table 12 summarizes all the possible output voltage swings and OVP level as a function of the VMIN pin setting:

Table 12. OVP	level and out	put voltage	swing versus	VMIN pin setting

VMIN pin setting	GND	vcc	220 kΩ	Float
V _{OUT,OVP} (V)	41.4	43.4	45.1	50.9
V _{OUT,MAX} (V)	36.9	38.0	38.9	41.9



	Table 12. OVP level and output voltage swing versus vinin pin setting						
VMIN pin setting	GND	vcc	220 kΩ	Float			
V _{OUT,min} (V)	27.4	26.5	25.5	22.8			
ΔV _{OUT} (V)	9.5	11.5	13.4	19.1			

Table 12. OVP level and output voltage swing versus visiting prin setting	Table 12.	OVP level	and output	t voltage	swing ve	ersus VMIN	pin setting
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The best choice for the VMIN pin configuration is the one that leads to an output voltage swing containing the V_{LED,MAX} - V_{LED,min} one plus a small margin. As visible in *Figure 37*, connecting the VMIN pin to GND the condition is satisfied.



Figure 37. Output voltage threshold for ideal ratio

Summarizing this design step, the VMIN pin has to be connected to GND and the theoretical output divider ratio is given by *Equation 8* (or *Table 11*):

Equation 8

 $K_{DIV,calc} = 0.0314$

The high-side resistor should drain a negligible current from the output: a value in the order of few hundreds of kilo ohms is often the proper choice:

Equation 9

 $R_{DIV,HS} = 511 \ k\Omega$

The value of the low side resistor is then calculated as:

Equation 10

 $R_{DIV,LS} = R_{DIV,HS} \cdot \frac{\kappa_{DIV,calc}}{1 - \kappa_{DIV,calc}} = 511 \ k\Omega \cdot \frac{0.0314}{1 - 0.0314} = 16.56 \ k\Omega$

The closest available value (E96 series) is:

Equation 11

 $R_{DIV,LS} = 16 k\Omega$

At this point the output divider ratio should be recalculated and the actual output voltage swing verified.



Equation 12

 $K_{DIV} = \frac{R_{DIV,LS}}{R_{DIV,LS} + R_{DIV,HS}} = 0.0304$

Equation 13

 $V_{OUT,MAX} = \frac{V_{FB,MAX}}{K_{DIV}} = \frac{1.161V}{0.0304} = 38.2V$

Equation 14

 $V_{OUT,\min} = \frac{V_{FB,min}}{K_{DIV}} = \frac{0.361V}{0.0304} = 28.3V$

Comparing the results of Equation 13 and Equation 14 to the ones of Equation 2 and *Equation 3*, the actual minimum output voltage is slightly (about 300mV) higher than required.

A possible solution could be selecting a different value for R_{DIVLS} or, alternatively, a different setting for the VMIN pin.

Considering the negligible difference and the fact that all the calculations are based on worst case conditions, the calculated values for R_{DIV.HS} and R_{DIV.LS}, as well as the VMIN pin setting, are kept.

4.2.2 Switching frequency setting

The desired switching frequency it is set by the resistor connected at the FSW pin:

Equation 15

 $R_{fSW} = \frac{K_{fSW}}{f_{SW}} = \frac{5 \cdot 10^{10} [Hz] [\Omega]}{600 \cdot 10^3 [Hz]} = 83.3 \ k\Omega$

4.2.3 **Dimming oscillator setting**

The gray scale clock generated by the internal high frequency oscillator or externally provided depends on the selected resolution (N) for the brightness registers:

Equation 16

 $f_{GSCK} = f_{DIM} \cdot 2^{N} = 120 \ Hz \cdot 2^{16} = 7.86 \ MHz$

The resistor at the FOSC pin is then calculated according to *Equation 16*:

Equation 17

 $R_{FOSC} = \frac{\kappa_{OSC}}{f_{GSCK}} = \frac{4 \cdot 10^{11} [Hz] [\Omega]}{7.86 \cdot 10^6 [Hz]} = 50.9 \ k\Omega$

4.2.4 Channels current setting

The current sunk by each channel during the on time of the dimming is set through the resistor at the ISETH pin:

Equation 18

 $R_{ISETH} = \frac{K_{ISETH}}{I_{CH,on}} = \frac{1200[V]}{20 \cdot 10^{-3}[A]} = 60 \ k\Omega$

Similarly, the current sunk during the off time depends on the resistor at the ISETL pin:



Equation 19

 $R_{ISETL} = \frac{K_{ISETL}}{I_{CH,off}} = \frac{4[V]}{5 \cdot 10^{-6}[A]} = 800 \ k\Omega$

The purpose of a small biasing current during the off time of the dimming is keeping the forward voltage of the LEDs to a controlled value in order to avoid excessive drops across the channels when an output voltage higher than 36 V is used. If this biasing current is not needed, the ISETL pin must be set high (ISETL to LDO3).

4.2.5 Inductor selection

The power inductor of the boost converter is typically selected in order to ensure Continuous Conduction Mode (CCM) over the entire operating range (i.e. input and output voltage ranges) of the LED driver. CCM operation is inherently less noisy and preferable whenever possible.

The switching duty-cycle in CCM is defined as:

Equation 20

 $D_{CCM} = 1 - \frac{V_{IN}}{V_{OUT}}$

And the inductor value for DCM to CCM boundary operation is given by:

Equation 21

 $L_{min,CCM} = \frac{\frac{V_{OUT} \cdot D_{CCM} \cdot (1 - D_{CCM})^2}{I_{OUT}}}{2 \cdot f_{SW}}$

The following table summarizes the operating corner conditions and the minimum inductance value for CCM operation.

	······ ·······························							
V _{IN}	10.80	10.80	13.20	13.20	12.00	V		
I _{OUT}	0.32	0.32	0.32	0.32	0.32	А		
V _{OUT}	28.35	38.23	28.35	38.23	33.25	V		
D _{CCM}	0.62	0.72	0.53	0.65	0.64			
L _{min,CCM}	6.63	5.70	8.55	7.77	7.21	μH		

Table 13. Operating conditions corner table

The inductor is therefore selected to be:

Equation 22

 $L > \max(L_{min,CCM}) = 8.55 \ \mu H$

The selected value for the inductor is L=10 μ H.

After the inductance value has been fixed, the suitable part must be selected taking into account the RMS and the peak currents in the worst-case.

The average current flowing through the inductor is given by:

Equation 23

 $I_{L,AVG} = \eta \cdot \frac{V_{OUT,MAX} \cdot I_{OUT}}{V_{IN,min}} = 1.08 A$



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Where:

- η=0.95 is the estimate d efficiency;
- $I_{OUT} = N_{CH} \cdot I_{CH,on} = 0.32$ A is the maximum output current;

The inductor current ripple is given by:

Equation 24

 $\Delta I_L = \frac{V_{IN,min}}{L} \cdot D_{MAX} \cdot T_{SW} = 1.29 A$

Where D_{MAX} = 0.72 is the switching duty cycle estimated for the minimum input and maximum value of output voltage.

The maximum value of the current in the coil is given by:

Equation 25

 $I_{L,pk} = I_{L,AVG} + \frac{\Delta I_L}{2} = 1.72 A$

While the RMS value of current in the coil is given by:

Equation 26

$$I_{L,RMS} = \sqrt{\frac{1}{3} \left(\left(I_{L,AVG} + \frac{\Delta I_L}{2} \right)^2 + \left(I_{L,AVG} + \frac{\Delta I_L}{2} \right) \left(I_{L,AVG} - \frac{\Delta I_L}{2} \right) + \left(I_{L,AVG} - \frac{\Delta I_L}{2} \right)^2 \right)} = 1.14 \text{ A}$$

For this application example the PCMB062D-100MS inductor has been selected. The characteristics of the inductor are resumed in the following table.

Parameter	Symbol	Value	Unit
Nominal inductance	L	10	μH
Coil DC-resistance	R _{DC,L}	0.101	Ω
Saturation current	I _{L,SAT}	2.5	А
Max RMS current (40 °C temp rise)	I _{L,RMS}	3.1	А

Table 14. Inductor characteristics

4.2.6 Selecting the output capacitor

The selection of the output capacitor is based on the maximum voltage ripple residual allowed at the output and the RMS current.

The LED7708 regulates the output voltage of the boost converter by means of an internal DAC whose output is used as 128 steps reference voltage (*Equation 27*).

Equation 27

 $V_{STEP} = \frac{v_{out, MAX} - v_{out, MIN}}{128} = \frac{(38.2V - 28.3V)}{128} = 77mV$

A good practice is keeping the switching ripple residual to a fraction of the step amplitude:

Equation 28

 $\Delta V_{OUT,ripple} \leq \frac{v_{STEP}}{5} \cong 15 \; \mathrm{mV}$

The minimum capacitance value for the output capacitor is therefore:



Equation 29

 $C_{OUT} > \frac{I_{OUT} \cdot (1 - D_{MIN})}{f_{SW} \cdot 2 \cdot \Delta V_{OUT, ripple}} = 8 \, \mu F$

A pair of 4.7 μ F capacitors is selected for this application example. When MLCCs are used, the effect of the biasing voltage has to be taken into account: the actual capacitance could be significantly lower than the nominal value depending on the dielectric type (Y5V type is not recommended).

The RMS current that flow through the output capacitor is given by:

Equation 30

$$I_{COUT,RMS} = N_{CH} \cdot I_{CH,on} \sqrt{\frac{D_{MAX}}{(1 - D_{MAX})} + \frac{D_{MAX}}{12}} \sqrt{((1 - D_{MAX})\frac{V_{OUT,MAX}}{I_{OUT} \cdot L \cdot f_{SW}})} = 0.52 A$$

The characteristics of the selected capacitors Murata part, GJ831CR71H475KA12L, are shown is *Table 15*.

Parameter	Symbol	Value	Unit
Nominal capacitance	C _{OUT}	4.7	μF
Capacitance tolerance		± 10%	
Rated voltage		50	V
Equivalent series resistor	R _{ESR,COUT}	5	mΩ
Dielectric type		X7R	

Table 15. Output capacitor characteristics

4.2.7 Selecting the input capacitor

To select the value of the input capacitor it is necessary select the maximum ripple allowed on the input voltage.

An acceptable value of the ripple could be:

Equation 31

 $\Delta V_{IN,ripple} < 0.100 \, V_{PP}$

The minimum value of the input capacitor is given by:

Equation 32

$$C_{IN,min} > \Delta I_L \cdot \left(\frac{D_{MAX}}{f_{SW} \cdot 2 \cdot \Delta V_{IN,ripple}}\right) = 7.7 \ \mu F$$

The RMS current that flow through the output capacitor is given by:

Equation 33

$$I_{CIN,RMS} = \frac{N_{CH} \cdot I_{CH,on}}{(1 - D_{min})} \cdot \frac{\frac{(V_{OUT,MAX} + 0.6) \cdot D_{min} \cdot (1 - D_{min})^2}{I_{OUT} \cdot f_{SW} \cdot L}}{\sqrt{12}} = 0.46 \, A$$

Where Dmin is the minimum duty cycle obtained for VIN,MAX and VOUT,min.

For this application example a couple of GJ831CR71H475KA12L capacitors has been selected (table 16).



Parameter	Symbol	Value	Unit
Nominal capacitance	C _{in}	4.7	μF
Capacitance tolerance		± 10%	
Equivalent series resistor	R _{ESR,Cin}	5	mΩ
Rated voltage		50	V
Dielectric type		X7R	

Table 16. Capacitor characteristics

4.2.8 Selecting the power switch

The selection of the power MOSFET of the boost converter must consider the maximum peak and RMS current, the maximum drain-source voltage and the minimization of the power losses. The peak current has already been calculated for the inductor at the end of the charging phase of each switching cycle (t_{ON}).

While the RMS current is calculated as:

Equation 34

$$I_{MOS,RMS} = \frac{N_{CH} \cdot I_{LED,on}}{(1 - D_{MAX})} \cdot \sqrt{\left(D_{MAX} \cdot \left(1 + \frac{\left(\frac{(V_{OUT,MAX} + 0.5) \cdot D_{MAX} \cdot (1 - D_{MAX})}{l_{OUT} \cdot f_{SW} \cdot L}\right)^2}{12}\right)} = 1.48 A$$

Of course the selected MOSFET must be capable of sustaining the peak current (*Equation* 25) and the maximum drain source voltage (i.e. the output one) plus a certain amount of margin for safe operation. Considering a 30%-40% margin above the maximum output voltage, a 60 V rated, 3 A MOSFET is a good choice.

Another point to be taken into account is the maximum power dissipation allowed on the power switch, i.e. its contribution to the overall efficiency. Parts showing a lower on-resistance ($R_{DS,ON}$) of course lead to a better efficiency, although a trade off between conduction and switching losses should be found (lower $R_{DS,ON}$ usually means bigger diesize and gate capacitance).

For this application example the STS5NF60L switch has been selected. The characteristics of the power switch are resumed in the following table.

Parameter	Symbol	Value	Unit
Max drain source voltage	V _{DS,MAX}	60	V
Rise time	t _{RISE}	13	ns
Fall time	t _{FALL}	10	ns
Drain source on resistance (@Tj= 25 °C)	R _{DS,ON}	45	mΩ
Total gate charge	Qg	17	nC

Table 17. Power MOSFET characteristics



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4.2.9 Selecting the sensing resistor

The sensing resistor in series with the source of the power switch of the boost converter provides a measure of the inductor peak current to the regulation loop. At the same time the voltage drop across this resistor is compared to a fixed threshold to implement the over current protection (OCP) for the power MOSFET.

In order to get a reasonable signal/noise ratio on the peak current information, a minimum value of about 25 mV (peak) has to be ensured at the CSNS pin in all the operating conditions.

A minimum value of the sensing resistor is then established as:

Equation 35

 $R_{SNS,min} > \frac{25mV}{I_{L,pk}} = 16 \text{ m}\Omega$

Therefore a suitable value for the sensing resistor could be R_{SNS} =25 m Ω .

4.2.10 Selecting the power diode

The average value of the current flowing throw the diode is equal to the average current on the LED channels.

The peak value of the current in the diode is equal to the peak current in the inductor.

For this application example the STPS1L60 diode has been selected. The characteristics of the inductor are resumed in the following table.

Parameter	Symbol	Value	Unit
Repetive peak reverse voltage	V _{RRM}	60	V
Average forward current	t _{F(AVG)}	1	А
Forward voltage drop	V _F (@Tj= 100 °C)	0.56	V

Table 18. Switch characteristics

4.2.11 Setting the slope compensation resistor

The resistor connected to the SLOPE pin sets the proper amount of slope compensation to avoid sub-harmonic instability that may occur when the switching duty-cycle is above 50%. In practice the compensation signal is not a simple ramp and a quick formula cannot be invoked for the design of this resistor. The amount of slope compensation that should be achieved through the RSLOPE resistor is given by:

Equation 36

 $S_{E,min} = \left| R_{SNS} \cdot \frac{V_{IN,min} - V_{OUT,MAX}}{L} \cdot \left(1 - \frac{0.18}{D_{MAX}} \right) \right| \cdot K_{SF} = 6.68 \cdot 10^4 \text{ A/s}$

Where K_{SF} =1.3 is a margin for a robust calculation.

The value of the setting resistor is the result of a recursive calculation involving non-linear equations. For a quick calculation it is preferable to rely on the design spread sheet.



Figure 38	. Design tool	RSLOPE selection	n screenshot
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As shown in	Figure 3	88, the tool	suggests	R _{SLOPE} =90	9 kΩ.
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4.2.12 Setting the power switch Over current protection

Because of the amount of slope compensation impacts on the actual current limit threshold of the OCP circuitry, the calculation of the resistor at the CLIM pin is obtained from the already mentioned design tool.

Figure 39	. Design tool	RCLIM selection	screenshot
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Recommended over current protection threshold	loce	2.24	A	
Calculated value of RCLIM reistence	R	104 10	10	

The over current protection threshold is given by:

Equation 37

 $I_{OCP} \ge 1.3 \cdot I_{L,PK} = 2.24 A$

Where the 1.3 factor is introduced to avoid the OCP to be triggered during load transients.

Selecting a 3 A over current protection threshold, the RCLIM resistor is equal to:

Equation 38

 $R_{CLIM} = 104 k\Omega$

4.3 Efficiency estimation

The following paragraphs provide an estimation of the power dissipation related to the external components (mainly the inductor, the power switch and the fly-wheeling diode) and to the device.

4.3.1 **Power MOSFET power dissipation**

The choice of the power MOSFET basically depends on the maximum drain source voltage, the worst case peak and RMS drain current and a balance between the two contributions to the total power dissipation: conduction and switching power losses.

The conduction power losses are directly linked to the on-resistance ($R_{\text{DS},\text{ON}}$) and the worst-case RMS current:

Equation 39

 $P_{D,COND} = R_{DS,ON} \cdot I_{MOS,RMS}^2 = 45 \ m\Omega \cdot 1.48 \ A \cong 100 \ mW$

The switching power losses are given by:



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Equation 40

$$P_{D,SW} = V_{OUT,MAX} \cdot \frac{(t_{RISE} + t_{FALL})}{2} \cdot f_{SW} \cdot I_{OUT} \cdot \frac{V_{OUT,MAX}}{V_{IN,MIN}} \cong 300 \ mW$$

The overall power dissipation across the external switch is therefore:

Equation 41

 $P_{D,MOS} = P_{D,COND} + P_{D,SW} \cong 400 \ mW$

4.3.2 Free wheeling diode power dissipation

The power dissipation on the free wheeling diode is approximately given by:

Equation 42

 $P_{D,DIODE} = V_F \cdot I_{OUT} \cong 180 \ mW$

4.3.3 Inductor power dissipation

The inductor is subject to core power losses and DC coil resistance power losses. Usually the latter is predominant and the power dissipation in the worst case is approximately given by:

Equation 43

 $P_{D,IND} = R_{DCR} \cdot I_{L,RMS}^{2} \cong 130 \ mW$

4.3.4 Sensing resistor power dissipation

The power dissipated by the sensing resistor is given by:

Equation 44

 $P_{D,RSNS} = R_{SNS} \cdot I_{MOS,RMS}^{2} \cong 55 \ mW$

4.3.5 Input and output capacitors power dissipation

The power dissipated by the input capacitor is given by:

Equation 45

 $P_{D,CIN} = R_{ESR,CIN} \cdot I_{CIN,RMS}{}^2 \cong 1 \ mW$

While the power dissipated by the output capacitor is given by:

Equation 46

 $P_{D,COUT} = R_{ESR,COUT} \cdot I_{COUT,RMS}^{2} \cong 1 \ mW$

The total power losses due to the external components are therefore:

Equation 47

 $P_{D,EXT} = P_{D,MOS} + P_{D,DIODE} + P_{D,IND} + P_{D,RSNS} + P_{D,CIN} + P_{D,COUT} \cong 770 mW$



4.3.6 LED7708 power dissipation

Several sections of the LED7708 contribute to the overall chip power dissipation, although the main contributions come from the current generators, the linear regulators, the gate driver and the internal control circuitry.

The first contribution can be simply calculated as:

Equation 48

 $P_{D,GEN} = (N_{CH} \cdot I_{CH,on}) \cdot V_{CH,ON} \cong 320 \ mW$

Where all the channels are supposed to be active and the average voltage drop across them is $V_{CH,ON}{=}$ 1 V.

Of course a 100% dimming duty cycle is considered as worst case.

The power dissipated by the gate driver of the power switch is given by:

Equation 49

 $P_{D,DRV} = (Q_g \cdot f_{SW}) \cdot V_{LDO5} \cong 56 \, mW$

Where the first term in the parenthesis is the current consumption of the gate driver

The contributions of the two linear regulators are calculated as:

Equation 50

$$P_{D,LDO3} = I_{LDO3} \cdot \left(V_{IN,MIN} - V_{LDO3} \right) + V_{IN,MIN} \cdot I_{LDO3,BIAS} \cong 43 \ mW$$

Where:

- I_(LDO3,BIAS)=0.5 mA is the biasing current of the 3.3 V linear regulator;
- I_{LDO3}=5 mA is an estimation of the current drawn from the 3.3V linear regulator by the device (self-supply).

And

Equation 51

 $P_{D,LD05} = \left(V_{IN,MIN} - V_{LD05}\right) \cdot \left(Q_G \cdot f_{SW}\right) + V_{IN,MIN} \cdot I_{LD05,BIAS} \cong 70 \ mW$

Where V_{LDO5} = 5 V and $I_{LDO5,BIAS}$ = 1 mA is the biasing current of the 5 V linear regulator.

Although the worst case condition for the linear regulator is at maximum input voltage, equation 51 uses the minimum one in order to be consistent with the other power loss estimations.

Considering that the device could self supply its internal circuitry, the last power dissipation contribution is given by:

Equation 52

 $P_{D,IC} = I_{LDO3} \cdot V_{LDO3} \cong 17 \, mW$

The total power dissipated by the chip is therefore

Equation 53

 $P_{D,CHIP} = P_{D,GEN} + P_{D,DRV} + P_{D,LDO3} + P_{D,LDO5} + P_{D,IC} \cong 505 \, mW$

An estimation of the junction operating temperature is easily calculated as:



Equation 54

 $T_J = P_{D,CHIP} \cdot R_{TH,JA} + T_{AMB} \cong 70 \ ^{\circ}C$

Where $R_{TH,JA} = 35 \text{ °C/W}$ and $T_A = 50 \text{ °C}$ Considering that the output power for the given application is

Equation 55

 $P_{OUT} = (V_{OUT,MAX} - V_{CH,ON}) \cdot N_{CH} \cdot I_{CH,ON} \cong 12.04 W$

The boost converter efficiency is given by:

Equation 56

 $\eta_{BOOST} = \frac{P_{OUT}}{P_{OUT} + P_{D,EXT}} \cong 94.7\%$

While the overall application efficiency is:

Equation 57

 $\eta = \frac{P_{OUT}}{P_{OUT} + P_{D,EXT} + P_{D,CHIP}} \cong 90\%$

4.4 Control loop

The boost converter of the LED7708 is based on a current mode (CM) controller. Stability and optimal dynamic performance are achieved by properly designing the compensation network. Similarly to most part of the CM boost regulators, the model of the loop gain is obtained as the product of control to output transfer function (G(s)) and the feedback transfer function (H(s)).

Equation 58

$$\frac{v_{OUT}(s)}{I_C(s)} = G(s) \cdot H(s)$$

The control to output transfer function is

Equation 59

$$G(s) = \frac{\frac{(1 - \frac{s}{\omega_{ZRHPZ}}) \cdot (1 + \frac{s}{\omega_{ESRZ}})}{1 + \frac{s}{\omega_{P1}}} \cdot F_h(s)$$

where

Equation 60

$$\omega_{ZRHPZ} = \frac{\frac{V_{OUT,MAX}}{I_{OUT}} (1 - D_{MAX})}{L}$$

Equation 61

$$\omega_{ESRZ} = \frac{1}{C_{OUT} \cdot R_{ESR,COUT}}$$

Equation 62 $\omega_{P1} = \frac{I_{OUT}}{C_{OUT} \cdot V_{OUT,MAX}}$



And the sampling model is taken into account by

Equation 63

$$F_{h}(s) = \frac{1}{(1 + \frac{s}{2 \cdot \pi \cdot f_{SW} \cdot Q_{P}} + \frac{s^{2}}{(2 \cdot \pi \cdot f_{SW})^{2}})}$$

where

Equation 64

$$Q_P = \frac{1}{\pi \cdot (m_C \cdot (1 - D_{CCM}) - 0.5)} = 0.69$$

and

- $m_C = 1 + \frac{S_E}{S_N} = 3.41$ $S_N = \frac{V_{IN,MIN}}{L} = 2.7 \cdot 10^4 \frac{V}{s}$ $S_E = 6.51 \cdot 10^4 \frac{V}{s}$

The simplified feedback transfer function, H(s) is given by:

Equation 65

$$H(s) = A_{V,COMP} \cdot G_{m,EA} \cdot \left(\frac{1 + s \cdot R_{COMP} \cdot C_{COMP}}{s \cdot C_{COMP}}\right)$$

Where $A_{v,COMP} = 0.25$ and Gm,EA = 1 mS are characteristic of the internal transconductance amplifier connected at the COMP pin, while RCOMP and CCOMP are determined by the loop compensation strategy.

The slope compensation amount (SE) used in equation 64 is obtained by a recursive calculation base on non linear equations. The design tool provides the proper amount of compensation slope for a given operating point.

Figure -	40. Desiaı	n tool sam	plina pa	oles coef	ficients s	screenshot

Sampling poles coefficients:	Sn	2.70E+04	VIs	
	S.	6.51E+04	VIs	
	mo	3.41		
	Q.,	0.69		

Because of the regulation of the LED current is demanded to the constant current generators, there are virtually no load transients. Limited input voltage transients and relatively slow output voltage transitions due to the output adjustment algorithm do not ask for a high bandwidth.

A simple strategy to compensate the loop gain is fixing the cut off frequency well below the right half plane zero or half the switching frequency:

Equation 66

 $f_{RHPZ} = 152kHz$

Equation 67

 $f_{MAX} = \frac{f_{SW}}{2} = 300 kHz$



Equation 68

$$f_{0,S} \cong \frac{\min(f_{RHPZ}, \frac{JSW}{2})}{10} = 15.2 KHz$$

This initial limit for the bandwidth allows the calculation of the $\mathsf{R}_{\mathsf{COMP}}$ resistor:

Equation 69

 $R_{COMP,CALC} = \frac{2\pi \cdot f_{0,S} \cdot C_{OUT}}{\frac{V_{IN,MIN}}{V_{OUT,MAX}} \cdot Av_{COMP} \cdot G_{m,EA}} \cong 13.5 \, K\Omega$

The nearest standard value is:

Equation 70

 $R_{COMP} = 13k\Omega$

The capacitor of the network compensation is calculated by forcing the pole frequency to 1/10 of the selected cut off one.

Equation 71

$$C_{COMP,CALC} = \frac{1}{2\pi \cdot \frac{f_{0,S}}{10} \cdot R_{COMP}} \cong 4 \ nF$$

The nearest standard value is:

Equation 72

 $C_{COMP} = 3.9nF$

The Bode diagrams of the loop gain with the selected compensation network are shown in figure 40. The estimated cross-over frequency is $f_0=15.9$ kHz, while the resulting phase margin is PM = 70 deg.

For comparison the measured diagrams (dotted curves) have been added. The actual cross-over frequency is $f_0=15.2$ kHz, while the resulting phase margin is PM = 68 deg.



Figure 41. Mathematical model, GLoop acquisition comparison



5 Design tool

5.1 Introduction

To simplify and make faster the application design, a dedicated spread-sheet has been developed.

The sequence of design steps follows the same approach described in the previous paragraphs, making the selection of the external components quick end intuitive.

Two kinds of cells are basically present in the design tool:

- Green cells, to be filled by the user when a choice is required;
- Yellow cells, showing the results of the calculations based on the application specifications and/or the user's selections.

The design tool consists of four different sheets:

- "LED7708 design", where the application specifications are entered and the value of the setting components is provided;
- "External components data", where the user is asked to insert the technical specifications of some external components;
- "Power dissipation & losses", where an estimation of the power dissipated on the critical components is calculated;
- "Control loop compensation", where the proper network compensation is calculated to optimize the dynamic behavior of the boost converter section.

5.2 LED7708 design

The "LED7708_design" sheet is divided in 14 steps.

As a first step the application specifications must be entered (Figure 39).

Figure 42. Design tool, <Step 1. Application data> screenshot

Step 1. App	nication data				1			
	Input voltage range	V _N	10.8	12	13.2		v	
	Number of used channels	Now	1	16				
	Number of LED	N _{uto}		10				
	Channel current during on-phase	юкал	- 1	0.02		A		
	Channel current during off-phase	Сная		5		μA		
	Minimum LED Vf	V _{#38m}		3		v		
	Maximum LED Vf	Vestax	- 1	3.6		v		
	Expected operating ambient temperature	TA		50		°C		
	Minimum LED operating temperature	TLEO.ven	1	-20		°C		
	Maximum LED operating temperature	TLEDMAX		100		°C		
	Boost converter switching frequency	f _{sw}		600		kHz		
	Output dimming frequency	fore	1	120		Hz		
	Selected dimming resolution (12-bit or 16-bit)	N		16	1	bit		

The second step allows the user to select the VMIN pin setting and the output divider resistors in order to fit the LED supply voltage requirements (*Figure 43*).



Step 2. C	Dutput divider design						
	for the second second second		-	20.0			
	Expected minimum output votage	VLED.min		23.3	-	V	
	Expected mean output voltage	VLED.HEAN		33.2	-	V	
	Expected maximum output voltage	VLEDMAX	_	30.0	-	V	
	Expected output voltage swing	AVLED = VLED.MAX - VLED.min		0.0		v	
	VMIN pin setting		GND	VCC	220k	FLOAT	
	Output divider ratio		0.03	0.03	0.02	0.02	
	Over voltage protection threshold selection	VovP.ceic	42.80	44.72	46.63	52.39	v
	Maximum output voltage selection	VLED.MAX.cell	38.22	39.21	40.21	43.20	v
	Mean ouput voltage selection	VLED.NEAN.calc	33.24	33.24	33.24	33.24	v
	Minimum output voltage selection	VLED,min.cale	28.34	27.36	26.38	23.43	v
	Delta Output voltage selection	AVertice	9.88	11.85	13.83	19.77	v
	Output voltage swing	ΔV _{LED} -ΔV _{OUT celo}	3.10	5.07	7.05	12.99	v
	Minimum output voltage swing	MIN(AV, as a base and a)		31	1	v	
		with the tips whole takes					
	Recommended VMIN pin setting			GND			
	VMIN pin selected (GND,VCC,220K,FLOAT)	Best choice		GND			
	High side resistor selected	Rovves		511		kΩ	
	Reccomended low side resistor			1.60E+01	1	kΩ	
	Selected low side resistor	Rovus		16		kΩ	
	Minimum output voltage	Voutimin	-	28.35		v	
	Output voltage mean	VOUTMEAN		33.25	1	v	
	Maximum output voltage	VOLTMAX		38.23	1	V	
	Over voltage protection threshold	Varia		42.82		v	

Figure 43. Design tool, <Step 2. Output divider design> screenshot

The VMIN pin can be set low (GND), high (VCC), to an intermediate voltage (220K? resistor to ground) or left floating (FLOAT). According to the characteristics and the operating temperature range of the LEDs, the tool provides the resulting output voltage ranges corresponding to the above mentioned settings of the VMIN pin.

A more detailed description of the function of the VMIN pin can be found in the LED7708 datasheet.

Once the output voltage swing has been selected, the proper output divider can be determined. The user is asked to select a value for the high side resistor, while the low-side one is calculated consequently.

The third step allows the user to set the resistor at the FSW, GSK, SETH and ISETL pins based on the initial application specifications (*Figure 44*).

Figure 44. Design tool, <step 3.="" and="" fosc="" iseth,="" isetl="" pin="" resistors:<="" setting="" th=""><th>></th></step>	>
screenshot	

FSW resistor	R _{fm}	83.3	kΩ
GSCK frequency	fasce	7864.3	kHz
FOSC resistor	Rresc	50.9	kΩ
ISETH resistor	R _{SETM}	60.0	kΩ
ISETL resistor	R _{sst}	800.0	kΩ

The fourth step shows the operating corner table, obtained using the minimum, typical and maximum values for both the input and output voltages. For all the combinations are calculated the switching duty cycle and the minimum inductor value to ensure continuous conduction mode (CCM) operation of the boost converter.



p il operation	g curanono corrier table				_			
	Device operating matrix	Vallout	min/min	min/max	max/min	max/max	typ/typ	
		VN	10.80	10.80	13.20	13.20	12.00	V
		but	0.32	0.32	0.32	0.32	0.32	A
		Vout	28.35	38.23	28.35	38.23	33.25	V
	Duty cycle in CCM	Doox	0.62	0.72	0.53	0.65	0.64	
	DCM-CCM boundary Inductance	Lmin for CCM	6.63	5.70	8.55	7.77	7.21	μH

Figure 45. Design tool, <Step 4. Operating conditions corner table> screenshot

With the following step the user is asked to select the value of the inductor, taking into account the minimum inductance for CCM operation and the current ripple amount (usually set as 30%-50% of the average inductor current).

Figure 46. Design tool, <Step 5. Inductor selection> screenshot

Minimum inductor for CCM operation	Lmin, DOV		8.55		μH		
Avarage coll current	Luo	1	0.89		A		
Inductor selected	Lations		10		μН		
Minimum LED current for CCM operation		0.21	0.18	0.27	0.25	0.23	A
CCM flag indicator		TRUE	TRUE	TRUE	TRUE	TRUE	

The sixth step allows the user to select the application corner, value of input and output voltage that will be used in the following part of the design tool.

The most critical operating condition for a boost converter is minimum input voltage and maximum output voltage (column #2 of the operating matrix).

Figure 47	. Design tool,	< Step 6.	Operating	point selection>	screenshot
-----------	----------------	-----------	-----------	------------------	------------

Device operating matrix		1	2	3	4	5	
	VaVout	min/min	min/max	max/min	max/max	typ/typ	v
	V _N	10.80	10.80	13.20	13.20	12:00	A
	lout	0.32	0.32	0.32	0.32	0.32	v
	Vour	28.35	38.23	28.35	38.23	33.25	
Duty cycle in CCM	Doow	0.62	0.72	0.53	0.65	0.64	
DCM-CCM boundary Inductance	Lmin for CCM	7.78	4.96	10.03	6.76	7.20	μH
CCM flag indicator		TRUE	TRUE	TRUE	TRUE	TRUE	
Selected row			2.00				
Selected input voltage	V _{NSE.}		10.80		v		
Selected output current	but set		0.32		A		
Selected output voltage	Vourise.		38.23		v		
Selected duty cycle	D _{SE.}		0.72				
CCM flag indicator			TRUE	1			

Step #7 gives to the user an estimation of the peak and RMS current in the inductor related to the chosen operating point. The selection of a suitable part capable of sustaining these values is demanded to the user.

Figure 48. Design tool, <Step 7. Inductor peak and RMS current estimation> screenshot

Avarage coil current	Lavo	1.08	A	
Ripple coil obtained	۵٤,	1.29	A	
Coil peak current	La .	1.72	A	
Coil RMS current	Laus	1.14	A	

Step #8 is dedicated to the calculation of the minimum output capacitor based on the maximum output voltage ripple. In practice a 10 μ F minimum capacitance is advisable. When MLCCs capacitors are used, the capacitance drop due to the biasing voltage has to be taken into account (Y5V dielectric type is not recommended).



Step 8. Outpu	it capacitor selection		a a a		· · · · ·
	Selected maximum output ripple	V _{out/spie}	0.015	v	
	Recommended minimum value of output capacitor	Cour.min	8.39	μF	
	Selected output capacitor	Cour	10.00	μF	
	Ouput capacitor RMS current	bour aus	0.52	A	

Figure 49. Design tool, <Step 8. Output capacitor selection> screenshot

The ninth step allows the user to select the value of the input capacitor. In a boost converter the input capacitor is usually not critical at all, although a relatively stable input rail is desirable. A locally placed electrolytic capacitor helps a lot is having an almost ripple free input rail, but often this is a bulky solution. Assuming an input voltage ripple in the order of few tens of millivolts (eventually 100 mVpp), a reasonable value of few tens of micro Farads are the calculated (*Figure 50*).

Figure 50. Design tool, < Step 9. Input capacitor selection> screenshot

Select maximum input voltage ripple	V _{iN/opie}	0.10	v	
Recommended minimum value of input capacitor	C _{N,mn}	7.72	μF	
Selected input capacitor	C _{IN}	40.00	μF	
Input capacitor RMS current	knas	0.46	A	

Step #10 simply provides the estimated peak and RMS current flowing through the power MOSFET. The selection of the switch should be made according to these values, the maximum drain source voltage (i.e. the maximum output voltage) and some margin (30%-50%).

The on resistance of the selected switch should be as low as possible to improve the overall efficiency, although the resulting higher gate capacitance could lead to switching losses that overcome the conduction ones. For this reason a trade off driven by the estimation of the two contributions is recommended.

Figure 51. Design tool, <Step 10. Power MOSFET peak and RMS current estimation> screenshot

rot offer moor Er pear a	id rand darran countered				
Switch peak cur	rent	luce.or	1.72	A	
Switch RMS curr	rent	hos reis	1.48	A	

Step #11 allows the user to select the current sense resistor (*Figure 52*). This resistor is required to have a minimum value for an acceptable signal/noise ratio at the CSNS pin.

Step 11. Sens	any resision selection				
	Minimum value of the voltage drop on the sensing resistor	V _{INI.mn}	25.00	mV	
	Minimum current of Rsense resistor	lava	129	A	
	Recommended minimum value of Rsense resistor	Ravaurin	19.36	mΩ	
	Selected Rsense resistor	Reve	25.00	mΩ	

The following step is dedicated to the selection of the slope compensation resistor. An iterative calculation, based on non linear equation, is involved in the determination of the value of this component (*Figure 53*).



otep it. otope					
	Compensation slope evaluated	Sg.mn	6.68E+04	Als	
	Recommended value of RSLOPE resistor	Record.com	909.00	kΩ	
	Selected RSLOPE resistor	Relove	909.00	kΩ	
	Compensation slope for the selected RSLOPE resistor	Sg	6.51E+04	Als	

Figure 53. Design tool, <Step 12. Slope compensation resistor selection> screenshot

Once the resistor at the SLOPE pin has been selected, step #13 determines the value of the power switch Over-Current Protection (OCP) setting one (CLIM pin).

Figure 54. Design tool. <step 13.="" mosfet="" ocp="" power="" setting=""> :</step>	screenshot
---	------------

Poole Construction of Construction	and a second a second a			1 1	1
	Recommended over current protection threshold	bor	2.24	A	
	Calculated value of RCI III reistance	Read	104 10	ko	

5.3 External components

This sheet contains the relevant data of the power components. These values are used in the estimation of the losses and as a check threshold for some critical variable (e.g. peak and RMS current) in the worst case operation.

External MOSFET drain-source on resistance	Roson	45.00	m
External MOSFET rise time	teise	13.00	ns
External MOSFET fall time	tFALL	10.00	ns
External MOSFET gate charge	Qo	17.00	nC
Free-wheel diode forward voltage	V _F	0.56	v
Inductor DC resistance	Rocil	101.00	mű
Input capacitor ESR	RESP.CIN	5.00	mű
Output capacitor ESR	RESR.COUT	5.00	má
Chip supply current and external load at LDO3 pin	Loos	5.00	m/

Figure 55. Design tool, <External components> screenshot

5.4 Power dissipation and losses

This sheet provides an estimation of the power dissipation across the external components and the losses in the device.



Figure 56. Design tool, <Step 14. External components power losses estimation> screenshot

Mosfet conduction power losses	Pacono	99.15	mW	
Mosfet switching power losses	Polsw	298.82	m₩	
Total Mosfet power dissipation	P _{D.Mos}	397.97	m₩	
Freewheel diode power dissipation	P _{D,Diose}	179.20	mW	
Inductor power dissipation	P _{D,IND}	131.00	mW	
Sensing resistor power dissipation	Polesna	55.08	mW	
input capacitor power dissipation	PDON	1.08	mW	
Output capacitor power dissipation	Poloout	1.37	m₩	
Total external components power dissipation	Poser	0.77	v	

These calculations should refer to the worst case operating conditions (minimum input and maximum output voltages, maximum load) to ensure that all the selected parts operate in their respective safe operating area (SOA).

Figure 57. Design tool, <Step 15. LED7708 power dissipation estimation> screenshot

Output services	0	10.04	1.1	
Output power	Pour	12.04	W	
Current generators power dissipation	P _{D,Gen}	320.00	m₩	
Power Mosfet gate-driver power dissipation	Posseoner	56.00	m₩	
3V3 linear regulator power dissipation	Poloos	42.90	m₩	
5V linear regulator power dissipation	Poloos	69.96	m₩	
Internal chip (control circuitry) power dissipation	Polic	16.50	m₩	
Total chip power dissipation	P _{DChip}	505.36	m₩	
Chip junction temperature	T.	67.69	°C	

The calculated overall efficiency is a good estimation of the real one, although an experimental verification is advisable.

Figure 58. Design tool, <Step 16. Efficiency estimation> screenshot

top to. Enciency countation	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		 1 1 11
Boost converter efficiency	necost	0.94	
Overall eficiency	0	0.90	

5.5 Control loop compensation

The stability and the dynamic behavior of the boost converter is achieved by properly designing the compensation network, basically an R-C series connected at the output of the trans-conductance error amplifier. The tool calculates the frequency of the poles and the zeroes of the loop gain transfer function and suggests the bandwidth that minimizes the effects of the right half plane zero. The compensation network is therefore calculated by assuming a dominant pole behavior.



AN4578

Sampling poles coefficients:	Sn	2.70E+04	VIs	
	S,	6.51E+04	VIs	
	mo	3.41		
	Q _p	0.69		
Right halp plane zero (RPHZ) frequency	f _{2RHP}	151.74	kHz	
ESR zero frequency	fzesa	3183.10	kHz	
Half switching frequency	f _{sw}	600.00	kHz	
More pressing frequency constrain	f_INIT	151.74	kHz	
Maximum bandwidth suggested (0.1*fLIHIT)	BWs	15.17	kHz	
Bandwidth selected	BW	15.00	kHz	
Comp resistor suggested	Roomes	13.35	kΩ	
Comp resistor selected	Roowe	13.00	kΩ	
Frequency compensation pole	foome	3.00	kHz	
Comp capacitor suggested	Comps	4.08	nF	
Comp capacitor selected	Cours	3.90	oF	

Figure 59. Design tool, <Step 17. Compensation network design> screenshot

The Bode diagrams (magnitude and phase) of the loop gain transfer function is plotted and an estimation of the cut off frequency and the phase margin (PM) is calculated (*Figure 60*).



Figure 60. Design tool, < Step 18. Loop gain Bode diagram> screenshot



6 Revision history

Table 19.	Document	revision	history

Date	Revision	Changes
25-May-2015	1	Initial release.
12-Jan-2016	2	Updated: Figure 2, Figure 3, Figure 4 and Figure 5.



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