Using the UCD3138HSFBEVM-029

User's Guide

Literature Number: SLUUA95
March 2013

Digitally Controlled Hard-Switching Full-Bridge DC-DC Converter

1 Introduction

This EVM, UCD3138HSFBEVM-029 is to help evaluate the UCD3138RHA 40-pin digital control device in a 48-V telecom power conversion application and then to aid in UCD3138 design. The EVM is a standalone Symmetrical Hard Switching Full-Bridge (HSFB) DC-DC power converter.

The UCD3138HSFBEVM-029 can be used as it is delivered without additional work, from either hardware or firmware, to evaluate a hard switching symmetrical full-bridge DC-DC converter. This EVM allows for some of its design parameters to be re-tuned using a GUI based tool, called Texas Instruments Fusion Digital Power Designer. It is also possible to load custom firmware with user's own definition and development.

This user's guide provides basic evaluation instruction from a viewpoint of system operation in a standalone symmetrical HSFB DC-DC power converter.

WARNING

• High voltages are present on this evaluation module during operation and for a while even after power off. This module should only be tested by skilled personnel in a controlled laboratory environment.

• High temperature exceeding 60C may be found during EVM operation and for a while even after power off.

• This EVM's purpose is to facilitate the evaluation of digital control in a hard switching full bridge dc converter using the UCD3138, and cannot be tested and treated as a final product.

• Read and understand this user's guide thoroughly before starting any physical evaluation.

2 Description

The UCD3138HSFBEVM-029 demonstrates a symmetrical hard switching full-bridge DC-DC power converter with digital control using the UCD3138RHA 40-pin device. This EVM is with preloaded firmware that provides the required control functions for an HSFB converter. For details of the firmware please contact TI. UCD3138HSFBEVM-029 accepts a DC input from 36 V_{DC} to 72 V_{DC}, and outputs a nominal 12 V_{DC} with full output load power 360 W, or full output current 30 A.

2.1 Typical Applications

- 48-V Telecom DC-DC Power Conversion
- Servers
- Telecommunication Systems

2.2 Features

- Digitally Controlled and Standalone Hard Switching Full-Bridge DC-DC Power Conversion
- Voltage Mode Control
- Secondary Side Control
- DC Input from 36 V_{DC} to 72 V_{DC}
- 12 V_{DC} Regulated Output from No Load to Full Load
- Full-Load Power 360 W, or Full-Load Current 30 A
- High Efficiency
- Constant Soft-tart Time
- Protection: Over Voltage, Under Voltage, Over Current, and Over Temperature
- Constant Current and Constant Power
- Input Voltage Feed Forward Control
- PMBus Communications
- Test Points to Facilitate Device and Topology Evaluation

3 Performance Specifications

Table 1. UCD3138HSFBEVM-029 Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage operation range		36		72	V_{DC}
Input UVLO On			35		V_{DC}
Input UVLO Off			32		V_{DC}
Input current	Input = 36 V_{DC}, Full Load = 30A			11	A
Input current	Input = 48 V_{DC}, Full Load = 30A			9	A
Input current	Input = 72 V_{DC}, Full Load = 30A			6	A
Output Characteristics					
Output voltage, VOUT	No Load to Full Load		12		V_{DC}
Output load current, IOUT	36 to 72 V_{DC}			30	A
Output voltage ripple	48 V_{DC} and Full Load = 30A		30		mVpp
Systems Characteristics					
Switching frequency			200		kHz
Peak efficiency	48 V_{DC}, Load = 20A		94.5%		
Full load efficiency	48 V_{DC}, Full Load = 30A		93.5%		
Operating temperature	Typical 400 LFM forced air flow		25		ºC

4 Schematics

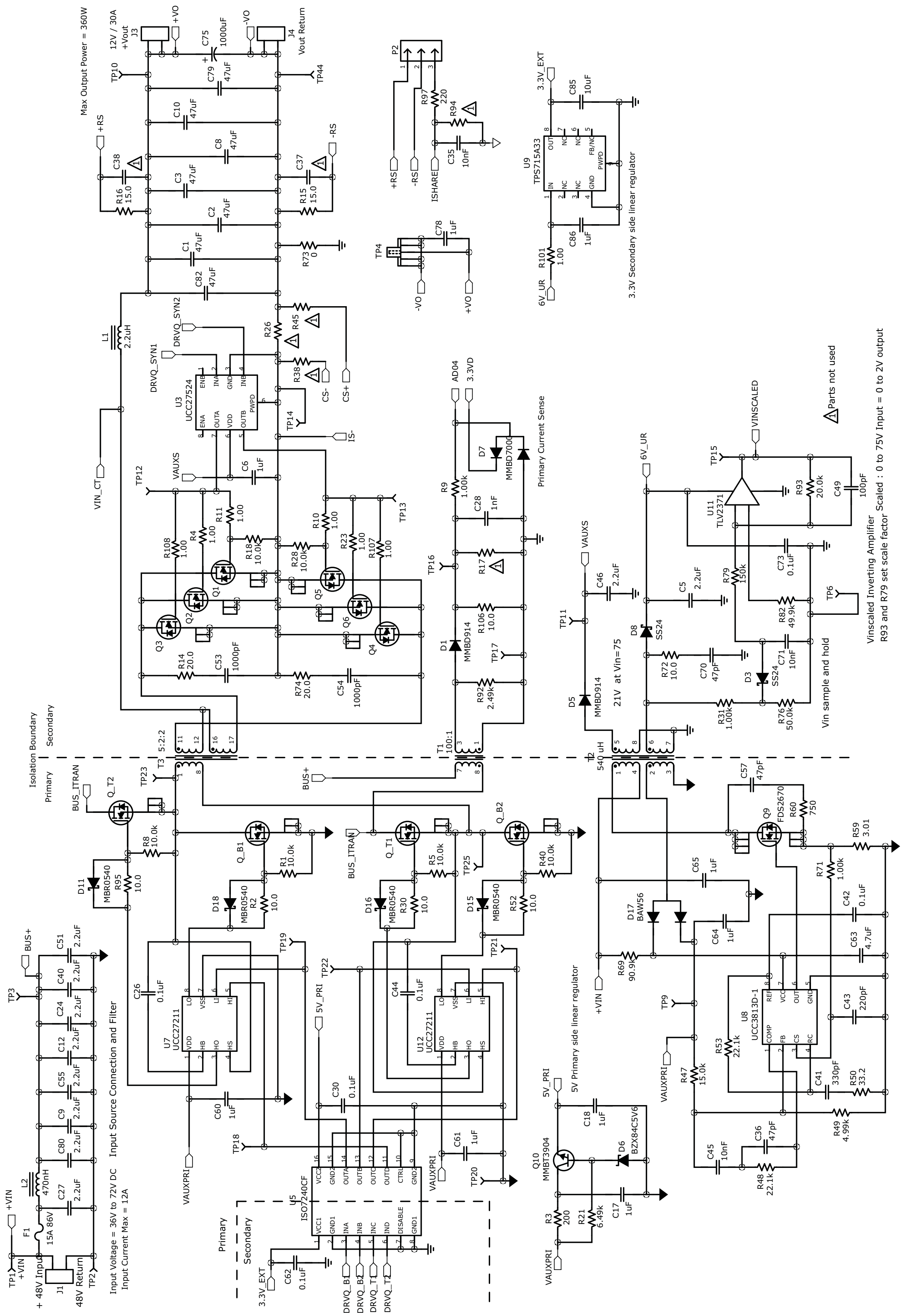


Figure 1. UCD3138HSFBEVM-029 Schematics Sheet 1 of 3

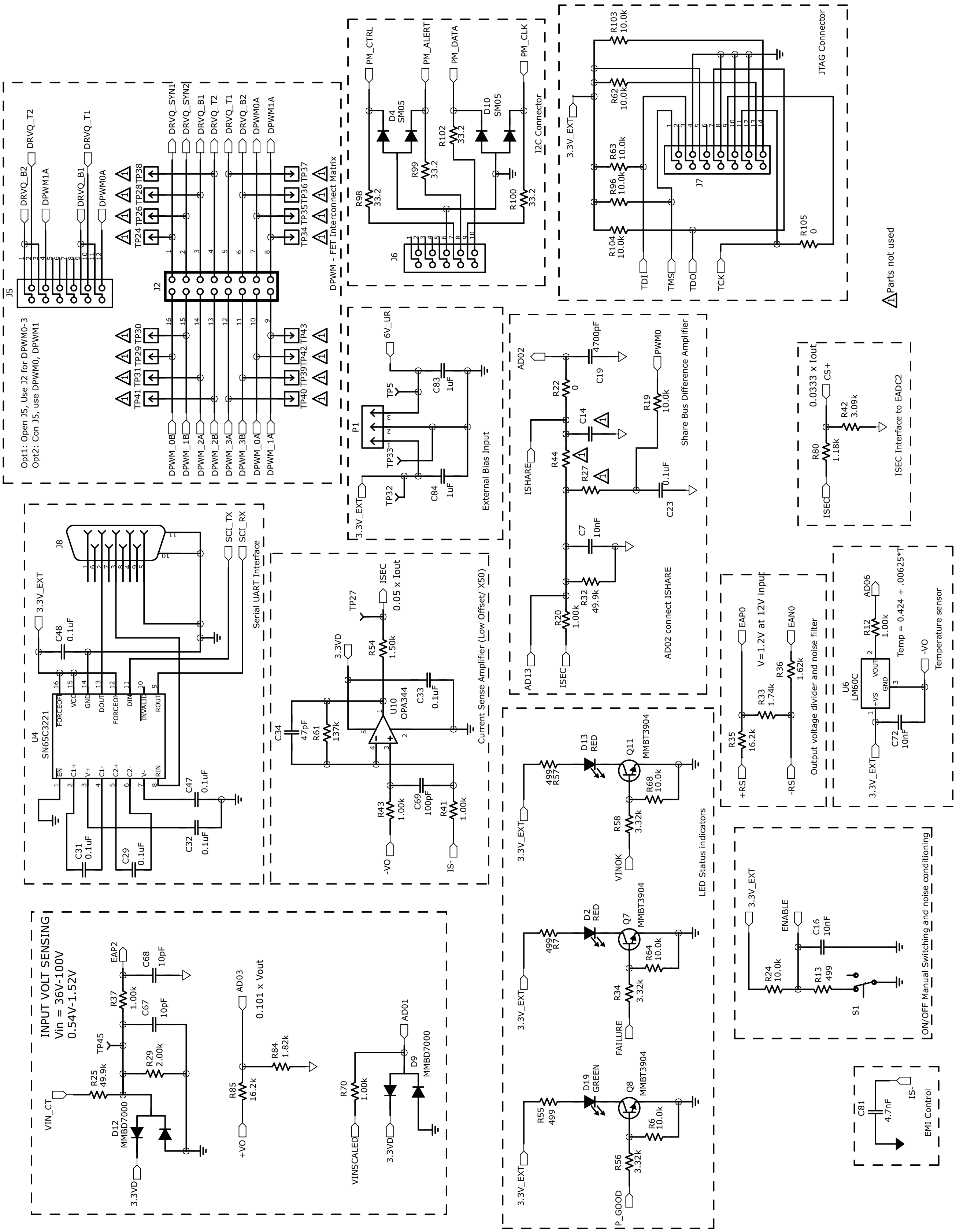


Figure 2. UCD3138HSFBEVM-029 Schematics Sheet 2 of 3

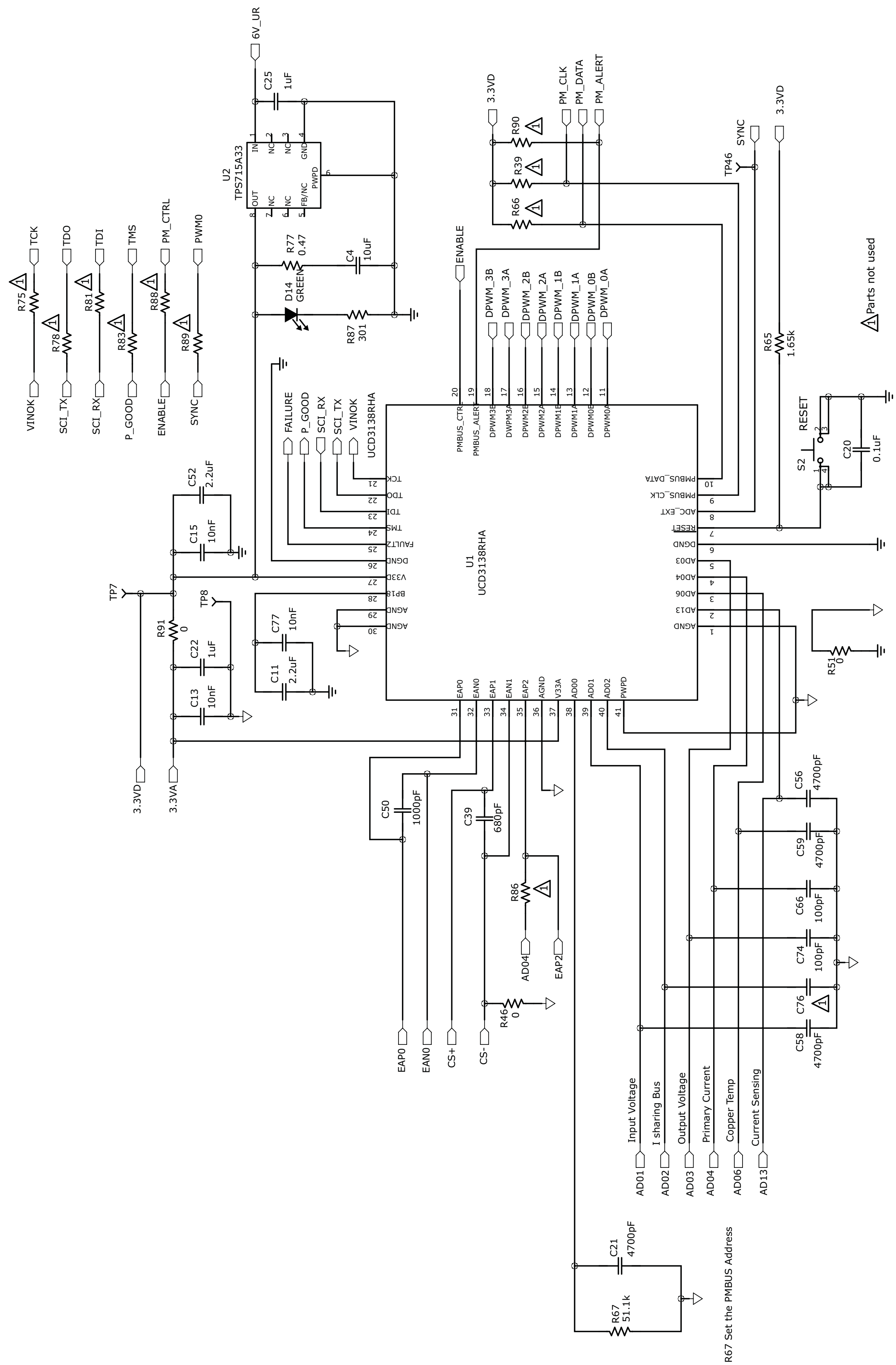


Figure 3. UCD3138HSFBEVM-029 Schematics Sheet 3 of 3

5 Test Setup

5.1 Test Equipment

DC Voltage Source: capable of 36 V_{DC} to 72 V_{DC}, adjustable, with minimum power rating of 400W, or current rating not less than 12A, with current limit function.

DC Multi-meter: 1 unit capable of 0 V_{DC} to 75 V_{DC} input range, four digits display preferred; and 1 unit capable of 0 V_{DC} to 15 V_{DC} input range, four digits display preferred.

Output Load: DC load capable of receiving 0 V_{DC} to 15 V_{DC}, 0 to 30A, and 0 to 360W or greater, with display such as load current and load power.

Current-meter, DC, optional in case the load has no display, 1 unit, capable of 0 to 30A. A low ohmic shunt and DMM are recommended.

Oscilloscope: capable of 500MHz full bandwidth, digital or analog, if digital 5Gs/s or better

Fan: 400 LFM forced air cooling

Recommended Wire Gauge: capable of 30A, or better than #14 AWG, with the total length of wire less than 8 feet (4 feet input and 4 feet return).

5.2 Recommended Test Setup

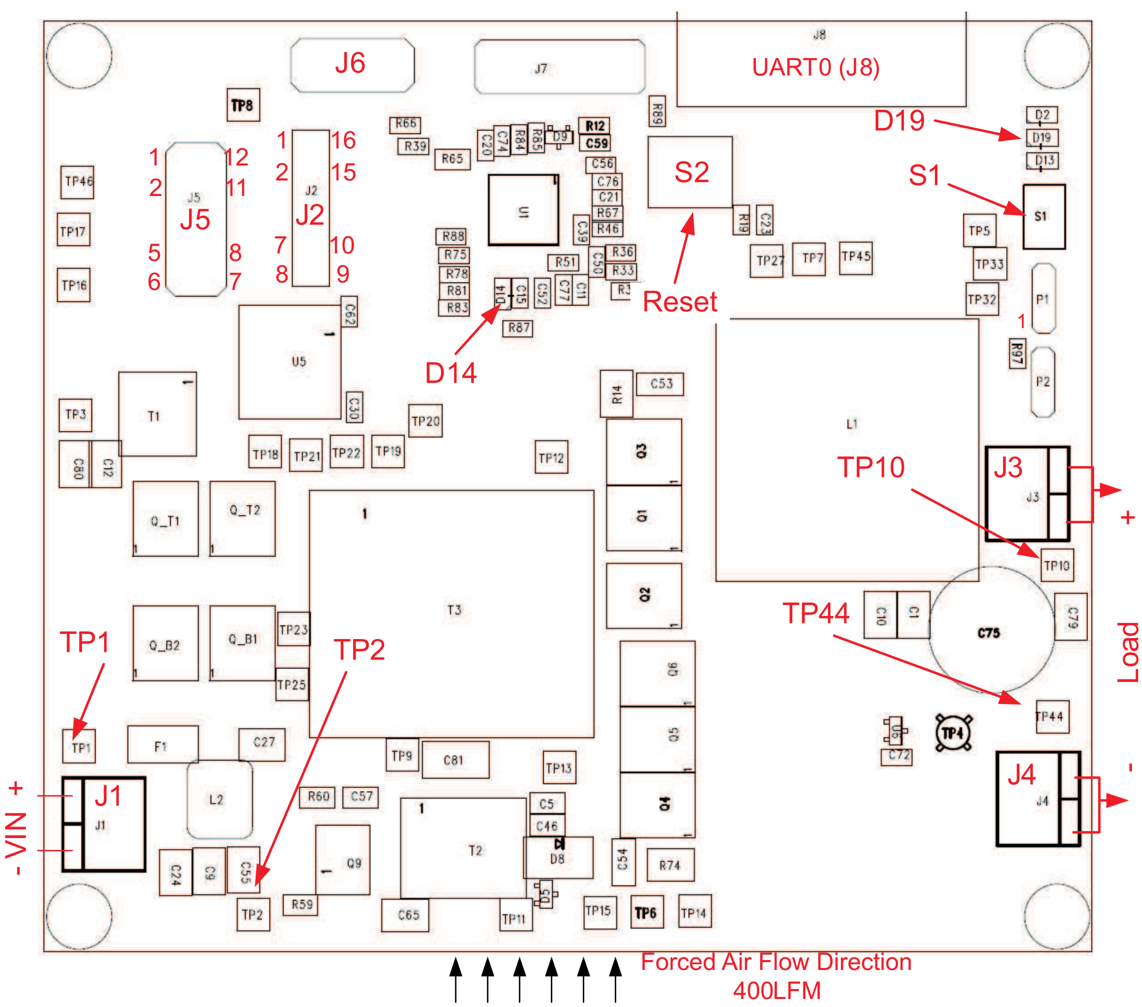


Figure 4. UCD3138FBHSEVM-029 Recommended Test Set Up

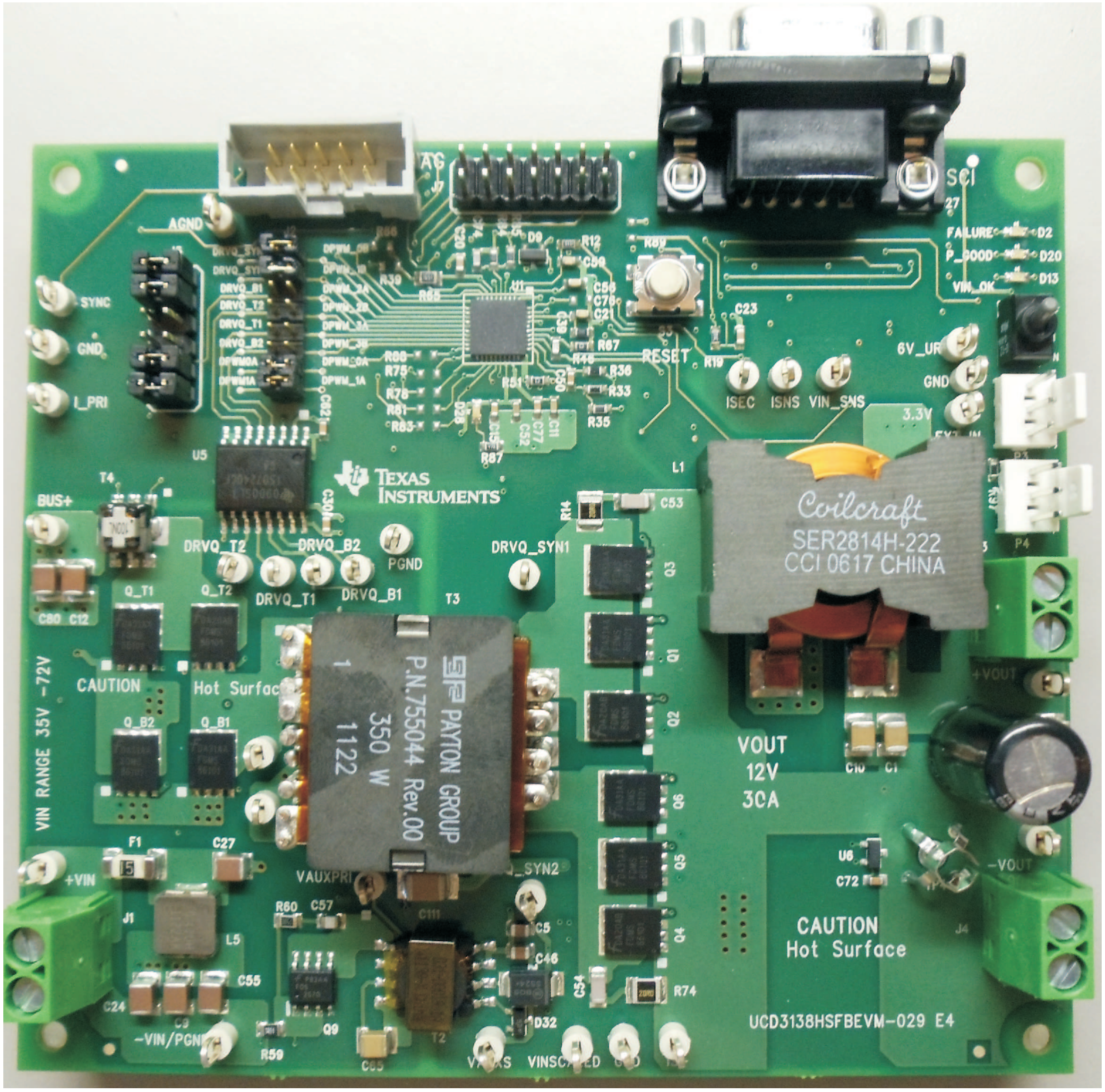


Figure 5. UCD3138HSFBEVM-029 – Board Outlook

6 List of Test Points

Table 2. List of Test Points

TEST POINTS	NAME	DESCRIPTION
TP1	+VIN	Input Voltage positive
TP2	PWRGND	Input Voltage negative
TP3	+BUS	Input voltage after filter
TP4	Voripple	BNC Vo ripple
TP5	6V UR Bias	Secondary Bias 6V_UR
TP6	PGND	Secondary bias GND
TP7	3.3VD	3.3VD
TP8	AGND	UCD3138 AGND
TP9	VAUXPRI	Primary side bias voltage
TP10	+Vo	+Vout test
TP11	VAUXS	Secondary side bias voltage
TP12	SR_Drive1	Drive to FET Q1, 2 and Q3
TP13	SR_Drive2	Drive to FET Q4, 5 and Q6
TP14	IS-	Secondary side current sense negative
TP15	VINSCALED	VIN monitoring sense on secondary side
TP16	I_Pri	Primary side current sense transformer output on secondary side
TP17	PGND	Secondary bias GND
TP18	DRV_QT2_iso	Q_T2
TP19	DRV_QB1_iso	Q_B1
TP20	PWRGND	Input Voltage negative
TP21	DRV_QT1_iso	Q_T1
TP22	DRV_QB2_iso	Q_B2
TP23	T3-1	Transformer T3 pin 1
TP24		Not Used
TP25	SW1	Switch node of Q_T1 and Q_B2
TP26		Not Used
TP27	ISEC	Secondary side current copper sensing after conditioning
TP28		Not Used
TP29		Not Used
TP30		Not Used
TP31		Not Used
TP32	3.3VEXT	3.3V_EXT
TP33	PGND	Secondary bias GND
TP34		Not Used
TP35-43		Not Used
TP44	-VO	-Vout test
TP45	EAP2	EAP2
TP46	SYNC	UCD3138 SYNC

7 List of Terminals

Table 3. List of Terminals

TERMINAL	NAME	DESCRIPTION
J1	VIN Input	2-pin, input voltage, 36 V_{DC} to 72 V_{DC}
J2	Driver-A	16-pin header, DPWM to driver configuration

Table 3. List of Terminals (continued)

TERMINAL	NAME	DESCRIPTION
J3	+VO	2-pin, output power positive
J4	-Vo	2-pin, output power negative
J5	Driver-B	12-pin header, DPWM to driver configuration
J6	PMBus	10-pin PMBus connection
J7	JTAG	14-pin JTAG connection
J8	UART0	Standard UART connection, RS232, 9-pin female
P1	Bias	External bias terminal for firmware debugging without power stage on
P2	ISHARE	ISHARE and load current sense

8 Test Procedure

8.1 Efficiency Measurement Procedure

WARNING

Danger of electrical shock. High voltage present during the measurement.

Do not leave EVM powered when unattended.

Danger of heat burn from high temperature.

1. Refer to Figure 4 for basic set up to measure power conversion efficiency. The required equipment for this measurement is listed in Section 5.1.
2. Before making electrical connections, visually check the boards to make sure no shipping damage occurred.
3. In this EVM package, two EVMs are included, UCD3138HSFBEVM-029, and USB-TO-GPIO. For this measurement, the UCD3138HSFBEVM-029 board is needed.
4. Connect the DC voltage source to J1-1 (+) and J1-2 (-). Set up the DC output voltage in the range specified in Table 1, between 36 V_{DC} and 72 V_{DC}; set up the DC source current limit 12A.
5. Connect an electronic load with either constant current mode or constant resistance mode. The load range is from zero to 30A.
6. Check and make sure the jumpers are installed correctly on J2 and J5.
   (a) J2 should be jumped across to connect its 1-16, 2-15, 7-10, and 8-9.
   (b) J5 should be jumped across to connect its 1-12, 2-11, 5-8, and 6-7.

WARNING

Follow the connections correctly to avoid possible damages.

7. It is recommended to use the switch S1 to turn on the board output after the input voltage is applied to the board. Before applying input voltage, make sure the switch, S1, is in the “OFF” position.
8. If the load does not have a current or a power display, a current meter or low ohmic shunt and DMM will be needed between the load and the board for current measurements.
9. Connect a volt-meter across the output connector and set the volt-meter scale 0 to 15V on its voltage, DC.
10. Turn on the DC voltage source output, flip S1 to “ON” and vary the load. Record output voltage and current measurements.

8.2 Equipment Shutdown

1. Shut down the DC voltage source
2. Shut down the electronic load.

9 Performance Data and Typical Characteristic Curves

Figure 6 through Figure 14 present typical performance results for UCD3138HSFBEVM-029.

9.1 Efficiency

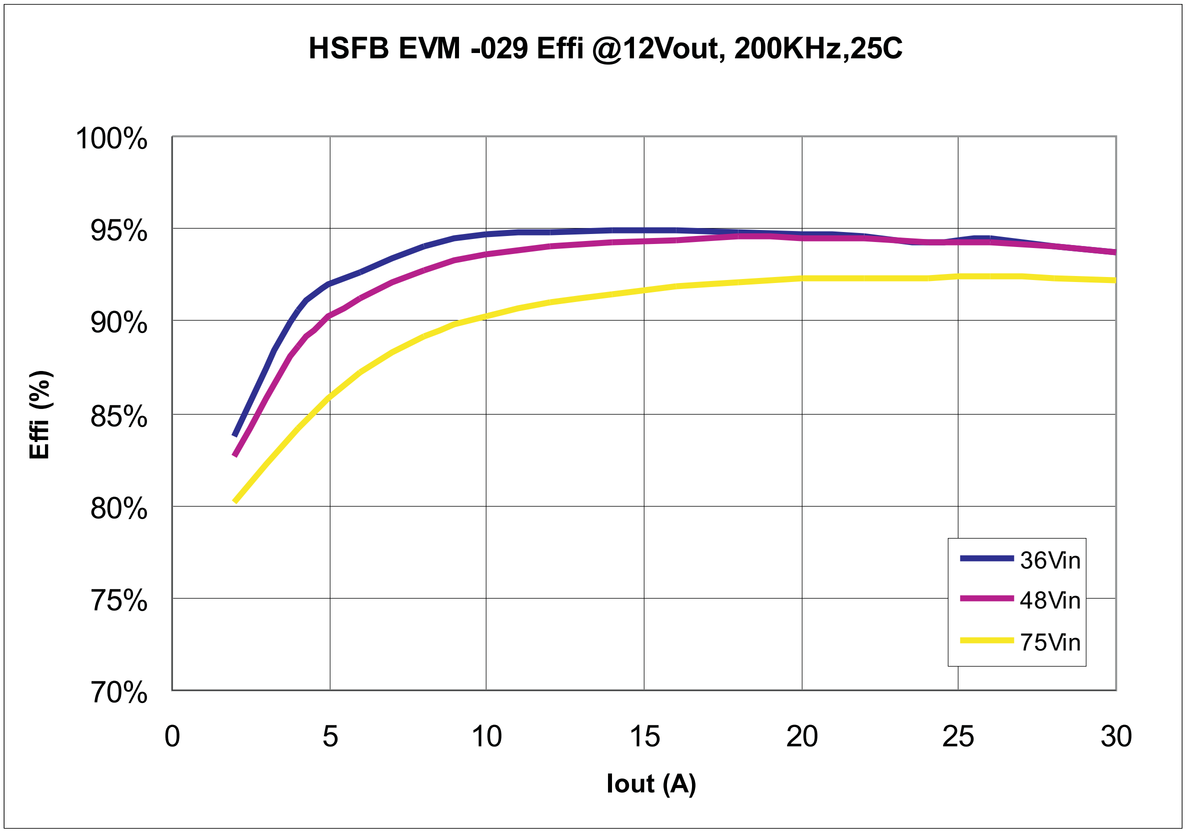


Figure 6. UCD3138HSFBEVM-029 Efficiency

9.2 Load Regulation

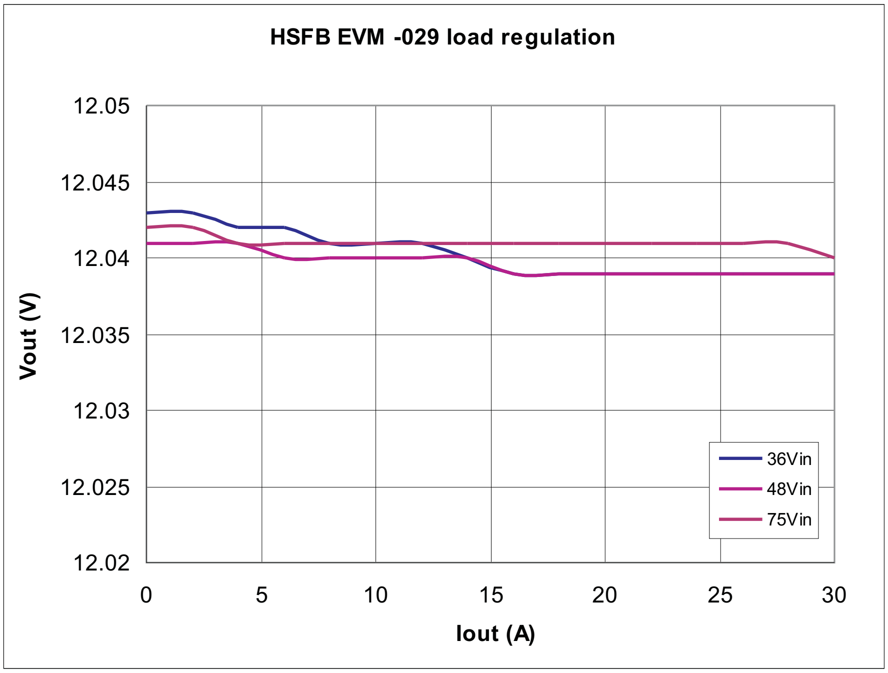


Figure 7. UCD3138HSFBEVM-029 Load Regulation

9.3 Line Regulation

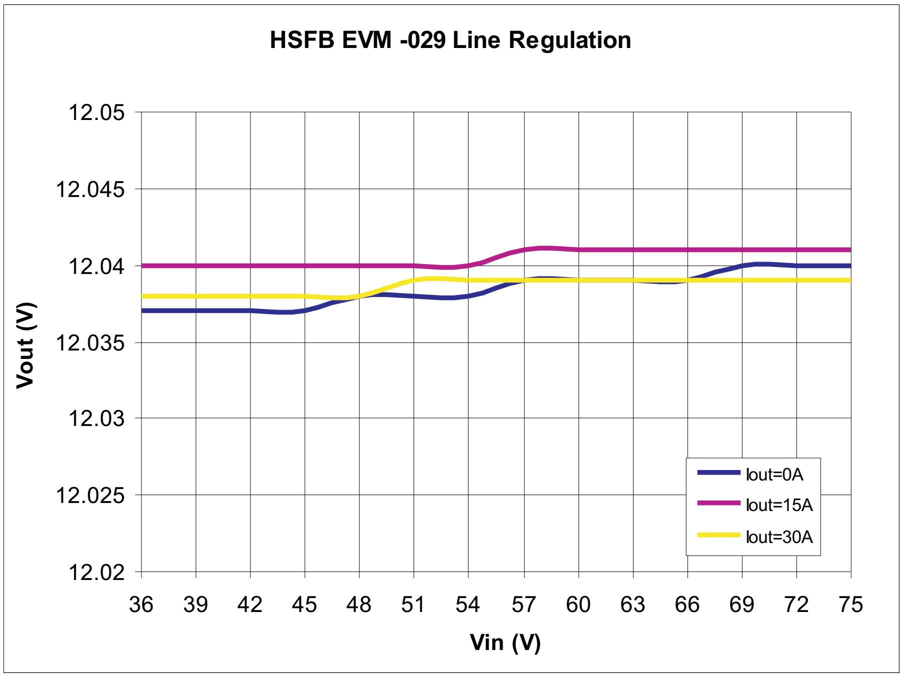


Figure 8. UCD3138HSFBEVM-029 Line Regulation

9.4 Constant Power Constant Current (CPCC)

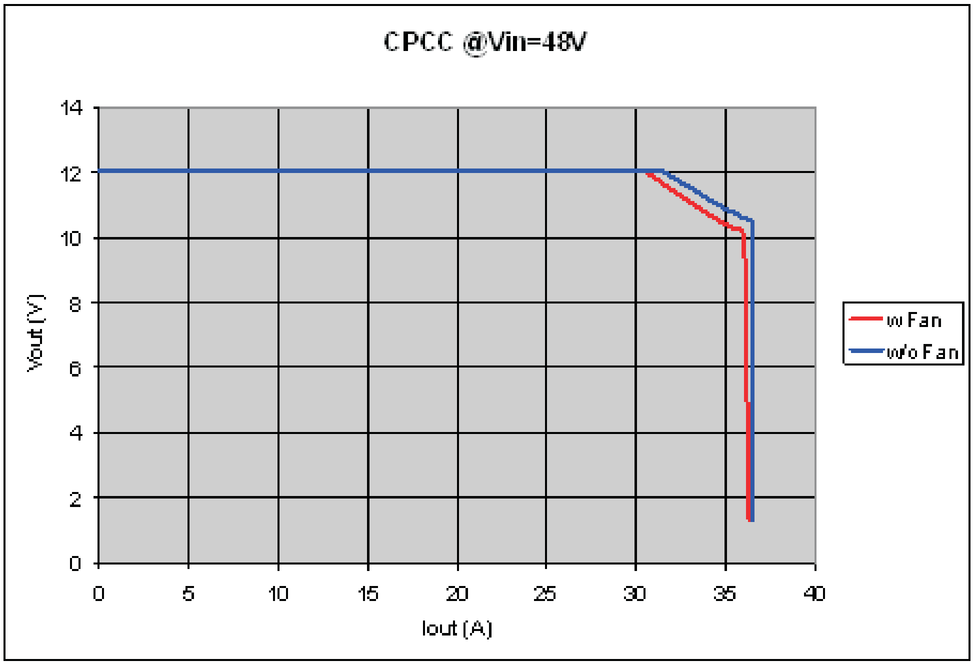


Figure 9. Constant Power Constant Current

9.5 Output Voltage Ripple

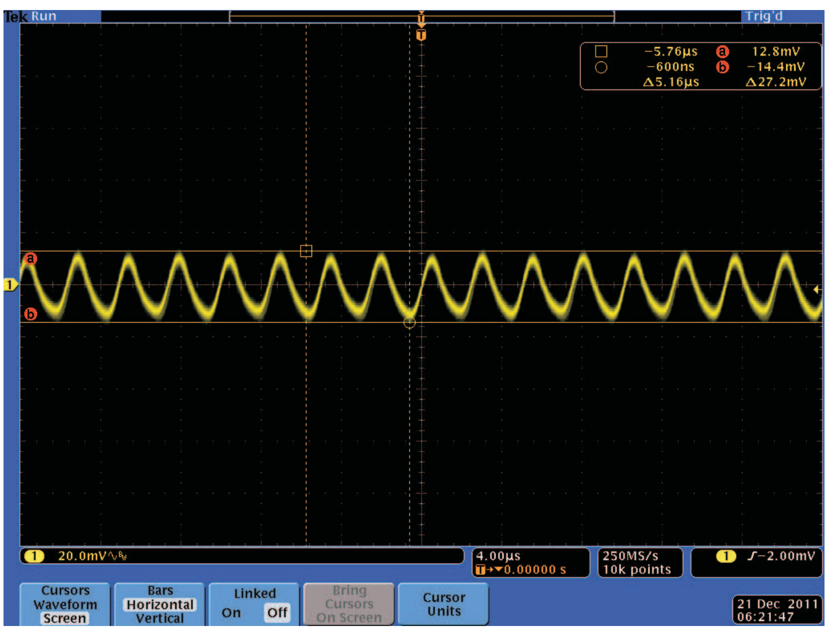


Figure 10. Output Voltage Ripple at 48 V_{DC} and Half Load, 27.2mV

9.6 Output Turn On

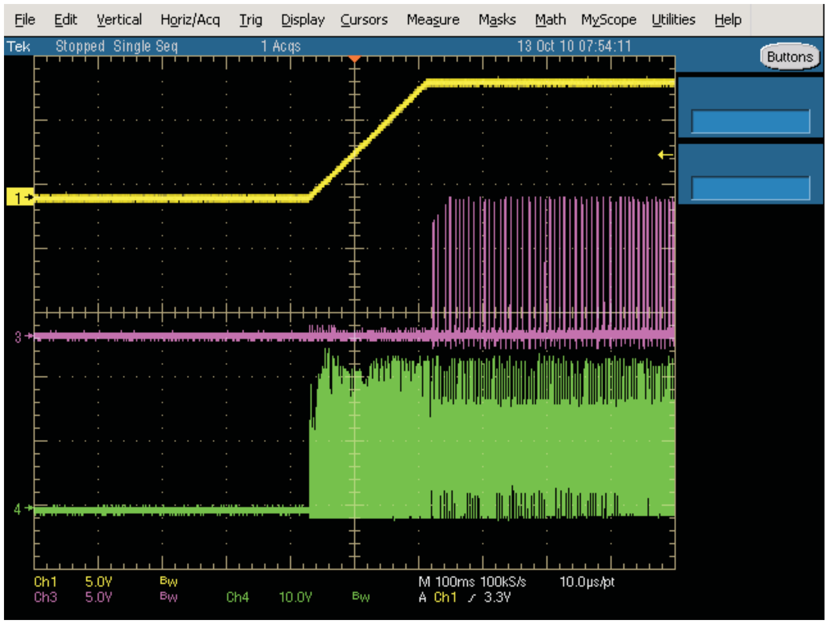


Figure 11. Output Turn On 48 V_{DC} with Load Range (Ch 1 = Vo, Ch 3= DPWM1B, Ch 4 = Vct, load = 1A)

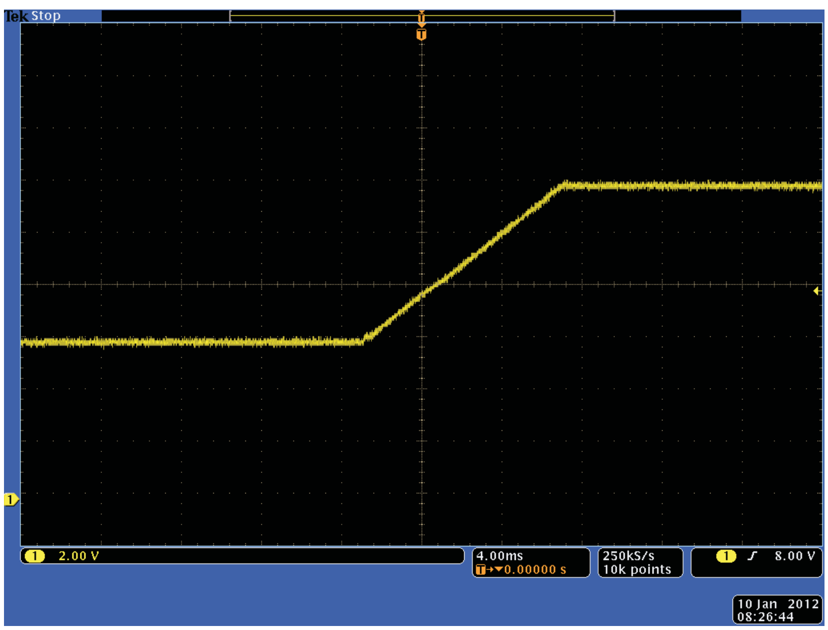


Figure 12. Output Turn On 48 V_{DC} with 6V Prebias

9.7 Bode Plots

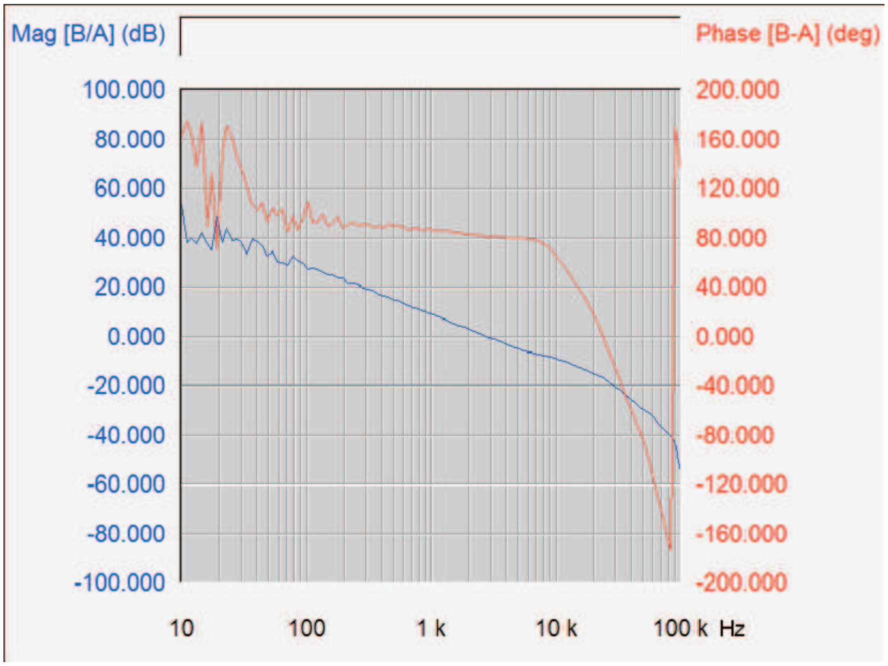


Figure 13. Control Loop Bode Plots at 48 V_{DC} and Half Load

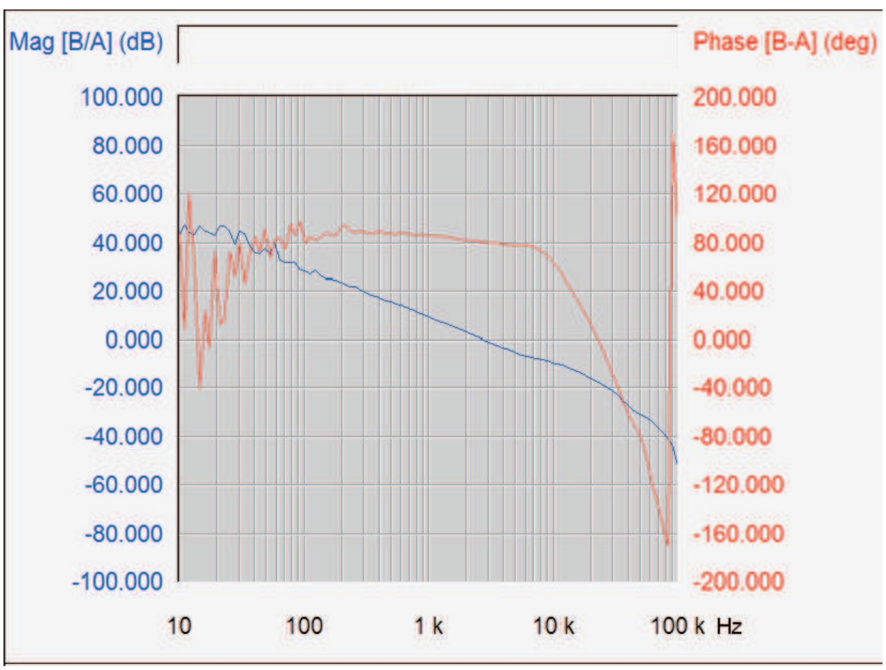


Figure 14. Control Loop Bode Plots at 48 V_{DC} and Full Load

10 EVM Assembly Drawing and PCB Layout

The following figures (Figure 15 through Figure 20) show the design of the UCD3138HSFBEVM-029 printed circuit board. PCB dimensions: L x W = 4.5 x 4.0 in, PCB material: FR4 or compatible, four layers and 2oz copper on each layer

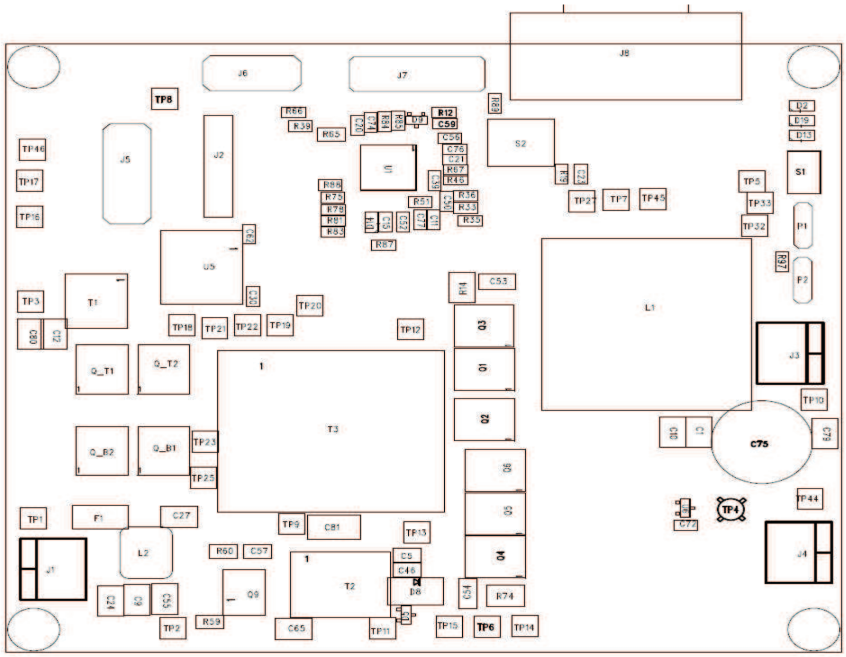


Figure 15. UCD3138HSFBEVM-029 Top Layer Assembly Drawing (top view)

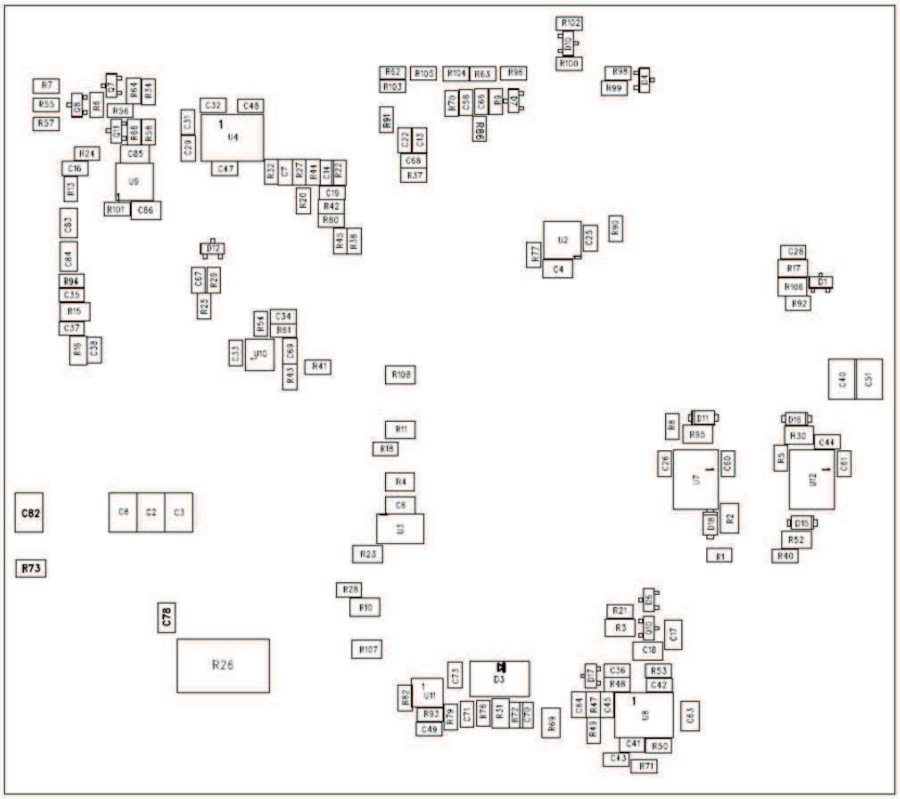


Figure 16. UCD3138HSFBEVM-029 Bottom Assembly Drawing (bottom view)

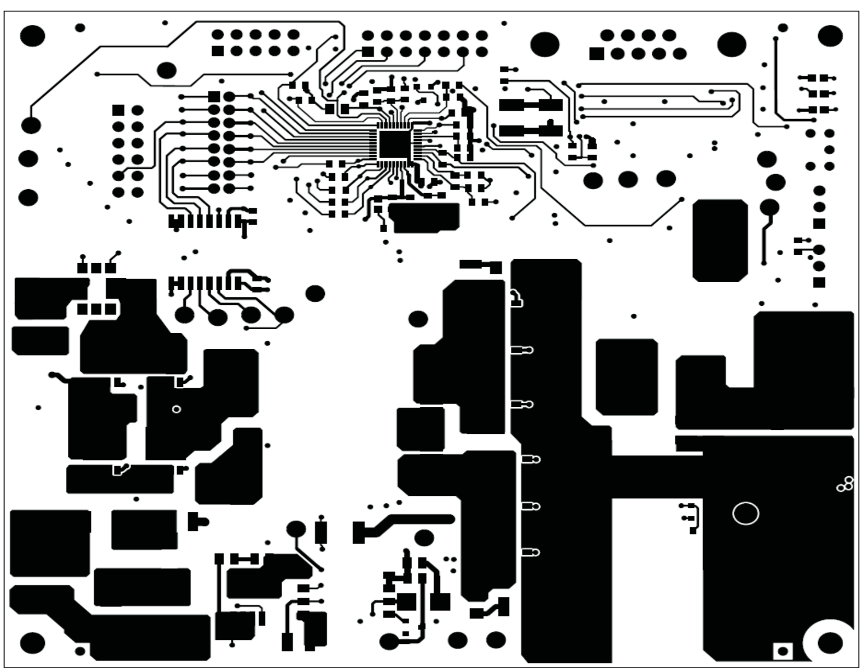


Figure 17. UCD3138HSFBEVM-029 Top Copper (top view)

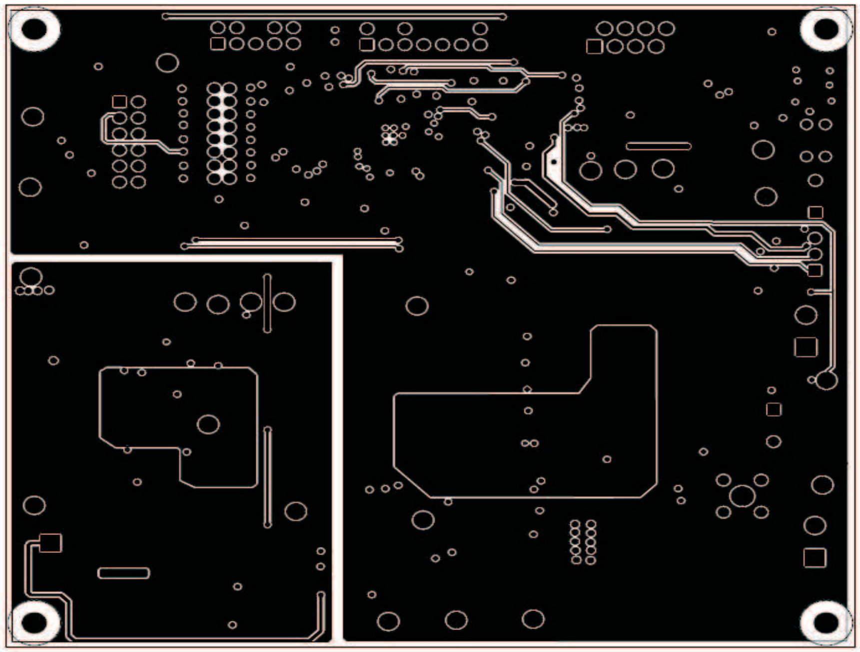


Figure 18. UCD3138HSFBEVM-029 Internal Layer 1 (top view)

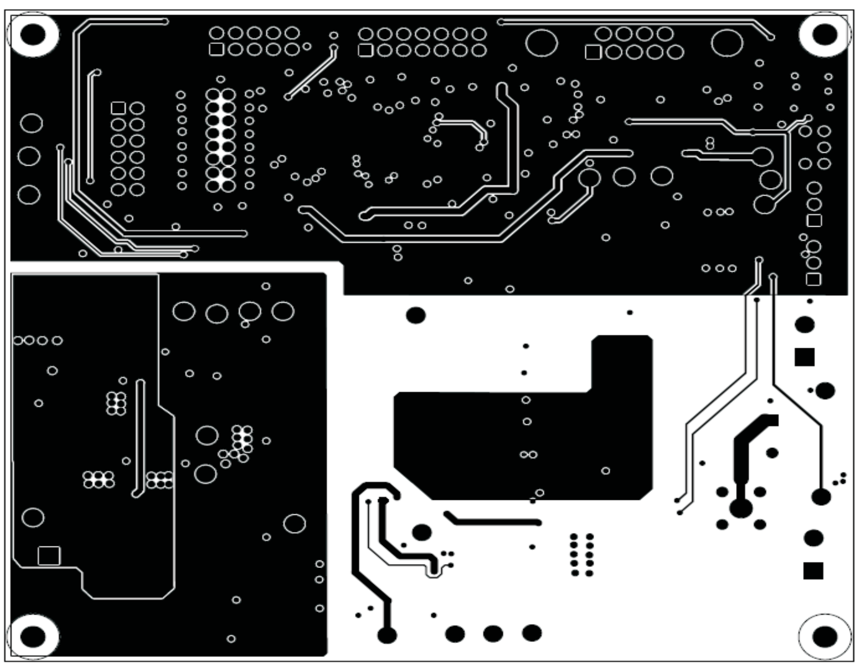


Figure 19. UCD3138HSFBEVM-029 Internal Layer 2 (top view)

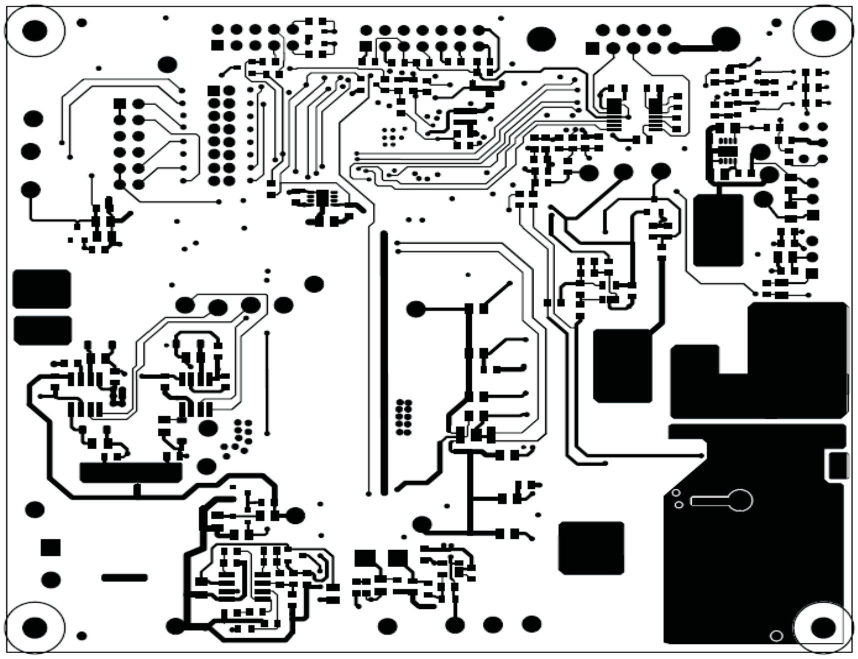


Figure 20. UCD3138HSFBEVM-029 Bottom Copper (top view)

11 List of Materials

Component list based on schematics of Figure 1 though Figure 3.

Table 4. UCD3138HSFBEVM-029 List of Materials

QTY	RefDes	Description	Part Number	MFR
7	C1, C2, C3, C8, C10, C79, C82	Capacitor, ceramic, 16V, X5R, 20%, 47uF, 1210	STD	STD
2	C11, C52	Capacitor, ceramic, 6.3V, X7R, 10%, 2.2uF, 0603	STD	STD
0	C14, C37, C38, C76	Capacitor, ceramic, 50V, X7R, 10%, Open, 0603	STD	STD
5	C19, C21, C56, C58, C59	Capacitor, ceramic, 50V, X7R, 10%, 4700pF, 0603	STD	STD
12	C20, C23, C26, C29, C30, C31, C32, C33, C42, C44, C47, C48	Capacitor, ceramic, 50V, X7R, 10%, 0.1uF, 0603	STD	STD
5	C22, C25, C60, C61, C64	Capacitor, ceramic, 16V, X7R, 10%, 1uF, 0603	STD	STD
1	C28	Capacitor, ceramic, 50V, X7R, 10%, 1nF, 0603	STD	STD
3	C34, C36, C70	Capacitor, ceramic, 50V, NP0, 10%, 47pF, 0603	STD	STD
1	C39	Capacitor, ceramic, 50V, X7R, 10%, 680pF, 0603	STD	STD
2	C4, C85	Capacitor, ceramic, 10V, X5R, 10%, 10uF, 0805	STD	STD
1	C41	Capacitor, ceramic, 50V, X7R, 10%, 330pF, 0603	STD	STD
1	C43	Capacitor, ceramic, 50V, X7R, 10%, 220pF, 0603	STD	STD
4	C49, C66, C69, C74	Capacitor, ceramic, 50V, NP0, 10%, 100pF, 0603	STD	STD
2	C5, C46	Capacitor, ceramic, 16V, X7R, 10%, 2.2uF, 0805	STD	STD
1	C50	Capacitor, ceramic, 50V, X7R, 10%, 1000pF, 0603	STD	STD
2	C53, C54	Capacitor, ceramic, 100V, X7R, 10%, 1000pF, 1206	STD	STD
1	C57	Capacitor, ceramic, 200V, NP0, 10%, 47pF, 0805	STD	STD
7	C6, C17, C18, C78, C83, C84, C86	Capacitor, ceramic, 16V, X7R, 10%, 1uF, 0805	STD	STD
2	C62, C73	Capacitor, ceramic, 16V, X7R, 10%, 100nF, 0603	STD	STD
1	C63	Capacitor, ceramic, 16V, X7R, 10%, 4.7uF, 0805	STD	STD
1	C65	Capacitor, ceramic, 100V, X7R, 10%, 1uF, 1210	STD	STD
2	C67, C68	Capacitor, ceramic, 50V, NP0, 10%, 10pF, 0603	STD	STD
9	C7, C13, C15, C16, C35, C45, C71, C72, C77	Capacitor, ceramic, 50V, X7R, 10%, 10nF, 0603	STD	STD
1	C75	Capacitor, Electrolytic, 16V, 20%, 1000uF, 12.5 x 20.00 mm	EEU-EB1C102	Panasonic
1	C81	Capacitor, ceramic, 2000V, X7R, 10%, 4.7nF, 1812	STD	STD
8	C9, C12, C24, C27, C40, C51, C55, C80	Capacitor, ceramic, 100V, X7R, 10%, 2.2uF, 1210	STD	STD
2	D1, D5	Diode, fast switching, 100V, SOT23	MMBD914LT1G	Fairchild
4	D11, D15, D16, D18	Diode, Schottky, 40V, 0.5A, SOD-123	MBR0540T1G	On Semi
2	D14, D19	LED, 565NM, green DIFF, 0603	SML-LX0603GW	LUMEX
1	D17	Diode, small-signal, 85V, 200MA, SOT23	BAW56-V-GS08	Vishay-Liteon
2	D2, D13	LED, 660NM, super red diff, 0603	SML-LX0603SRW	Lite On
2	D3, D8	Diode, Schottky, 2A, 40V, SMB	SS24T3G	ON SEMI
2	D4, D10	Diode,TVS Zener dual, 300W, 5V, SOT23	SM05T1G	ON SEMI
1	D6	Diode, Zener, 225MW, 5.6V, SOT-23	BZX84C5V6-T1G	ON SEMI
3	D7, D9, D12	Diode, dual switch, 100V, SOT23	MMBD7000LT1G	ON SEMI
1	F1	FUSE 15A 86 V_{DC} fast 6125FA, 15A 86V, 2410	TR2/6125FA15A	Cooper

Table 4. UCD3138HSFBEVM-029 List of Materials (continued)

3	J1, J3, J4	2 position 5mm terminal block, TB 2X5mm, 0.40 x 0.35 inch	ED350/2	OST
1	J2	Header 16 position 2mm, header 2mm 16 pos	PRPN062PAEN-RC	Sullins
1	J5	Header 12 position 100mil, header 0.1 12 POS", 0.100 inch x 2X6	PEC06DAAN	Sullins
1	J6	Shrouded header 10 pos straight, header 100-2x5 shroudedheader 100-2x5 shrouded0.100 inch x 5 x 2	N2510-6002-RB	Sullins
0	J7	Conn hdr dual 14pos .100 SRT AU, open, 0.100 inch x 2x7	PEC07DAAN	Sullins
1	J8	Connector, 9-pin D, right angle, female, 1.213 x 0.510	182-009-213R171	Norcomp
1	L1	Inductor, power, 35A, 2.2uH, 1.100 x 1.100 inch	SER2814H-222KL	Coilcraft
1	L2	Inductor, power, 16A, 470nH, 0.255 x 0.270 inch	IHLP2525CZERR47M01	Vishay
2	P1, P2	Conn header 3pos .100 vert tin, 3 pin polarized header, 0.100 inch x 3	22-27-2031	Molex
4	Q_B1, Q_B2, Q_T1, Q_T2	MOSFET, N-channel, 100V, 60A, 8mohm, QFN	FDMS86101	Fairchild
6	Q1, Q2, Q3, Q4, Q5, Q6	MOSFET, N-channel, 100V, 60A, 8mohm, QFN	FDMS86101	Fairchild
4	Q7, Q8, Q10, Q11	Transistor, NPN, 350mW, 200mA, 40V, SOT23	MMBT3904	FAIRCHILD
1	Q9	MOSFET, N-channel, 200V, 3A, S08	FDS2670	Fairchild
16	R1, R5, R6, R8, R18, R19, R24, R28, R40, R62, R63, R64, R68, R96, R103, R104	Resistor, chip, 1/10W, 1%, 10.0k, 0603	STD	STD
1	R101	Resistor, chip, 1/10W, 1%, 1, 0603	STD	STD
2	R14, R74	Resistor, chip, 1/3W, 1%, 20, 1210	STD	STD
2	R15, R16	Resistor, chip, 1/8W, 1%, 15, 0805	STD	STD
0	R17	Resistor, chip, 1/8W, 1%, Open, 0805	STD	STD
5	R2, R30, R52, R95, R106	Resistor, chip, 1/8W, 1%, 10, 0805	STD	STD
1	R21	Resistor, chip, 1/10W, 1%, 6.49k, 0603	STD	STD
5	R22, R46, R51, R91, R105	Resistor, chip, 1/10W, 0, 0603	STD	STD
4	R25,R32,R76,R82	Resistor, chip, 1/10W, 1%, 49.9k, 0603	STD	STD
0	R26	Resistor, current sense , 3W, 1%, open, 0.394 x 0.205 inch	BVS-M-R001-1.0	Isotek
0	R27, R38, R39, R44, R45, R66, R75, R78, R81, R83, R86, R88, R89, R90, R94	Resistor, chip, 1/10W, 1%, open, 0603	STD	STD
1	R29	Resistor, chip, 1/10W, 1%, 2.00k, 0603	STD	STD
1	R3	Resistor, chip, 1/8W, 1%, 200, 0805	STD	STD
1	R31	Resistor, chip, 1/8W, 1%, 1.00k, 0805	STD	STD
1	R33	Resistor, chip, 1/10W, 1%, 1.74k, 0603	STD	STD
3	R34, R56, R58	Resistor, chip, 1/10W, 1%, 3.32k, 0603	STD	STD
2	R35, R85	Resistor, chip, 1/10W, 1%, 16.2k, 0603	STD	STD
1	R36	Resistor, chip, 1/10W, 1%, 1.62k, 0603	STD	STD
6	R4, R10, R11, R23, R107, R108	Resistor, chip, 1/8W, 1%, 1, 0805	STD	STD
1	R42	Resistor, chip, 1/10W, 1%, 3.09k, 0603	STD	STD
1	R47	Resistor, chip, 1/10W, 1%, 15.0k, 0603	STD	STD
2	R48, R53	Resistor, chip, 1/10W, 1%, 22.1k, 0603	STD	STD

Table 4. UCD3138HSFBEVM-029 List of Materials (continued)

1	R49	Resistor, chip, 1/10W, 1%, 4.99k, 0603	STD	STD
5	R50, R98, R99, R100, R102	Resistor, chip, 1/10W, 1%, 33.2, 0603	STD	STD
1	R54	Resistor, chip, 1/10W, 1%, 1.50k, 0603	STD	STD
1	R59	Resistor, chip, 1/8W, 1%, 3.01, 0805	STD	STD
1	R60	Resistor, chip, 1/8W, 1%, 750, 0805	STD	STD
1	R61	Resistor, chip, 1/10W, 1%, 137k, 0603	STD	STD
1	R65	Resistor, chip, 1/8W, 1%, 1.65k, 0805	STD	STD
1	R67	Resistor, chip, 1/10W, 1%, 51.1k, 0603	STD	STD
1	R69	Resistor, chip, 1/8W, 1%, 90.9k, 0805	STD	STD
4	R7, R13, R55, R57	Resistor, chip, 1/10W, 1%, 499, 0603	STD	STD
1	R72	Resistor, chip, 1/10W, 1%, 10, 0603	STD	STD
1	R73	Resistor, chip, 1/8W, 0, 0805	STD	STD
1	R77	Resistor, chip, 1/10W, 1%, 0.47, 0603	STD	STD
1	R79	Resistor, chip, 1/10W, 1%, 150k, 0603	STD	STD
1	R80	Resistor, chip, 1/10W, 1%, 1.18k, 0603	STD	STD
1	R84	Resistor, chip, 1/10W, 1%, 1.82k, 0603	STD	STD
1	R87	Resistor, Chip, 1/10W, 1%, 301, 0603	STD	STD
8	R9, R12, R20, R37, R41, R43, R70, R71	Resistor, chip, 1/10W, 1%, 1.00k, 0603	STD	STD
1	R92	Resistor, chip, 1/10W, 1%, 2.49k, 0603	STD	STD
1	R93	Resistor, chip, 1/10W, 1%, 20.0k, 0603	STD	STD
1	R97	Resistor, chip, 1/10W, 1%, 220, 0603	STD	STD
1	S1	Switch, on-on mini toggle, SPDT 28V 0.4A, 0.28 x 0.18 inch	G12AP	NKK
1	S2	Switch, SPST, PB momentary, sealed washable, 0.245 X 0.251	KT11P2JM34LFS	C & K
1	T1	SMT 100:1 current sense XFMR, 100:01:00, 0.284 x 0.330 inch	PA1005.100	Pulse
1	T2	Transformer, aux. flyback ±10%, 540 uH, 0.400 x 0.480 inch	031-00019	XFMRS Inc
1	T3	Power XFMR 400W 5:2:2, 26x29.5 mm	755044	Payton
29	TP1, TP2, TP3, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP25, TP27, TP32, TP33, TP44, TP45, TP46	Test point, white, thru hole, 5012, 0.125 x 0.125 inch	5012	Keystone
1	TP4	Adaptor, 3.5-mm probe clip (or 131-5031-00), 0.200 inch	131-4244-00	Tektronix
1	U1	UCD3138RHA, Digital Power Controllers, QFN	UCD3138RHA	TI
1	U10	OPA344, MIC OP AMP RRIO, SOT23-5	OPA344NA/250	TI
1	U11	TLV2371, OP AMP 3MHZ RRIO, SOT23-5	TLV2371IDBVR	TI
2	U2, U9	TPS715A33, LDO REG, QFN-8	TPS715A33DRBT	TI
1	U3	UCC27524, Dual HS MOSFET Driver, 5A, HTSSOP	UCC27524DGN	TI
1	U4	SN65C3221, LINE DRVR/RCVR 1CH, TSSOP-16	SN65C3221PWR	TI
1	U5	QISO7240CF, UAD CHANNEL 25 MBPS DIGITAL ISOLATOR, SO-16	ISO7240CFDWR	TI
1	U6	LM60C, Temp Sensor, SOT-23	LM60CIM3X	TI
2	U7, U12	UCC27211, HIGH/LOW SIDE DRIVER, 4A, SO8	UCC27211D	TI

Table 4. UCD3138HSFBEVM-029 List of Materials (continued)

1	U8	UCC3813D-1, LOW-PWR CUR-MODE PWM, SO8	UCC3813D-1	TI

Appendix A 12 Digital Full-Bridge Converter Description

A.1 Converter Block Diagram

Figure 21 shows the converter block diagram used in the EVM. The signals used for control and for detection are also defined in Figure 21 in connection to the UCD3138 pins which are listed in Section 12.2 and Figure 22 as well.

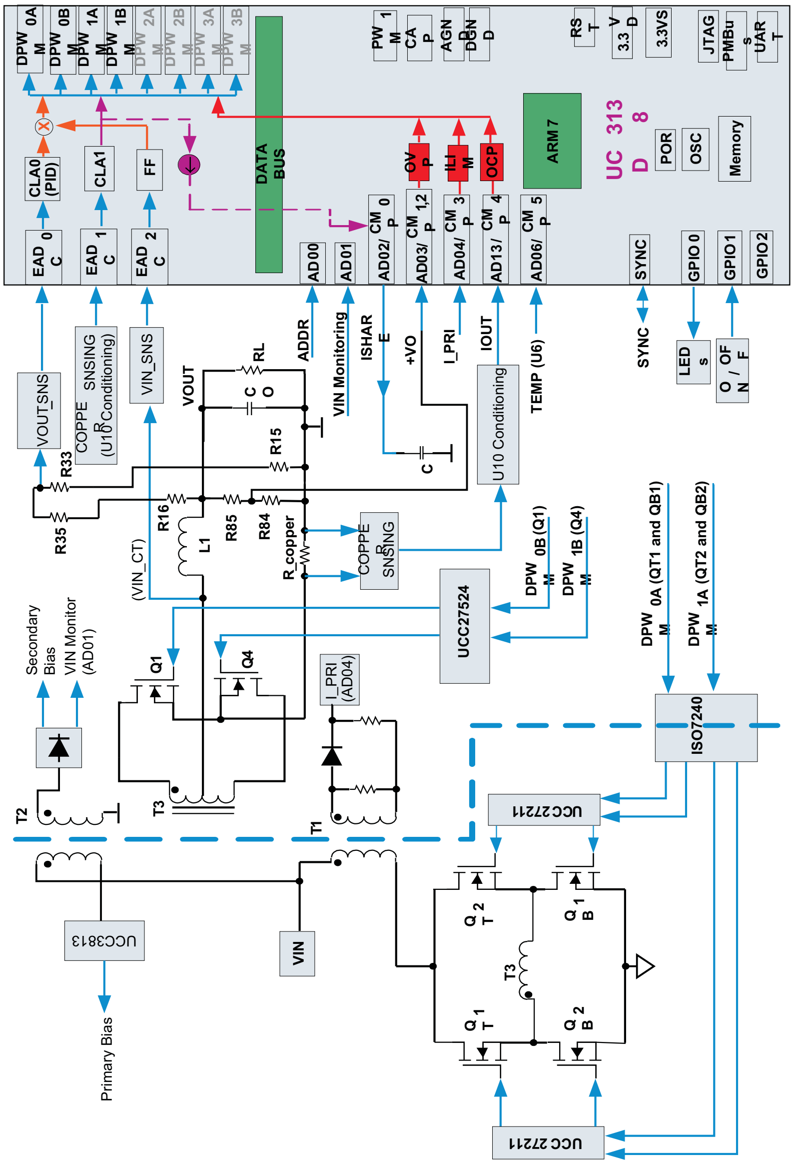


Figure 21. Converter Block Diagram and Pin Definitions

A.2 UCD3138 Pin Definition

The definition of each UCD3138 pin is defined as shown in Figure 21. The definitions shown in Figure 22 are for these pins used in the EVM to make full-bridge converter control. It can be found in Figure 21 how the signals on these pins are used in the converter in this EVM.

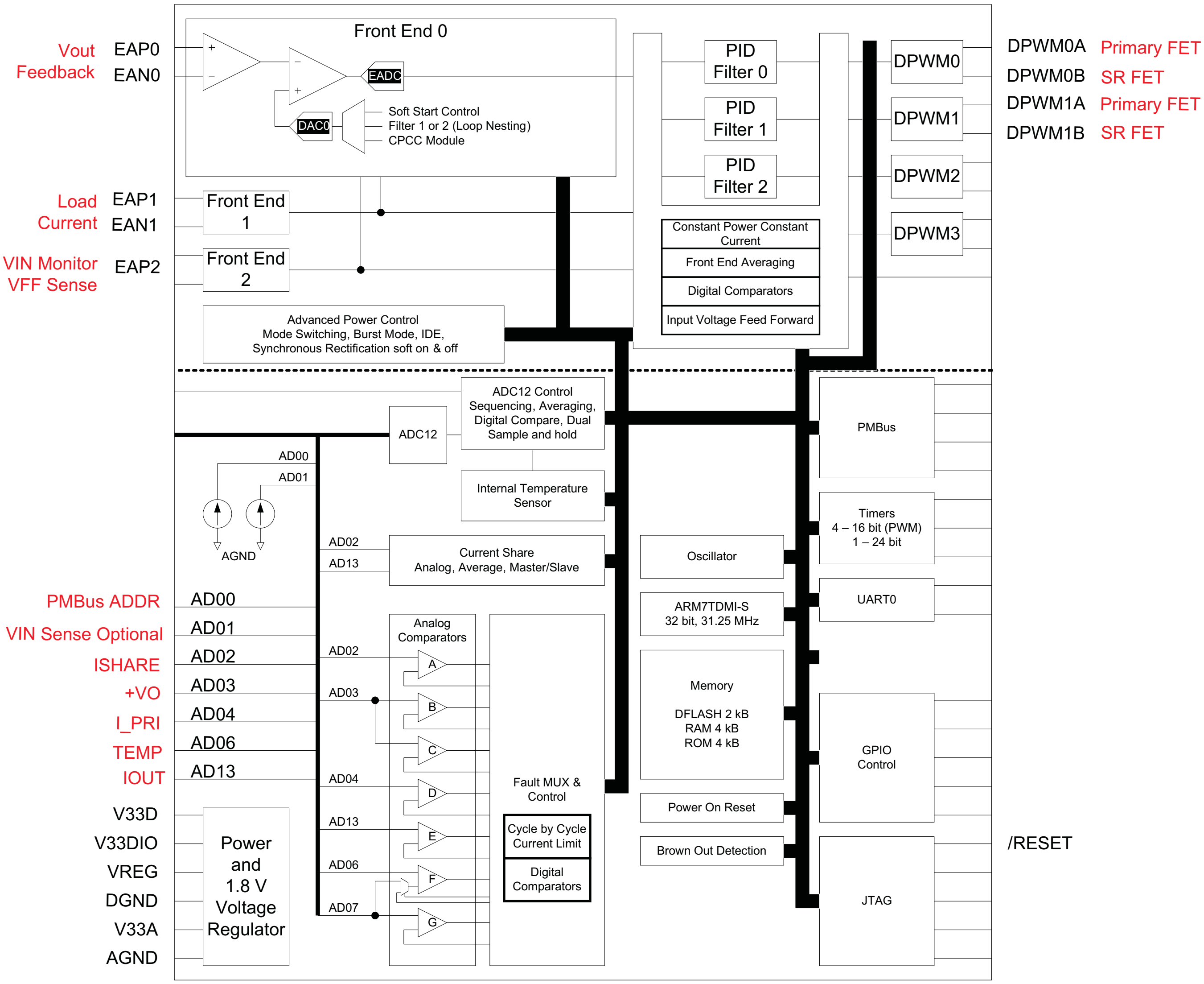


Figure 22. UCD3138 Pin Definition in Hard Switching Full-Bridge Control

A.3 12.3 EVM Hardware – Introduction

In this section, the EVM hardware functions are described.

A.3.1 Power Stage

This EVM implements a traditional symmetrical hard switching full-bridge dc-dc converter topology. The power stage circuit is shown in Figure 23. The complete schematics are shown in Figure 1 through 3. The main power components on the primary side, Q_T1, Q_T2, Q_B1, and Q_B2 form the MOSFET full-bridge converter. These four FETs are controlled by the UCD3138 DPWM module 0 (DPWM0A) and module 1(DPWM1A). The controller, UCD3138, is located on the secondary side. The driver signals to these four FETs are through digital isolator U5 to transmit from the secondary side to the primary side. The synchronous rectifiers are shown on the same page and are labeled as Q1 to Q3 and Q4 to Q6. They are controlled by DPWM module 0 (DPWM0B) and DPWM module 1 (DPWM1B). Please refer to Figure 22 for DPWM module 0 and 1. The main power transformer is T3. T1 is the current transformer used to sense the primary side current and feed into the secondary side UCD3138 controller through AD04.

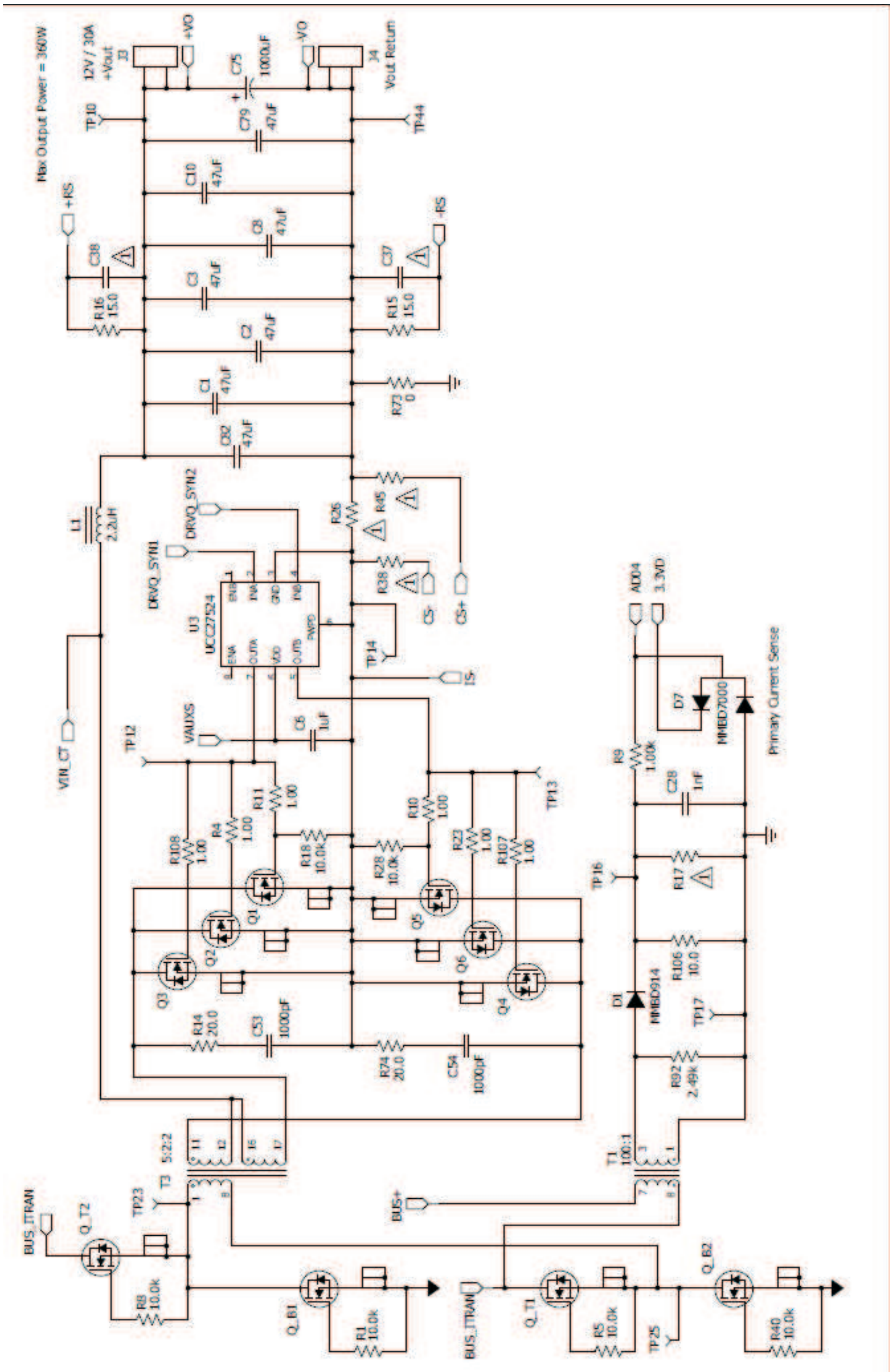


Figure 23. Full-Bridge Converter Power Stage

A.3.2 Bias Power Supply

The main bias supply is a flyback converter using the UCC3813 controller from Texas Instruments. The bias circuit is shown in Figure 24.

In this circuit, one output (VAUXPRI) is on the primary side and two outputs (VAUXS and 6V_UR) are on the secondary side. The feedback signal is taken from VAUXPRI. The secondary side controller needs +3.3V, which is derived from 6V_UR by a regulator (U2) to supply UCD3138 and by a regulator (U9) to supply digital isolator (U5), external temperature sensor (U6) and UART controller (U4). On the primary side a 5V-LDO is to supply the digital isolator to transmit drive signals from the secondary side to the primary side. The three LDO associated bias circuits are shown in Figure 25.

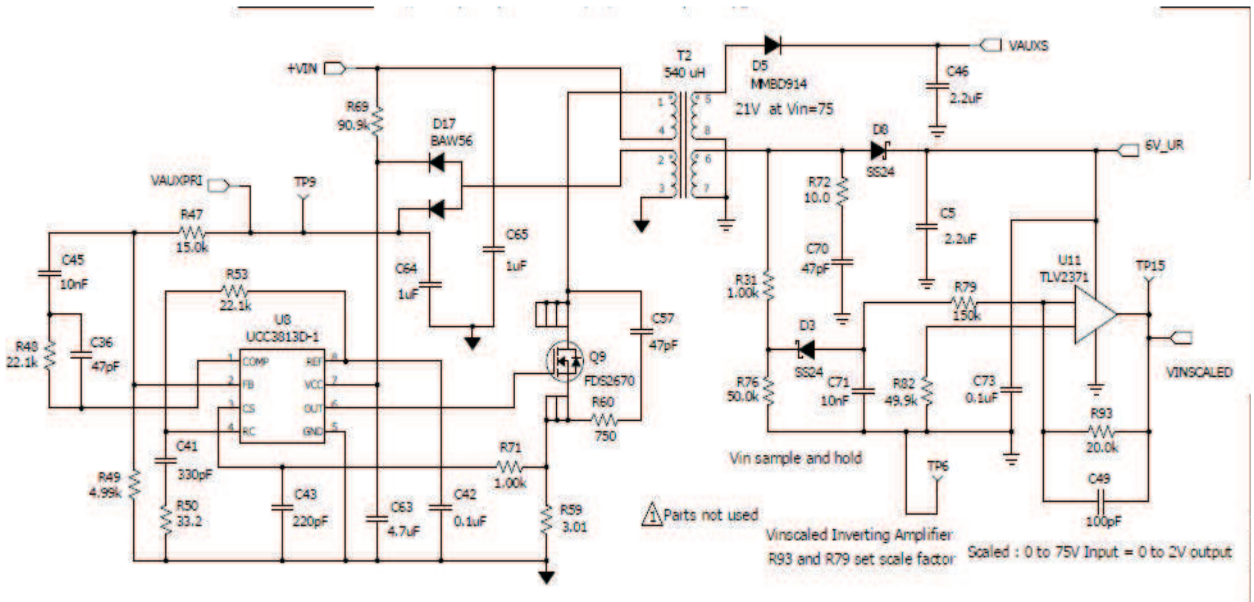


Figure 24. Main Bias Circuit and Input Voltage Optional Monitoring

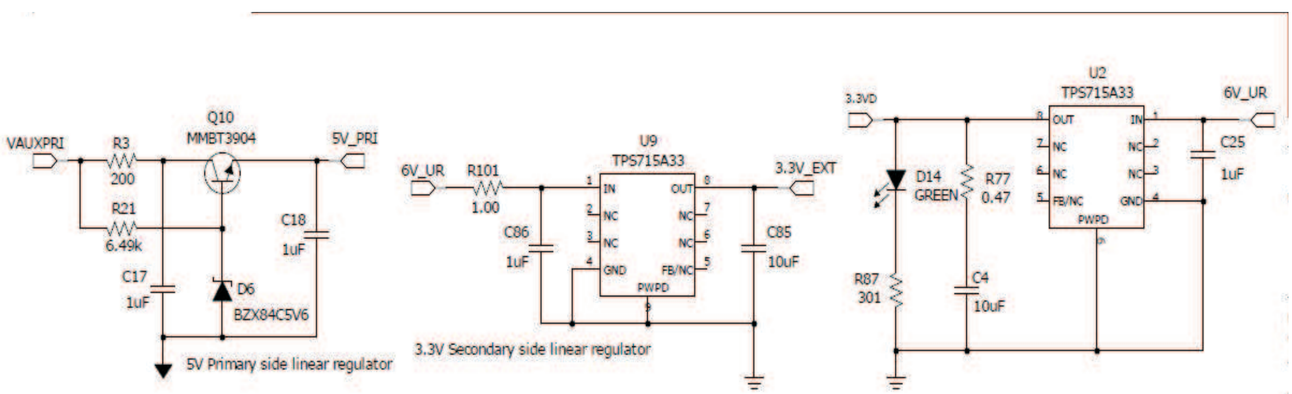


Figure 25. LDO Bias Circuits

A.3.3 Input Voltage Sensing Using Bias Transformer

As the controller is located on the secondary side, special approaches are required to obtain the input voltage information from the primary side for control needs. One approach is to use the main bias power supply transformer winding.

As shown in Figure 24, a sample-and-hold circuit is on the secondary side to sense the primary voltage. When switch Q9 turns on, D3 turns on by the negative voltage from divider R31 and R76. The voltage on the winding (6, 7) of bias transformer T2 charges capacitor (C71) to a negative voltage equal to Vin/N times the attenuator ratio of R31 and R76, (N is turns ratio of T2). When Q9 is turned off, D3 is turned off, and the voltage on C71 is held until next switching period. The voltage on C71 is proportional to the input voltage. U11 is used to invert the input negative voltage to positive output voltage scaled by R93 and R79. This input voltage monitoring approach is an optional for potential applications while not enabled in the EVM firmware.

A.3.4 Input Voltage Sensing Using Main Transformer

The sensing approach described in Section 12.3.3 is good to use in steady-state but not capable of fast transient sensing. This approach presents slow detection and slow response. Its advantage is less noise sensitive.

To improve input voltage sensing speed in real time, the main power transformer can be used. As shown in Figure 26, the approach takes the input voltage signal (VIN_CT) from the center tap of the main transformer secondary side windings, then scaling the signal to feed into UCD3138 EADC02. This EVM uses this sense structure when the converter is in startup, in steady-state, as well as in input voltage feed forward control. Particularly when use this structure for converter startup, the approach is called single-frame input voltage sensing. Single-frame here means one switching cycle. More details on how the main transformer is used to make input voltage sense can be found in Section 12.5.

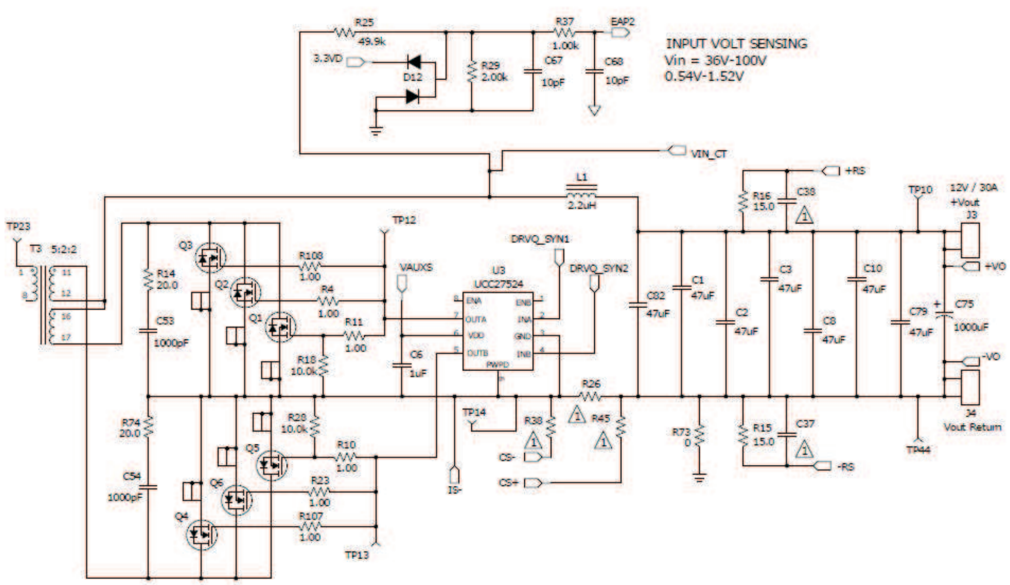


Figure 26. Input Voltage Sensing Using Main Transformer

A.3.5 Load Current Sensing by PCB Copper

To utilize the board area, this EVM uses copper trace (R26) to sense the output load current. The copper sensing related circuit is shown in Figure 27X. R41 and R43 are installed to feed the sensing signal to the current amplifier U10. With a low pass filter (C7, R54 and R20), the output voltage of the amplifier is of DC voltage in nature. The signal is then fed to AD13 of the controller. The amplifier gain can be set to 137 by choosing R41 =R43 =1k, R61 =137k.

AD13 is used to sense the load current , then the processor utilize the information for many applications, such as reporting the current to the host, calculating output power, implementing current sharing and over current protection.

The accuracy of sensing current with a copper trace is usually poor because the resistance of copper trace depends not only on the base copper thickness and plating, but also on the temperature of the copper. The base copper has a temperature coefficient of about 4000 PPM per degree C. Fortunately, the resistance can be measured and stored during manufacturing, and the temperature of the copper trace can be measured to compensate for temperature drift. The temperature of the copper trace is measured by a temperature sensor U11 (LM60C) then feed into UCD3138 through AD06. Please refer to Section 12.6.7 for temperature sensing.

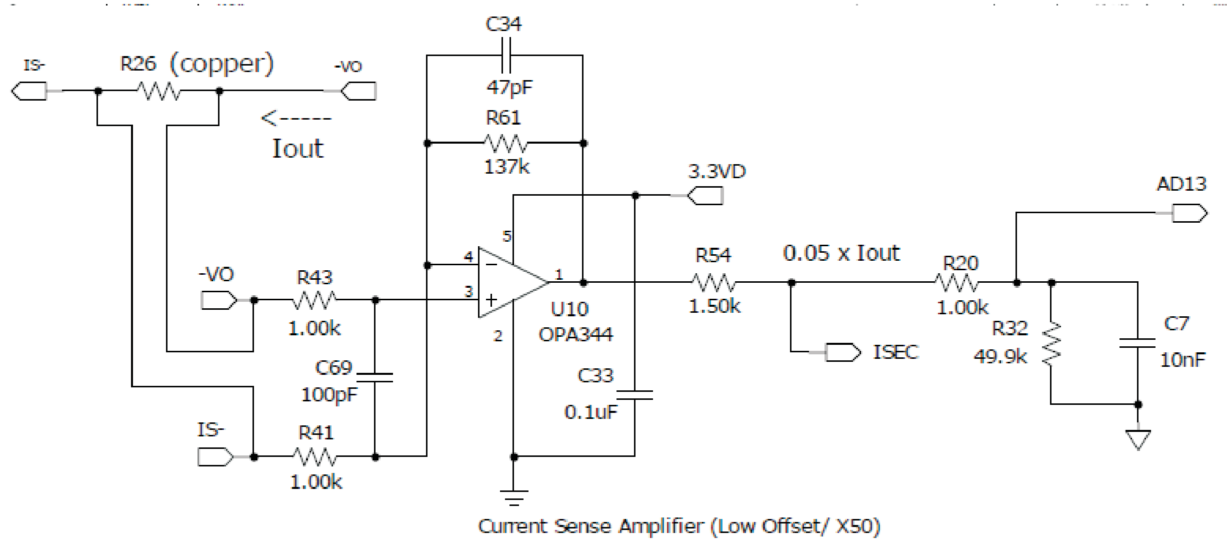


Figure 27. Load Current Sensing by PCB Copper

A.3.6 Load Current Sharing

UCD3138 supports three major current sharing techniques:

- Average Current Sharing, or PWM Bus Current Sharing
- Master/Slave Current Sharing,
- Droop Mode Current Sharing, or Analog Bus Current Sharing

This EVM uses the average current sharing. If interested in the other two sharing techniques, please contact TI for further assistance.

The average current sharing technique uses a share bus to balance and evenly distribute current on each paralleled converter. The share bus is called ISHARE in this EVM design. Hence, when making load current sharing, ISHARE from each board requires connecting together. ISHARE connection is located on P2 terminal pin 3 on the EVM board.

Figure 28 shows the load sharing module inside UCD3138. When enable the average current sharing, SW1 turns on. The ISHARE bus is on AD02 output which generates a voltage corresponding to the load current of that board. As all boards in share connected together by each of their own ISHARE, the voltage on EXT CAP (C19) is an averaged value representing a targeted sharing value for each converter output current. AD13, is used to measure the load current of each board in voltage, then compare to the voltage on ISHARE to adjust one's own output current level to match the targeted ISHARE value by DPWM duty cycle control.

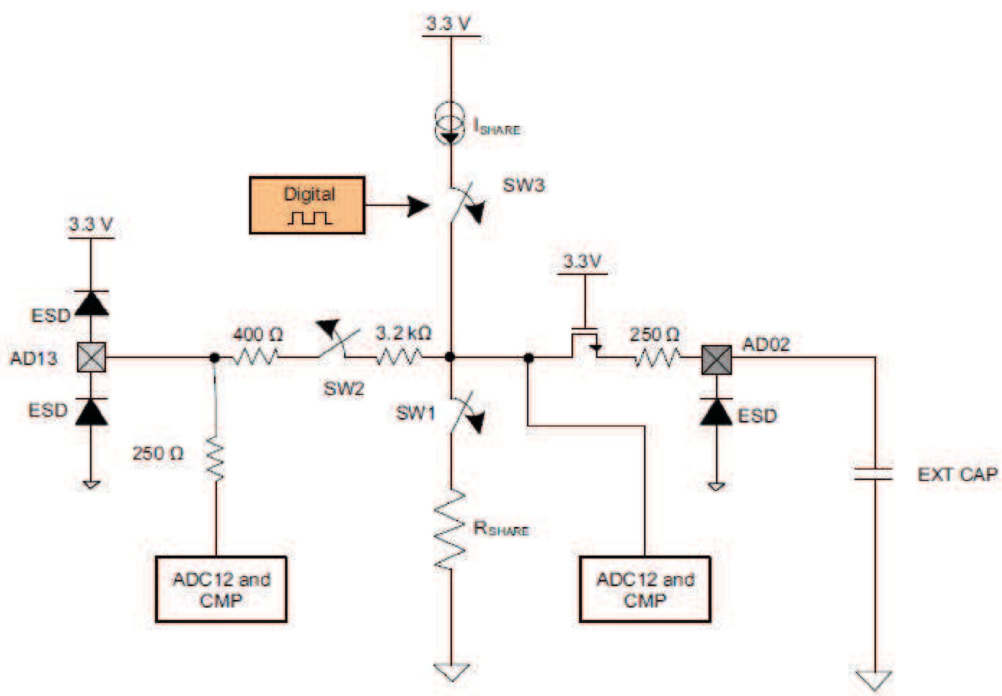


Figure 28. UCD3138 Load Sharing Module

A.3.7 Serial Port Interface

The schematic of the interface for the serial port (UART) is shown in Figure 29. The UART is able to provide real time debug and subsequently reduce code development time. It can also be used as a monitor for fast changing internal variables. The UART is not enabled in delivered EVM boards. Please contact TI to find how to enable this function.

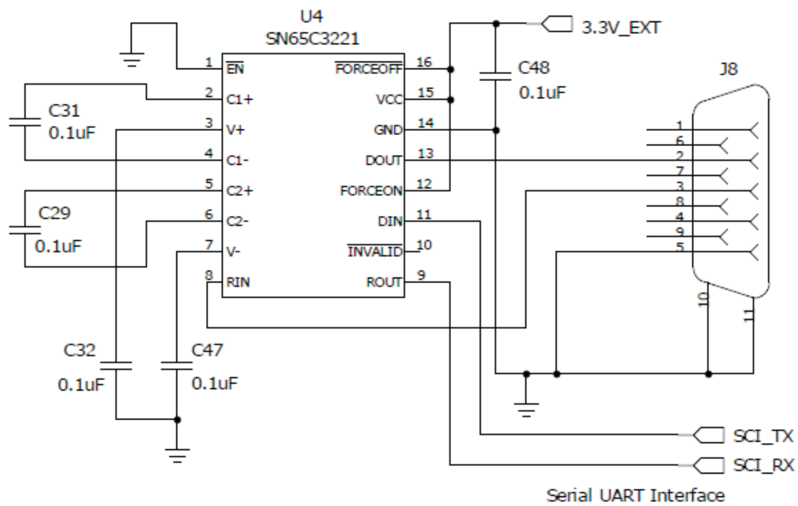


Figure 29. Serial Port Interface in the Converter

A.3.8 LED Indicators

Table 5. LED Status Lights

REF DES	SILK SCREEN TEXT	FUNCTION
D14		This light is on in green when 3.3VD is present on UCD3138.
D13	VIN_OK	This light is on in red when input voltage ok.
D2	FAILURE	This light is on in red when latch-off fault(s) present, currently OVP only.
D19	P_GOOD	This light is on in green when the output voltage is within the thresholds defined by PMBUS_CMD_POWER_GOOD_ON and PMBUS_CMD_POWER_GOOD_OFF

A.4 EVM Firmware – Introduction

The reference firmware provided along with the EVM is only intended to demonstrate basic HSFB converter control functionality as well as basic PMBus communication. The firmware can be used as an initial platform for particular applications. A brief introduction to the firmware is provided in this section.

A.4.1 Firmware Infrastructure Overview

The firmware includes one startup routine and three program threads. The startup routine is to make initialization to set up the controller to the targeted operation functions or status. Please contact TI to obtain the detailed initialization information.

The three program threads are (a) the Fast Interrupt (FIQ); (b) the Standard Interrupt (IRQ); and (c) the Background Loop, as shown in Figure 30.

- Fast Interrupt (FIQ)
  - Critical or time sensitive tasks are within the FIQ. Functionally, FIQ events are the highest priority and are addressed as soon as possible. It occurs every 4 switching- cycles, set by DPWM interrupt.
- Standard Interrupt (IRQ)
  - The majority of the firmware tasks occur during the IRQ. IRQ events occur synchronously every 100 µs set by timer.
- Background Loop
  - Non time sensitive tasks are implemented in background loop. Background Loop items are addressed whenever FIQ and IRQ events are not handled.

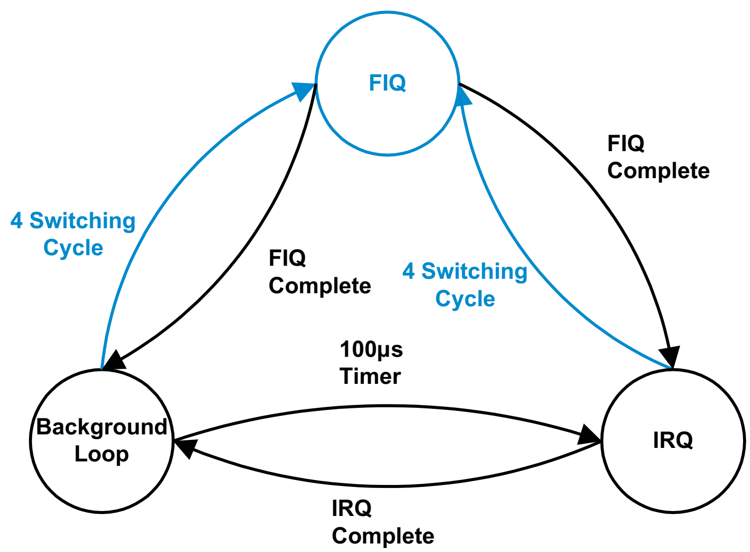


Figure 30. Firmware Structure Overview

A.4.2 Tasks within FIQ

The FIQ events are with the highest priority and are addressed as soon as possible. Critical or time sensitive tasks are in the FIQ. In the firmware uploaded into the EVM, the function called by the FIQ is Constant Power and Constant Current function.

There are two control loops in the EVM. Voltage Loop for Vout regulation; and Current Loop for constant current protection. Front End 0 and Filter 0 are for the voltage loop, Front End 1 and Filter 1 are for the current loop. In FIQ, the filter output of the two loops is compared. The loop takes control of the power stage is decided base on the larger output of the two filter-outputs.

The FIQ gets called to response every 4 switching cycles.

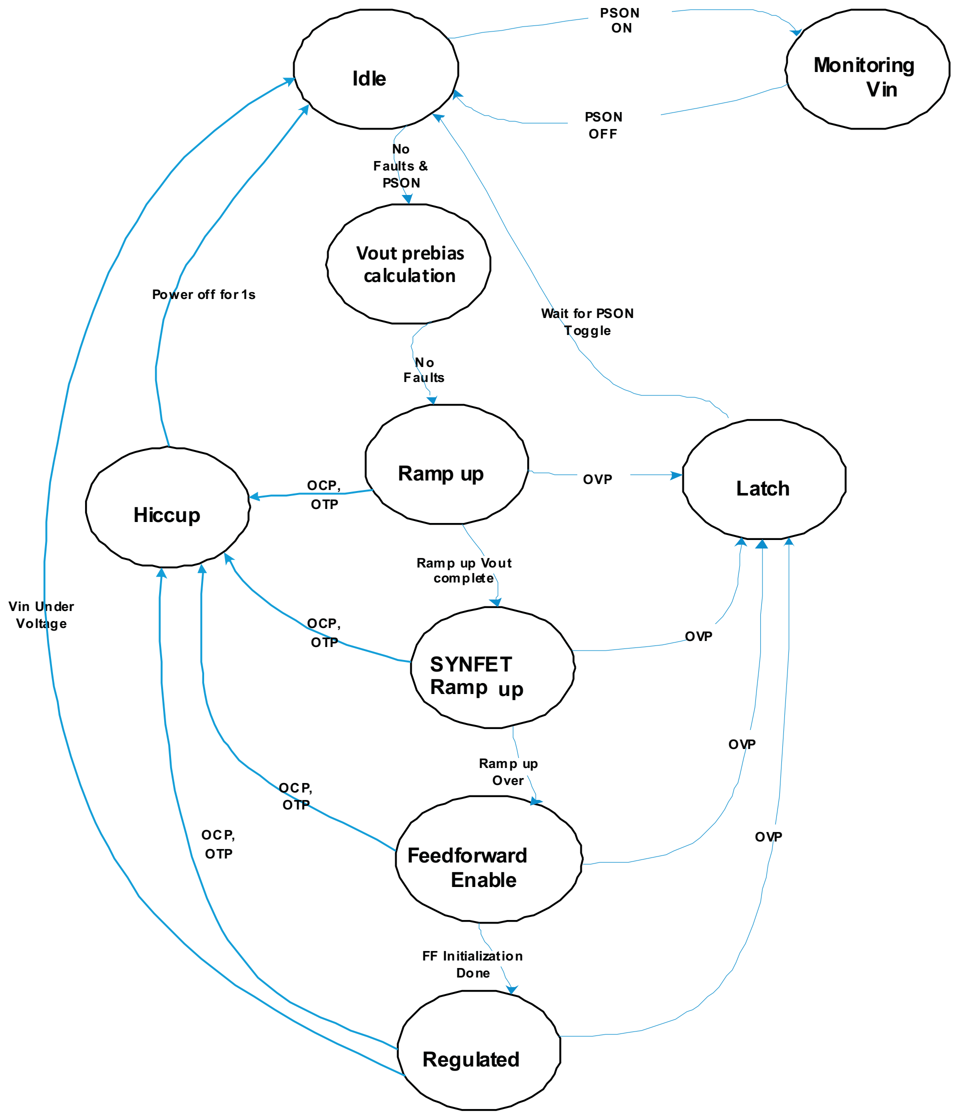


Figure 31. State Machine

A.4.3 Tasks within IRQ State Machine

Almost all firmware tasks occur during the IRQ. The only exceptions are the serial interface and PMBus tasks, which occur in the Background Loop; and the over current protection (OCP), which is handled by the FIQ. The IRQ is called to response every 100 µs.

At the heart of the IRQ function is the power supply State Machine implemented with “switch” command. The State Machine has its structure as shown in Figure 31. At a higher level, this State Machine allows the digital controller to optimize the performance of the power supply, based on exactly what it is doing.

A.4.4 Tasks within Background Loop

The background loop handles all PMBus communication as well as process and transmit data through the UART. The data flash is managed with a dual-bank approach. This provides redundancy in the event of a power interruption during the programming of data flash. Once new data flash values have been written, a function called erase_task() is initiated in the background loop to erase the old values. The erase_task() continues to get called until all of the old DFLASH segments are erased. Erasing the data flash in segments allows the processor in the controller to handle other tasks instead of waiting for the entire data flash to be erased before doing anything else.

A.5 System Normal Operation

The EVM is designed to operate in PWM hard switching mode in normal operation conditions. At very light load condition, if needed, the burst operation can be enabled for EVM operation. Please contact TI to find how to enable this function.

On the other end of the operation, if the load power keeps increasing beyond the rated value, then an over load condition will occur. In such a case, the system will enter protection operation, first entering constant power constant current mode, then if load power still keeps increasing, this will trigger cycle-by-cycle current limit. Please refer to Section 12.6 to learn more about these protection functions.

The converter of this EVM is designed to work in the following manner.

- When Vin reaches above 22V, the auxiliary power supply turns on. The UCD3138 starts and uses the single-frame approach to check if Vin reaches 36V if S1 is on. If Vin reaches 36V or above, operation starts.
- The converter is in normal operation to regulate the output voltage at 12V nominally. As shown in Figure 32, Ch1 = TP13, Ch2 = TP25, Ch3 = TP23, and Ch4 = TP12, all referenced to the primary-side ground.
- When the load current reaches such a level to have full power as specified in a pre-determined constant power setting, say 360W, the output voltage to be regulated reduced, the higher the load current, the lower the output voltage regulation point, in this way, the constant power operation is achieved.
- The converter is controlled to keep operating in constant power mode until the load current reaches a pre-determined level, say 36A, then the operation enters the constant current mode. In this mode, Frond End 1 and Filter 1 takes control of the power stage and maintains the output current at the setting point 36A. If the controller sees a large current on the primary side, say over 14A, hardware cycle-by-cycle current limit function becomes active.
- Further increase load current will shift the primary side current peak value higher. When the peak values reaches a pre-determined level, the operation is in short circuit protection mode.

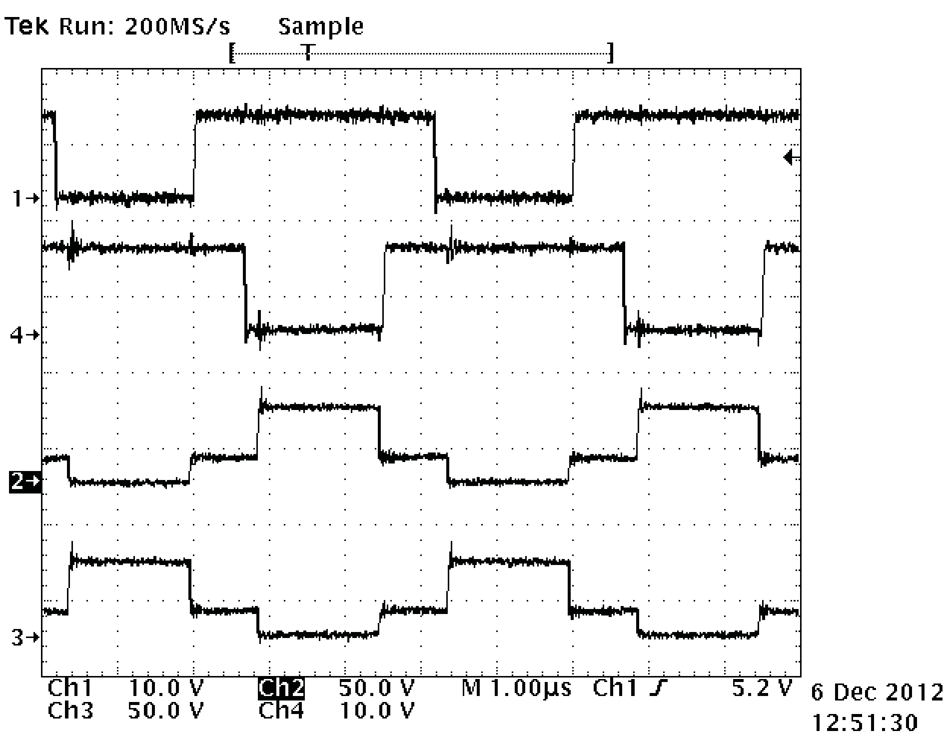


Figure 32. Normal Operation Switching Waveforms

A.5.1 Start-Up with Single-Frame Input Voltage Sensing

Before start up, the EVM uses a different way to sense the primary side voltage. It is called single-frame Vin sensing. In idle mode, two sets of single DPWM frames with 800ns width are sent, EADC2 are used to catch the second pulse from secondary and input voltage is determined. The sensing point can be programmed to get the best noise performance. The single-frame Vin sensing scheme is illustrated in Figure 33. Figure 34 shows test waveforms, where the green and the blue are two primary DPWM; the orange is VIN_SNS feed to EADC2. The purple is the transformer CT.

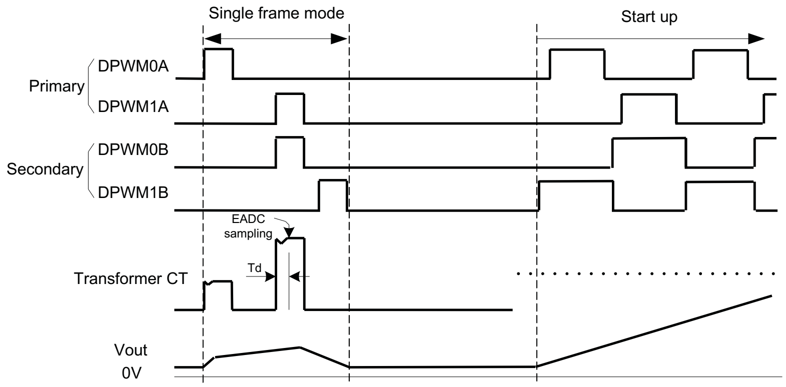


Figure 33. Input Voltage Sensing Using EADC2

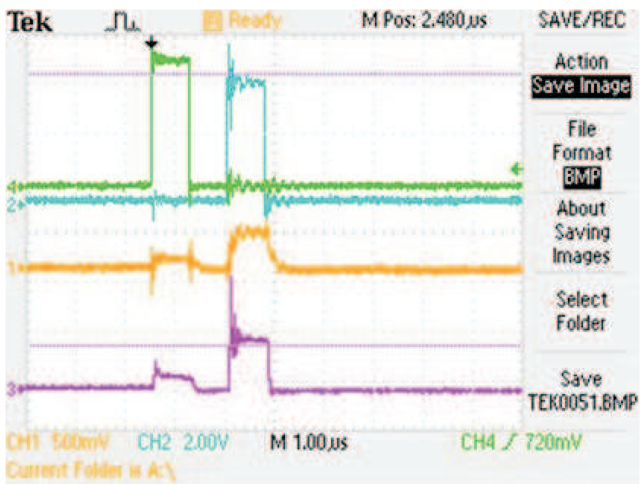


Figure 34. Single-Frame Approach Test

In normal operation control, the sensing hardware connection also serves the input voltage feed forward control, refer to Section 12.5.4.

A.5.2 Prebias Load and Load Synchronous Startup

When start a converter into pre-biased load condition, or start with two or more converters in parallel, special techniques are required since even a small difference from each output voltage may cause reverse current flow. The special technique, called Synchronous Startup, is used to enhance the parallel startup performance of UCD3138 controlled converters. This technique uses a GPIO pin as sync-pin which connects each board together to start at the same time then the output voltage difference from different converter is minimized.

A.5.3 Current Sharing Operation

To make two boards in current sharing operation, P2 pin 3 of each board is required to connect together as shown in Figure 35. P2 pin 3 serves as an “ISAHRE” connection, refer to Section 12.3.6. Figure 36 provides a test result, the yellow is output voltage, the other two channels are output currents from two paralleled EVM boards. The test was made with total load current change from 3A to 60A. The current sharing ratio in steady state at 60A-load is nearly perfect, i.e., close to 50%-50%. In the transient, the sharing difference is about 9.8A with settle down time about 560us. With the 95% load step change, the Vo overshoot and undershoot is about 0.4V on 12V, or about 3.5%

The current sharing operation is made possible in the steady-state. To share the load current in soft start time, it is recommended to use Synchronous Startup technique as described in Section 12.5.2. With this technique, the load current can still be shared to some degree since CPCC allows completing the soft start without shut down even if one converter in slight over load condition. Please contact TI to find how to set up Synchronous Startup.

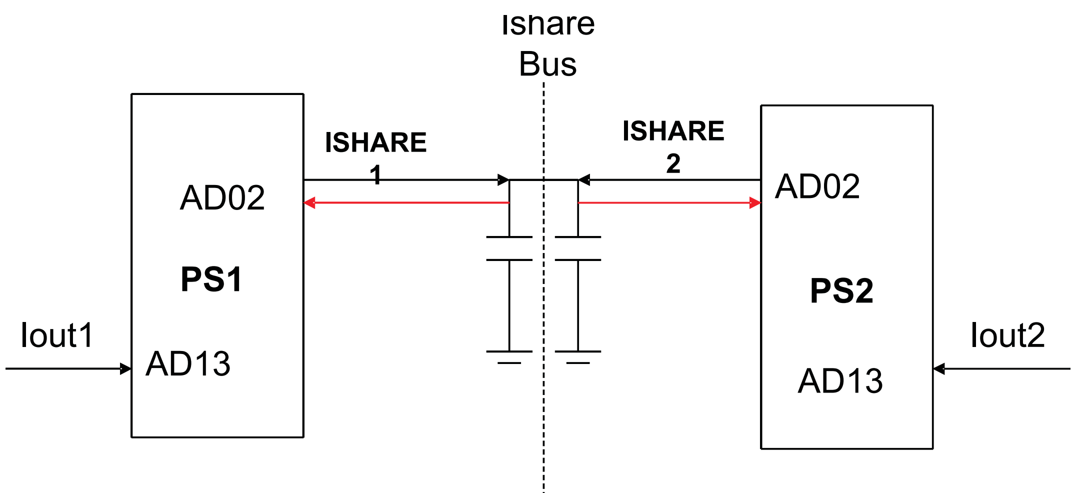


Figure 35. Current Sharing Operation

Figure 36. Current Sharing Test

A.5.4 Input Voltage Feed Forward Control

The input voltage feed forward control employed in the power converter control is to help to maintain output voltage regulation during input voltage high transient time. This technique can adjust the needed final duty cycle right with the input voltage change without go through normal feedback loop which usually has much longer timer delay in order to correct the output voltage error from input voltage transient. By ignoring the various losses, assuming output voltage 12V and unity transformer turns ratio, and assuming the converter secondary-side in CCM (as SR is in place), the relationship between input and output in a dc-dc forward type of converter, can be described by the duty cycle,

$$d = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

Plot this equation, the relationship between input and output can be shown with the red curve in Figure 37.

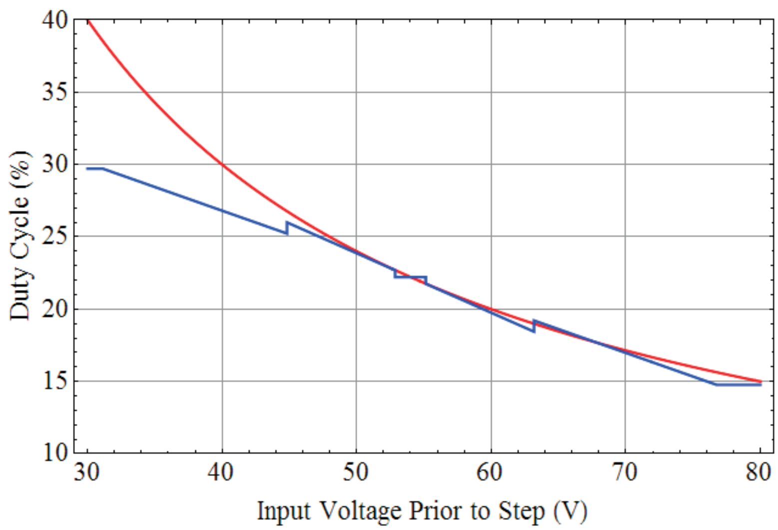


Figure 37. Duty Cycle Change in Feed Forward Control

In digital control, the duty cycle shown in the red-curve can be represented by a piecewise-linear approximation overlaid in the blue-curve. UCD3138 implements the blue-curve approximation with a non-liner multiplier as shown Figure 38 which shows the control functions implemented in UCD3138. In normal operation without input voltage transient, CLA2 output is unity. The DPWM is solely controlled by CLA1. When input voltage is in transient, CLA2 generates a multiplier based on input voltage change level which can be pre-programmed.

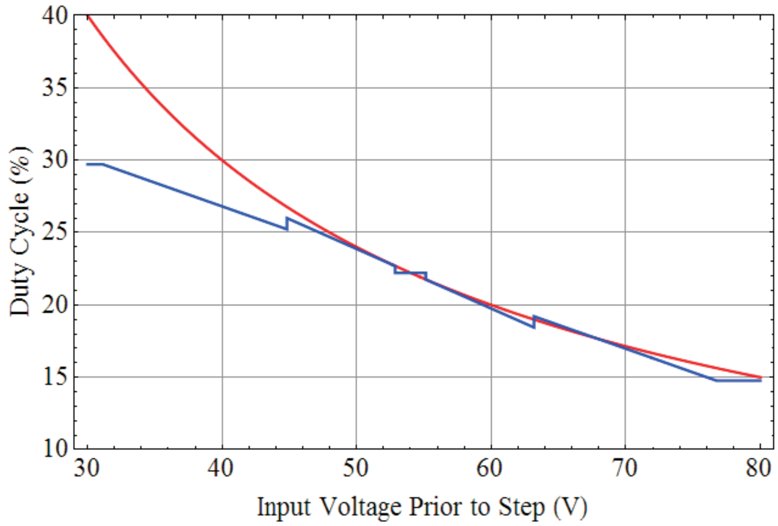


Figure 38. UCD3138 Digital Feed-Forward Control

On the control used in this EVM, the input voltage sense value is compared with Vref2, their difference, Vth, will set up the multiplier from CLA2 to CLA1 as below.

- If -Vth1 < Vth < Vth1, CLA2 = Gain0, or Kp0
- If -Vth2 < Vth < –Vth1, or, Vth1 < Vth < Vth2, CLA2 = Gain1, or Kp1
- If -Vth2 > Vth or Vth2 < Vth, CLA2 = Gain2, or Kp2

The above can be expressed as,

$$\text{Gain} = K_C + K_P \times \left(\text{VDAC} - V_{in\_sense}\right) \quad (2)$$

In steady-state, Gain0 = Kc, where Kc can be described as a unity number although in practice it may be designed differently to match other scaled values.

During the input voltage transient, nonlinear gain is generated to achieve desired duty cycle by feed forward control approximation.

As the control algorithm is of symmetrical characteristics from ±Vth1 and ±Vth2, an equilibrium point is required to be established. From practice such as in 48V-telecom application, this point may be initially selected at VIN0 = 48V. During the operation with different input voltage, a new equilibrium point will be re-established corresponding to that input voltage.

In this EVM design, Vin_sense signal is from VIN_CT as shown in Figure 26 and its relationship to VIN is expressed as,

Vin_sense = (Vin/N) x R29 / (R25+R29) = k x Vin, where k = 0.0154, and N is the turns ratio of Transformer T3.

A.5.5 Feed Forward Function Test

Load = 1A, Vin from 40V to 58V, Vin slew rate 20V/us, Vo maximum shift 0.68V, recovery time 50us. In Figure 39, the purple is Vout and the yellow is Vin. In Figure 40, the green is primary side DPWM and the yellow is Vin.

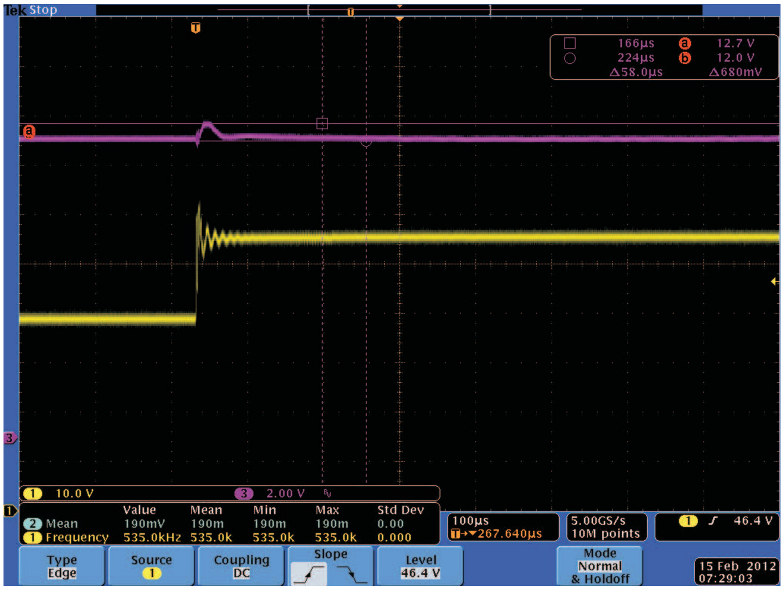


Figure 39. Vo Change from Digital Feed Forward Control

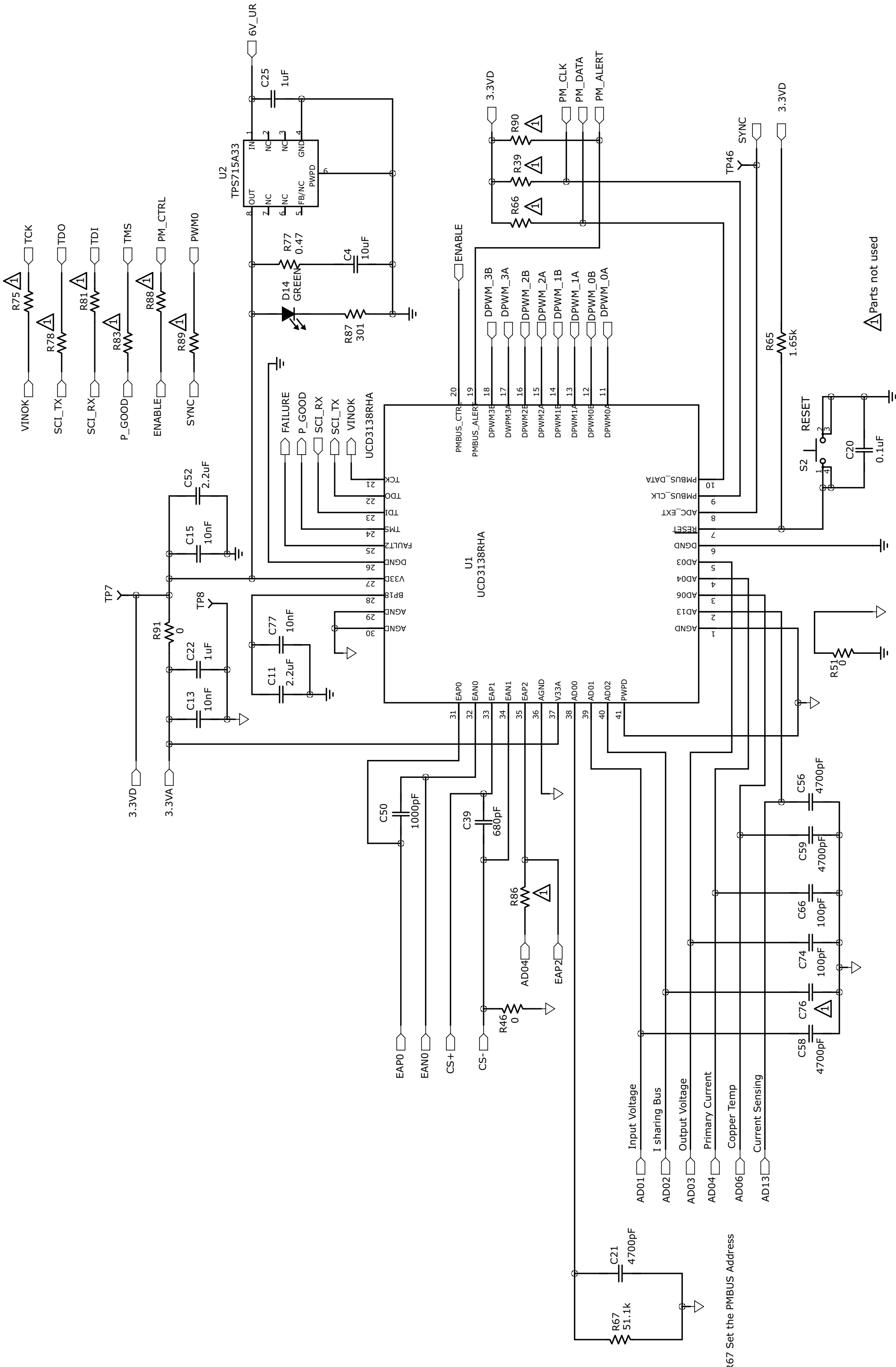


Figure 40. Duty Cycle Change from Digital Feed Forward Control

A.5.6 Light Load Operation

At light load, the burst operation can be enabled when the switching duty cycle is small. The significant benefit from this operation is the reduction of the power losses. The associated disadvantage is of higher output voltage ripple in steady-state and of larger output voltage dip in load demanding transient. But the higher ripple and the larger dip can be solved especially with digital control of its convenience and flexibility. For example, non-linear control from digital control can solve the large dip during load transient. The higher ripple can also be reduced by narrowed duty cycle on/off limit for burst operation control.

Figure 41 shows the burst operation timing diagram with UCD3138. When the controller detected light load condition, the operation is enabled into Light-Load-Enable (LLE) by firmware. When load condition is changed to heavy, CLA can generate a large gain to adapt the load change and minimize the output voltage drop although the operation is still in LLE mode. If the load keeps heavy for certain time, light load will be terminated by the firmware.

The burst operation mode is disabled in the EVM. Please contact TI to know how to enable this feature.

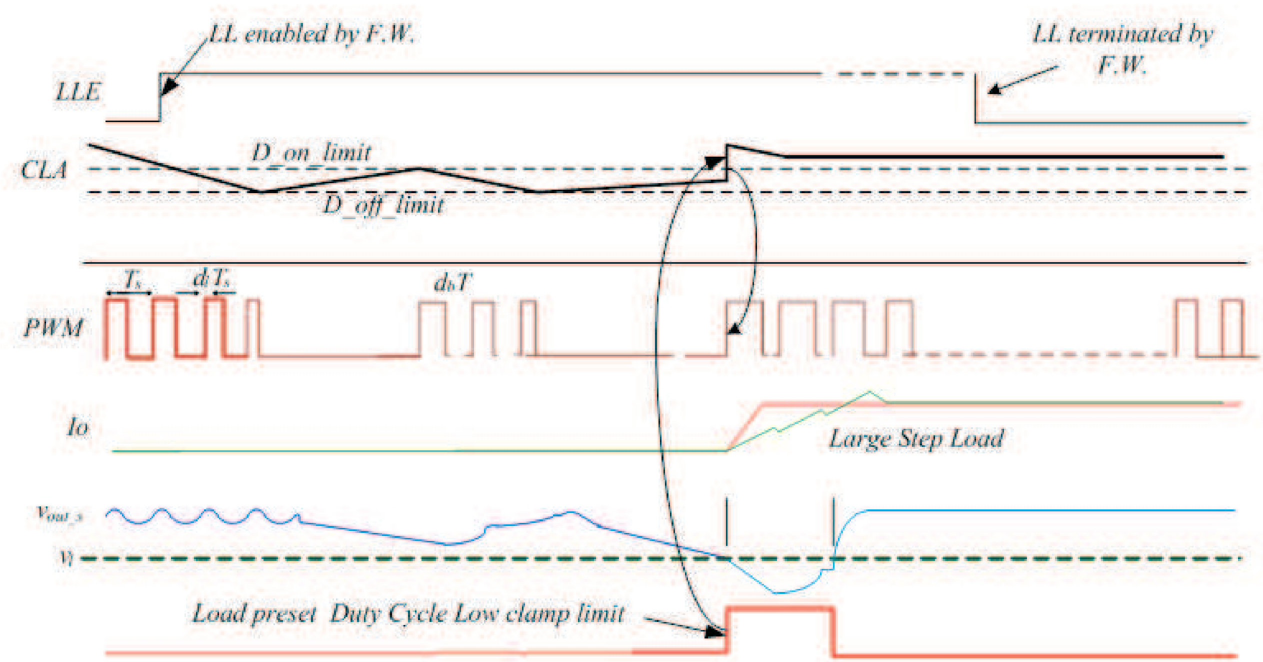


Figure 41. Burst Operation Timing Diagram

A.6 System Operation in Protection

A.6.1 Faults and Warnings

The system comes equipped with a variety of programmable fault and warning options. In section 12.3.8, Table 5 lists the LEDs used to indicate a fault. Table 6 below shows the basic faults and warnings available in the EVM along with the corresponding action taken by these events. Each of these parameters can be modified through the GUI.

Table 6. Faults and Warnings

SIGNAL	TYPE	WARNING	FAULT RESPONSE
VOUT	Over	Report	Report & Latch off
	Under	Report	Report
VIN	Over	Report	Report & Latch off
	Under	Report	Report & Latch off
IOUT	Over	Report	Report & Latch off
IIN	Over	Report	Cycle by cycle limiting
Temperature	Over	Report	Report & Latch off

The GUI reporting includes appropriate setting of the PMBus alert line, status byte and status word. Faults and warnings can be reset by toggling the unit off and then on. Alternatively, as long as the system does not latch off, the “Clear Faults” button can also be used to clear any faults or warnings. Refer to Figure 42 which is from the Designer GUI Monitor tab. More details can be found in Section 13.

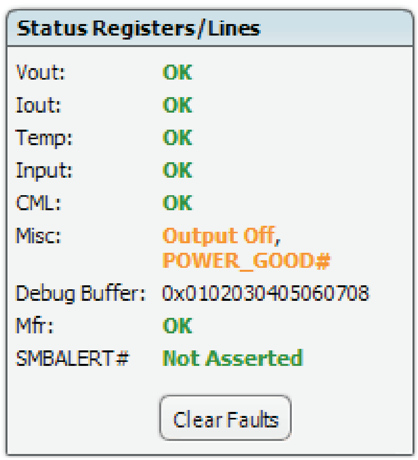


Figure 42. Faults and Warnings

A.6.2 Constant Power Constant Current Operation

Both hardware and firmware in this EVM supports Constant Power Constant Current, or CPCC operation. Figure 43 illustrates the behavior of the output voltage and output current (V¬OUT vs. IOUT). However, the EVM comes pre-programmed with a constant power threshold of 360 W and a constant current threshold of 36 A. Some of the limits are adjustable through the GUI and new setting can be saved to data flash. The maximum hardware capability is to limit the current within 36A. Figure 44 shows the GUI interface to these controls with the default values. The CPCC can be enabled or disabled through GUI. Details can be found in Section 13.4.2.

After the output power reaches the set point, Vout starts to drop while the power keeps the same which means the current may increase. The power stage stays on and it won't enter latch mode. When the current loop filter output (Front End 1 and Filter 1) is larger than the voltage loop filter output (Front End 0 and Filter 0), the current loop takes control of the power stage and output voltage starts in hiccup operation state. In hiccup state, the power stage stays on for 1s, and then goes to idle state and try to turn on again. If the load is reduced, the power stage will go to regulated state. If the load current is still high, the output voltage goes to hiccup state again. Only OVP will take the power stage to latch-off state. OTP, OCP, and constant current will take the power state to hiccup state. In hiccup state, the power state turns on automatically. In latch state, toggle off the PSON switch is needed or recycle the input power.

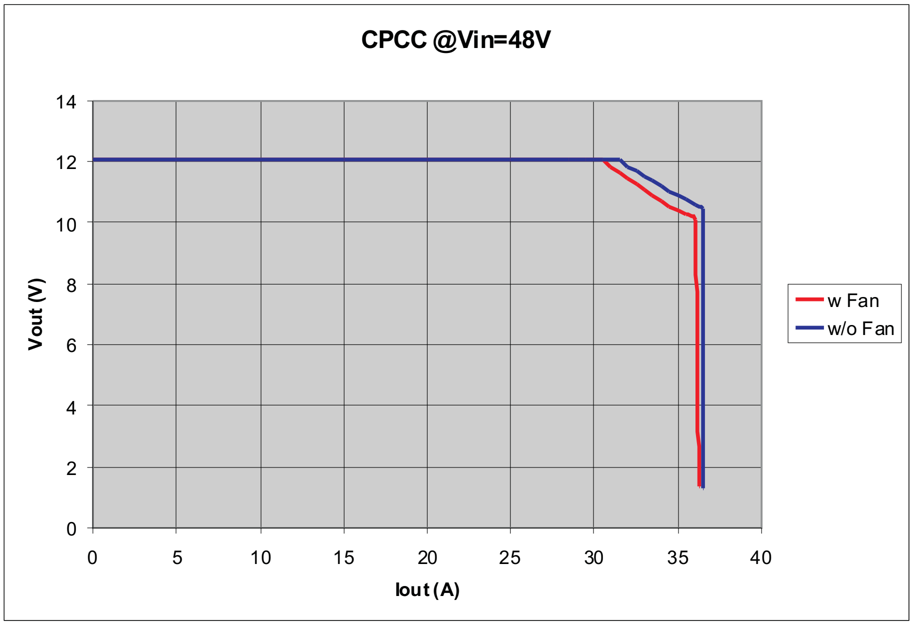


Figure 43. Constant Power Constatnt Current Operation

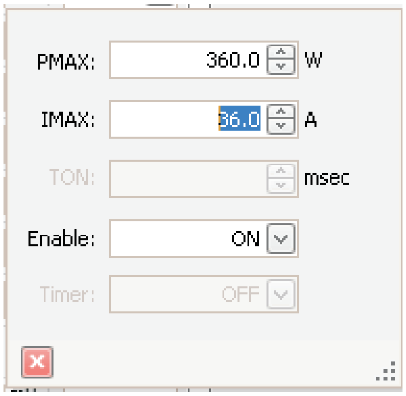


Figure 44. CPCC Default Values and Adjustable through GUI

A.6.3 Cycle-By-Cycle Current Limit

Cycle by cycle current limit is made to the primary side input current. The current is sensed by current transformer T1. The sensing circuit is shown in Figure 45; also refer to full schematics of Figure 1 and power stage Figure 23. The current signal is fed into AD04 and compared to a programmable threshold on a cycle-by-cycle basis. Whenever this current exceeds the threshold the active DPWM waveforms are truncated. The cycle-by-cycle current limit is mainly used to the primary current to limit its peak within pre-determined value, default as 16A.

As AD04 is a simple voltage comparator, external current slope compensation circuit may be needed in order to minimize the sub-harmonics normally existing in peak current mode control including cycle-by-cycle current limit. An example circuit is shown in Figure 46. More detail on this circuit can be found in “Modeling, Analysis and Compensation of the Current-Mode Converter”, (TI Literature Number SLUA101).

In case the peak current mode control is employed in an application, the peak current mode control should be made through Front End 2 (EADC2) instead of using AD04. Frond End 2 has build-in current slope compensation (RAMP) as shown in Figure 47 which does not require external slope compensation.

UCD3138 can balance two pulses in a switching cycle with the same width. In UCD3138RHA, this feature exists in the DPWM module on its two outputs, for example between DPWM0A and 0B, but not available on the interconnection matrix. Then this EVM is not able to balance the pulse width in a switching cycle. If this feature is preferred, please contact TI for technical assistance.

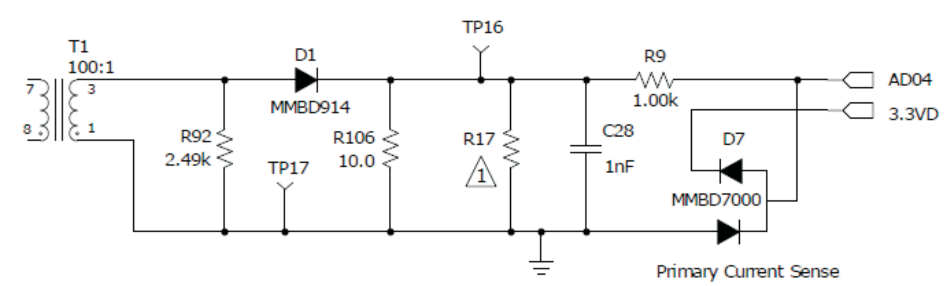


Figure 45. Cycle-by-cycle Current Limit Sensing Circuit

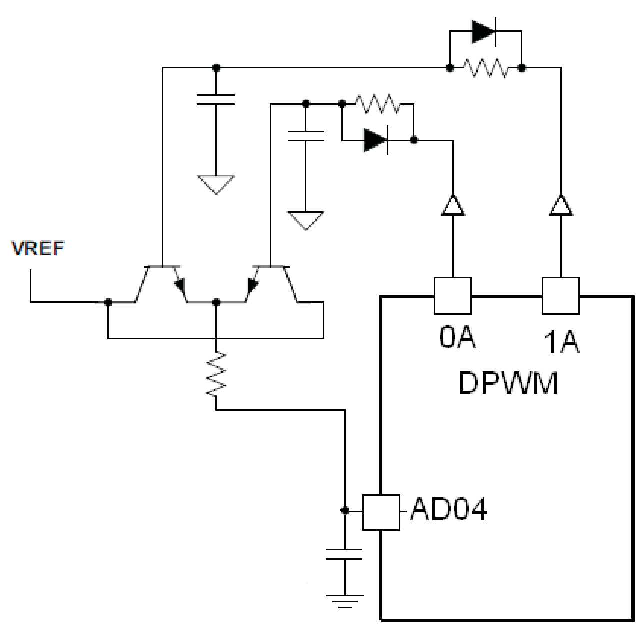


Figure 46. An Example of External Slope Compensation

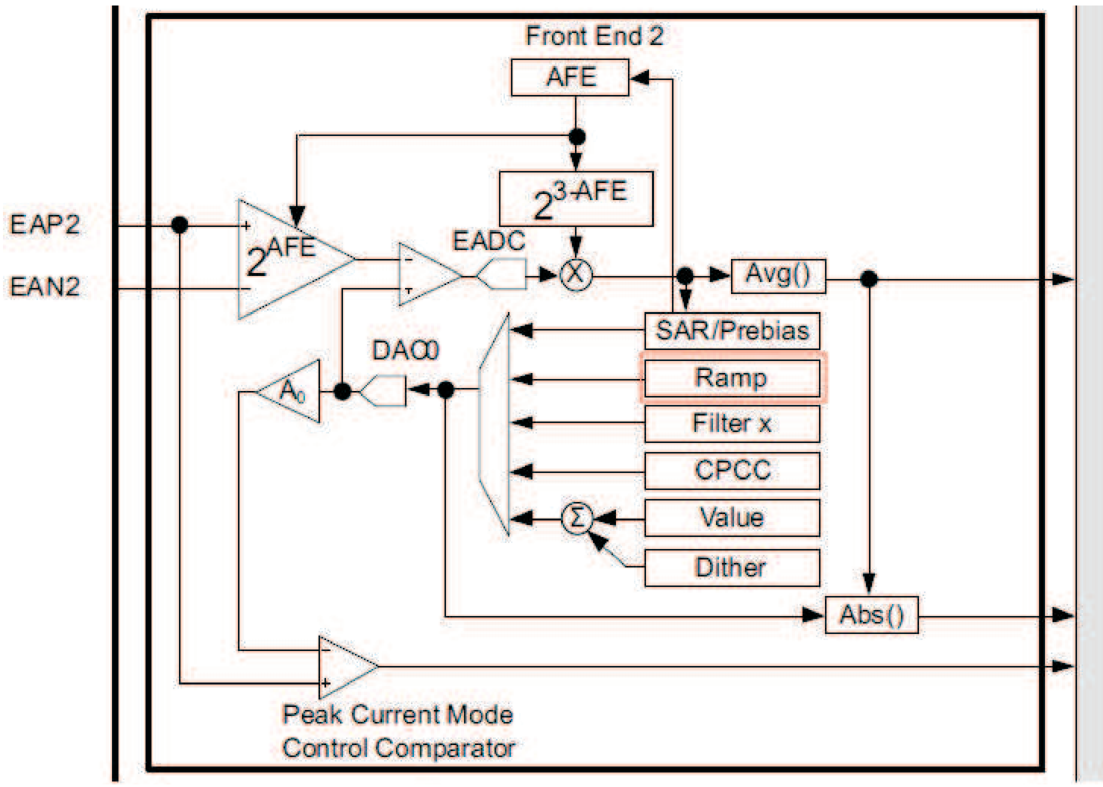


Figure 47. Peak Current Mode Control with Front End 2

A.6.4 Short Circuit Protection

Load short circuit protection is mainly based on the secondary side current sensing when the load current is beyond a 36A by default. In short circuit protection the output voltage is in hiccup state.

Figure 48 shows a test results with the conditions: short circuit test at 30A load, Vout (Ch1), Ipri (Ch 2), and Vin (Ch 3)

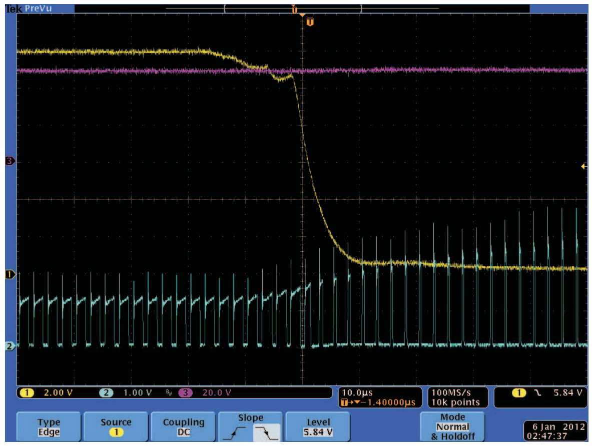


Figure 48. Short Circuit Protection Test

A.6.5 Output Over Voltage

Output over voltage detection and protection is through AD03, refer to Figure 1 and Figure 23. When output over voltage is detected, the switching pulses will be disabled and the board will be in latch-off until recycle the input power or toggle the switch S1.

A.6.6 Input Over Voltage

The input over voltage is detected based on the main power transformer winding as described in Section 12.3.4. Currently in the EVM delivered, input voltage is detected and the firmware provides warning to the Designer GUI. Please contact TI if need OVP protection.

A.6.7 Over Temperature

Over temperature includes UCD3138 internal temperature sensing and external added temperature sensing. The external over temperature condition is determined by a temperature sensing element on U13, LM60C. The temperature signal is fed into the controller through AD06. U13 is located on board top side next to the current sensing copper. Then it is sensing the temperature of secondary-side board temperature. In addition to the over temperature protection, this temperature information is used to compensate the copper current sensing.

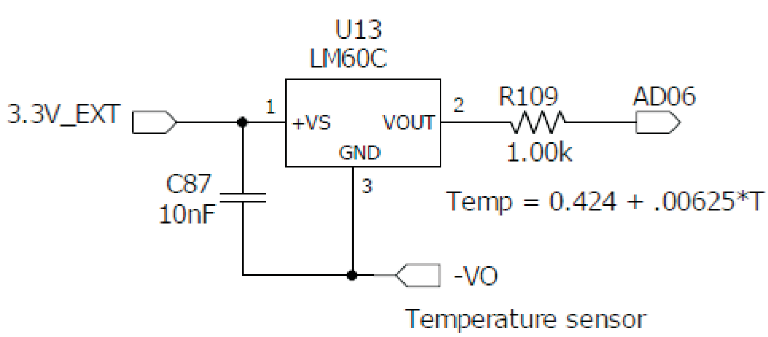


Figure 49. Temperature Detection Circuit

A.7 Loop Compensation Using PID Control

PID control is usually used in the feedback loop compensation in digitally controlled power converters. We will describe several aspects how to use PID control.

A.7.1 Digital PID Coefficients Transfermation to Poles and Zeros in s-Domain

PID control in UCD3138 CLA for control loop is formed in the following equation in z-domain:

$$G_c(z) = K_P + K_I \frac{1+z^{-1}}{1-z^{-1}} + K_D \frac{1-z^{-1}}{1-\alpha \times z^{-1}} \tag{3}$$

If Equation (3) is converted to the s-domain equivalent using the bilinear transform, the result has two forms. One is with two real zeros and one real pole:

$$G_{cz}(s) = K_0 \frac{\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}{s\left(\frac{s}{\omega_{p1}}+1\right)} \tag{4}$$

K0 is the gain of the frequency domain pole at origin, and K0 is also represented as the angular frequency when the integrator Bode plot gain crosses over with 0-dB. By the way, K0 can be used as a method for initially designing the feedback loop compensation, refer to [5] for more details.

The second way is when the two zeros are possibly presented with complex conjugates and in such a case,

$$G_{cz}(s) = K_0 \frac{\left(\frac{s^2}{\omega_r^2}+\frac{s}{Q \times \omega_r}+1\right)}{s\left(\frac{s}{\omega_{p1}}+1\right)} \tag{5}$$

Two complex conjugate zeros are expressed as,

$$\omega_{z1,\,z2} = \frac{\omega_r}{2 \times Q}\left(1 \pm j\sqrt{4 \times Q^2 - 1}\right) \quad \text{and} \quad j = \sqrt{-1} \tag{6}$$

$$\omega_r = \sqrt{\omega_{z1} \times \omega_{z2}} \tag{7}$$

$$Q = \frac{\sqrt{\omega_{z1} \times \omega_{z2}}}{\omega_{z1} + \omega_{z2}} \tag{8}$$

The factor of Q is in the range of 0 to infinite. The two complex conjugate zeros become the two real zeros when Q is not greater than 0.5.

$$Q \le 0.5 \tag{9}$$

Hence, Equation (4) is actually a special form of Equation (5). In this sense, Equation (5) can be used in either case across the range of Q.

A low pass filter usually exists in a control loop of its feedback path. The low pass filter adds a pole to the loop,

$$H_{cs}(s) = K_{cs} \frac{1}{\frac{s}{\omega_{pcs}} + 1} \tag{10}$$

The close loop transfer function is then shown as below:

$$G_{cs}(s) = \frac{G_M(s) \times G_{PID}(s)}{1 + G_M(s) \times G_{PID}(s) \times H_{cs}(s)} \tag{11}$$

where GM(s) is the control plant transfer function. For example, GM(s) can be the transfer function associated to the modulator in an HSFB converter.

The parameters can be calculated with the assumption of sensor sampling cycle Ts much smaller than the corresponding time constant of the voltage loop bandwidth, TC. A rule of thumb is to choose the sampling frequency to meet

$$T_s \le 0.05 \times T_C \tag{12}$$

When the above assumption is true, the delay effect from the sampling (usually with zero order hold or ZOH) can be ignored and the parameters can be determined after we know where the poles and zeros should be positioned. Table 7 summarizes the poles and zeros in a form to relate z-domain to s-domain.

$$K_P = \frac{K_0 \times \left(\omega_{p1} \times \omega_{z1} + \omega_{p1} \times \omega_{z2} - \omega_{z1} \times \omega_{z2}\right)}{\omega_{p1} \times \omega_{z1} \times \omega_{z2}} \tag{13}$$

$$K_I = \frac{K_0 \times T_s}{2} \tag{14}$$

$$K_D = \frac{2 \times K_0 \times \left(\omega_{p1} - \omega_{z1}\right) \times \left(\omega_{p1} - \omega_{z2}\right)}{\omega_{p1} \times \omega_{z1} \times \omega_{z2} \left(T_s \times \omega_{p1} + 2\right)} \tag{15}$$

$$\alpha = \frac{2 - T_s \times \omega_{p1}}{2 + T_s \times \omega_{p1}} \tag{16}$$

Table 7. Poles and Zeros from PID Coefficients

System Name	Transfer Functions
Complex Zeros (K0, fz, Qz, fp)	$\dfrac{\dfrac{s^2}{(2 \times \pi \times f_z)^2} + \dfrac{s}{2 \times \pi \times f_z \times Q_z} + 1}{\dfrac{s}{2 \times \pi \times K_0} \times \left(\dfrac{s}{2 \times \pi \times f_p} + 1\right)}$
Real Zeros (K0, fz1, fz2, fp)	$\dfrac{\left(\dfrac{s}{2 \times \pi \times f_{z1}} + 1\right) \times \left(\dfrac{s}{2 \times \pi \times f_{z2}} + 1\right)}{\dfrac{s}{2 \times \pi \times K_0} \times \left(\dfrac{s}{2 \times \pi \times f_p} + 1\right)}$
Device PID (Kp, Ki, Kd, α)	$1000 \times \left(K_p + K_i \times \dfrac{1+z^{-1}}{1-z^{-1}} + K_d \times \dfrac{1-z^{-1}}{1-\alpha \times 2^{-8} \times z^{-1}}\right) \times 2^{-SC} \times KCOMP \times 2^{-19} \times \dfrac{1}{2^4 \times (PRD+1)}$

A.7.2 Tuning PID Coefficients for Loop Compensation

When making fine-tune adjustments to the feedback control loop, one would like to know each parameter in PID how to affect the control loop characteristics without going through complicated description of the above equations. Table 8 below helps this and visually shown in Figure 50.

Table 8. Tuning PID Coefficients

CONTROL PARAMETERS	IMPACT ON BODE PLOT
K_P	Increasing KP
	Pushes up the minimum gain between the two zeros.
	Moves the two zeros apart.
K_I	Increasing KI
	Pushes up integration curve at low frequencies.
	Gives a higher low-frequency gain.
	Moves the first zero to the right.
K_D	Increasing KD
	Shifts the second zero left.
	Doesn't impact the second pole.
α	Increasing α
	Shifts the second pole to the right.
	Shifts the second zero to the right.
$T_s = 1 / f_s$	Increasing the sampling frequency fs :
	Causes the whole Bode plot to shift to right.

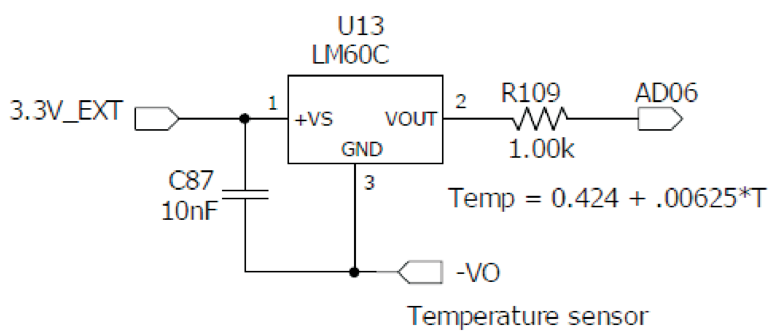


Figure 50. Tuning PID Parameters

A.7.3 Measuring the Control Loop

The control loop measurement can be made by injecting frequency sweep signal across R16. The connections can take advantage of P2 pin 1 and TP10.

A.8 Evaluating the EVM with GUI

Collectively, the GUI is called Texas Instruments Fusion Digital Power Designer. The GUI serves the interface for several families of TI digital control IC's including the family of UCD31xx, i.e., UCD3138 as its one member. The GUI can be divided into two main categories, Designer GUI and Device GUI. In the family of UCD31xx, each EVM is related to a particular Designer GUI to allow users to re-tune/re-configure a particular EVM in that regarding with existing hardware and firmware. Device GUI is related to a particular device to access its internal registers and memory cells.

UCD3138HSFBEVM-029 is a standalone board where UCD3138RGH 40-pin device is placed. The firmware to control this converter is downloaded into this board through Device GUI. How to install the GUI is described in the user's guide "Using the UCD3138CC64EVM-030 (TI Lit#, SLUU886)". The designer GUI is installed at the same time when installing the Device GUI.

A.8.1 Graphical User Interface (GUI)

As mentioned above, there are two types of graphical user interfaces (GUI), one is Device GUI, and the other is Designer GUI. The Device GUI is sometimes called low level GUI. From the Device GUI, device's registers are accessed if the device is in the ROM mode and the PMBus communication is established. This GUI should be used to download the code when the device is blank at the first programming. Also, at the flash mode, a customer can send PMBus commands to read or write the data. The Designer GUI is an interface between a host and a user's board. It supports some of PMBus commands for configuration, monitoring and design such as loop compensator built in the UCD3138 digital controller.

A.8.1.1 13.1.1 Hardware Setup

The board hardware connection is overall the same as shown in Section 5.2 and Figure 4 while shown in Figure 51 again. The addition to the setup is to connect USB-to-GPIO to the board. The ribbon cable connects to J6 and the USB cabled connects to a host PC computer. The remaining connections are described again in the below.

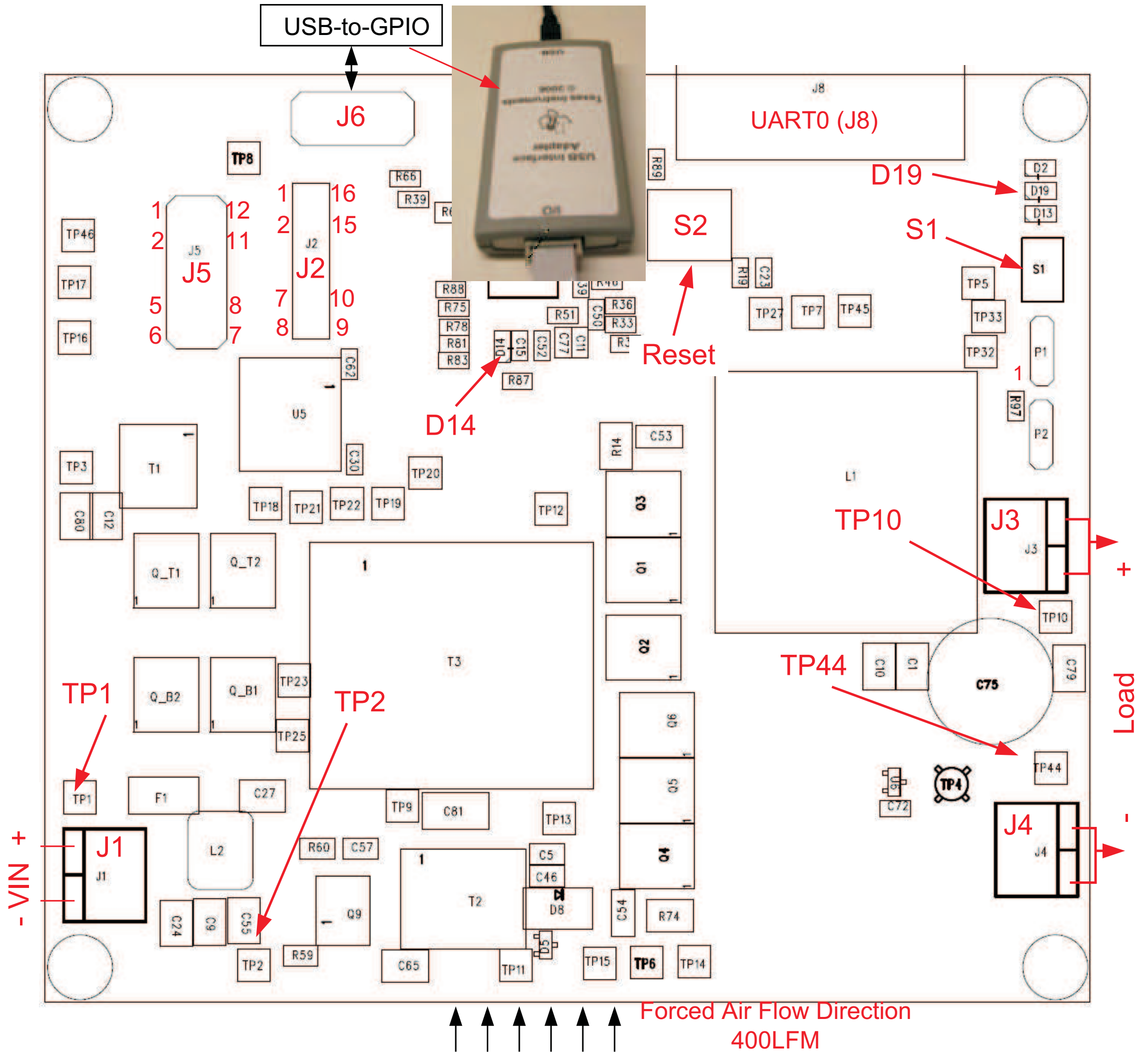


Figure 51. Test Setup

- Refer to Figure 51 for basic hardware connections. The required equipment is listed in Section 5.1.
- Before making electrical connections, visually check the boards to make sure no shipping damage occurred.
- Connect the DC voltage source to J1-1 (+) and J1-2 (-). Set up the DC output voltage in the range specified in Table 1, between 36 V_{DC} and 72 V_{DC}; set up the DC source current limit 12A.
- Connect an electronic load with either constant current mode or constant resistance mode. The load range is from zero to 30A.
- Connect USB-to-GPIO ribbon cable to J6 and connect USB-to-GPIO USB cable to a host PC computer.
- Check and make sure the jumpers are installed correctly on J2 and J5.
  - J2 should be jumped across to connect its 1-16, 2-15, 7-10, and 8-9.
  - J5 should be jumped across to connect its 1-12, 2-11, 5-8, and 6-7.

WARNING

Follow the connections correctly to avoid possible damages

- It is recommended to use the switch S1 to turn on the board output after the input voltage is applied to the board. Before applying input voltage, make sure the switch, S1, is in the “OFF” position.
- If the load does not have a current or a power display, a current meter or low ohmic shunt and DMM will be needed between the load and the board for current measurements.
- Connect a volt-meter across the output connector and set the volt-meter scale 0 to 15V on its voltage, DC.

A.8.1.2 GUI Installation

GUI software can be downloaded from the TI website, www.ti.com. The software should be installed in the host PC before it is executed. More details about the TI GUI, which is called TI Fusion Digital Power Designer (DFPD), can be found in its user's guide/manual. Please contact TI to get this user's guide/manual. After the GUI installation, the Guide can be found in the Designer GUI of its real time "Help".

"Help" > "Documentation & Help Center" > "UCD3138"

Copy the TI Fusion Digital Power Designer zip file and unzip the file TI-Fusion-Digital-Power-Designer-xx.zip to get installer TI-Fusion-Digital-Power-Designer-xxx.exe. The xxx in the file name refers to the GUI release version.

Double click the installer TI-Fusion-Digital-Power-Designer-xxx.exe and follow the straight forward instructions to finish the installation. Normally, you need accept all the installation defaults. In order to get all GUI functions, all boxes under Select Additional Tasks should be checked, shown in Figure 52.

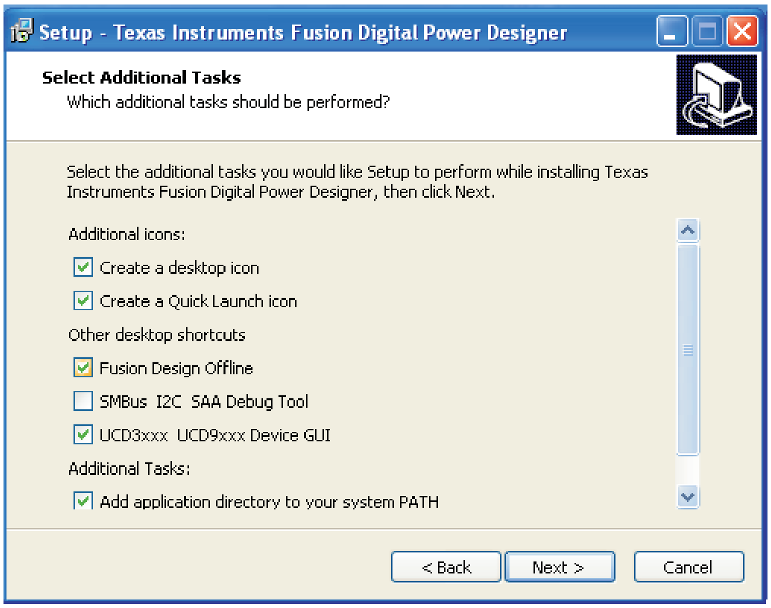


Figure 52. GUI Installation

After the installation, a quick launch button is created next to the start menu which contains shortcuts to commonly used applications. Figure 53 shows the icon of TI DFPD after the installation. Some other icons such as UCD3K Device GUI are also displayed on the desktop. For more information on the GUI installation, one can refer to UCD3138CC64EVM-030 user's guide.

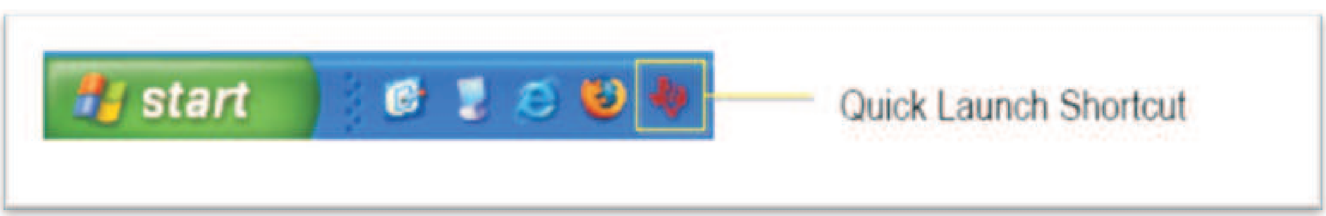


Figure 53. GUI Shortcut Location

A.8.1.3 USB-to-GPIO Adaptor Connection

CAUTION

Shut off DC power source before connection to avoid electrical shock!

Connect one end of the ribbon cable to the module, and connect the other end to the USB-to-GPIO (HPA172) interface adapter. Connect the Mini connector of the USB cable to the USB interface adapter, and connect the other end to the USB port of the host computer.

A.8.1.4 Launch the Designer GUI

Click the Quick Launch Shortcut icon located next to the start menu. The GUI starts to look for the attached device attached to the PMBus. If the device is found and the communication is established successfully, one should see a screen that looks similar to Figure 54. In the following we will describe how to use the GUI to evaluate the module.

Figure 54. Designer GUI Overview

A.8.1.5 Designer GUI Overview

The Designer GUI has four tabs, as shown in Figure 54, namely, Configure, Design, Monitor, and Status. After launch the GUI, its default tab is Monitor. To go to the other three tabs, simply click the tab you would like to go.

In the GUI used with this EVM, Configure is used to configure the EVM settings through PMBus commands. Design is mainly used to make tuning control loop parameters and to set up the Feed-Forward control non-linear gains. Monitor is used to monitor the board operation. Status is mainly used to show fault and/or warnings.

A.8.2 Operation Monitoring

After the designer GUI launched, the Monitor tab is presented by default as shown in Figure 54. This tab provides a quick overview of operation status with some settings changeable as well. This tab also provides oscilloscope type of plot view in real time operation. The number of scope windows can be adjusted by check or un-check upper left square boxes to show or to hide these scope plot windows.

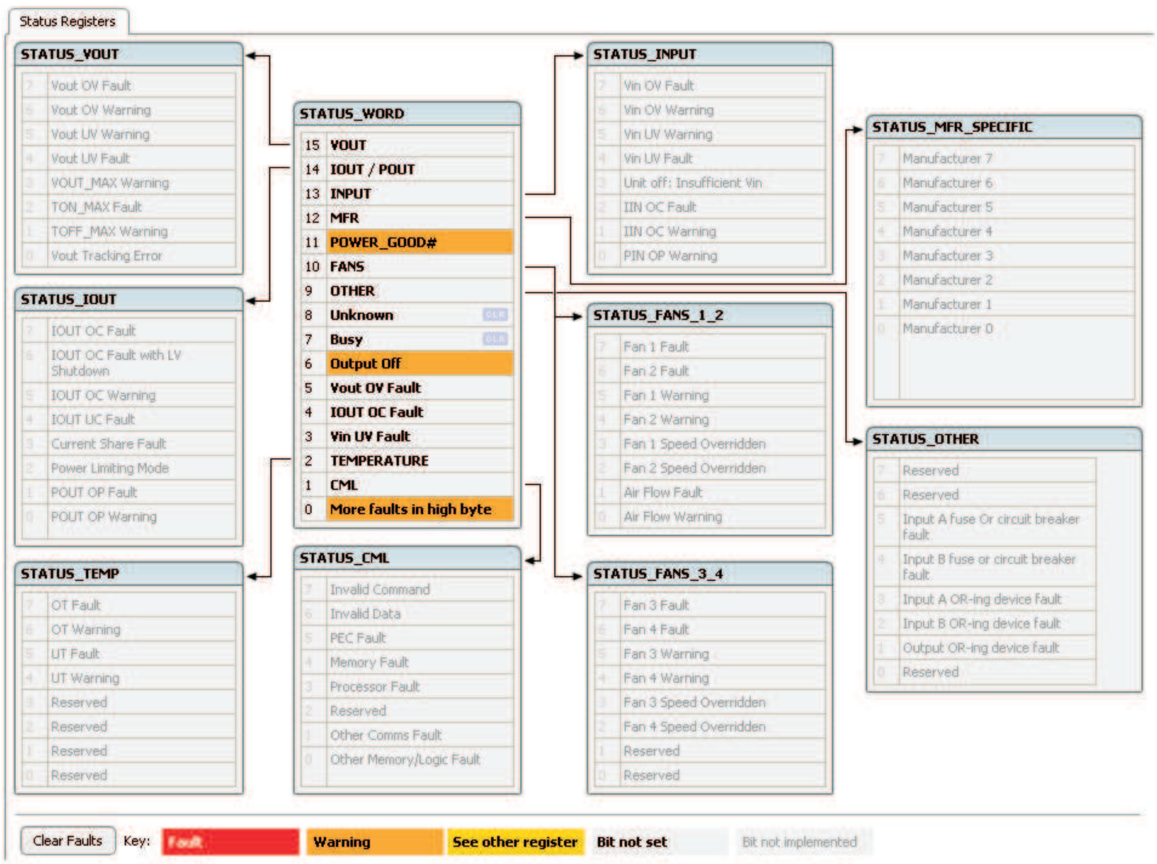


Figure 55. Designer GUI Status

A.8.3 Operation Status

After click the Status tab as shown in Figure 54, the EVM operation status is shown as in Figure 55. All grayed entries are candidates that can be implemented. Those in black are showing current operation status which helps to indicate potential operation issues with warning or fault indications. If a fault occurred, the corresponding entry is highlighted in red. Warnings are not a fault while may remind the user that those might need attention.

A.8.4 Configuring EVM

Configure tab can help to adjust the EVM feature setup conveniently without directly accessing the firmware code. Also, it helps to navigate through the various features of the converter through the GUI.

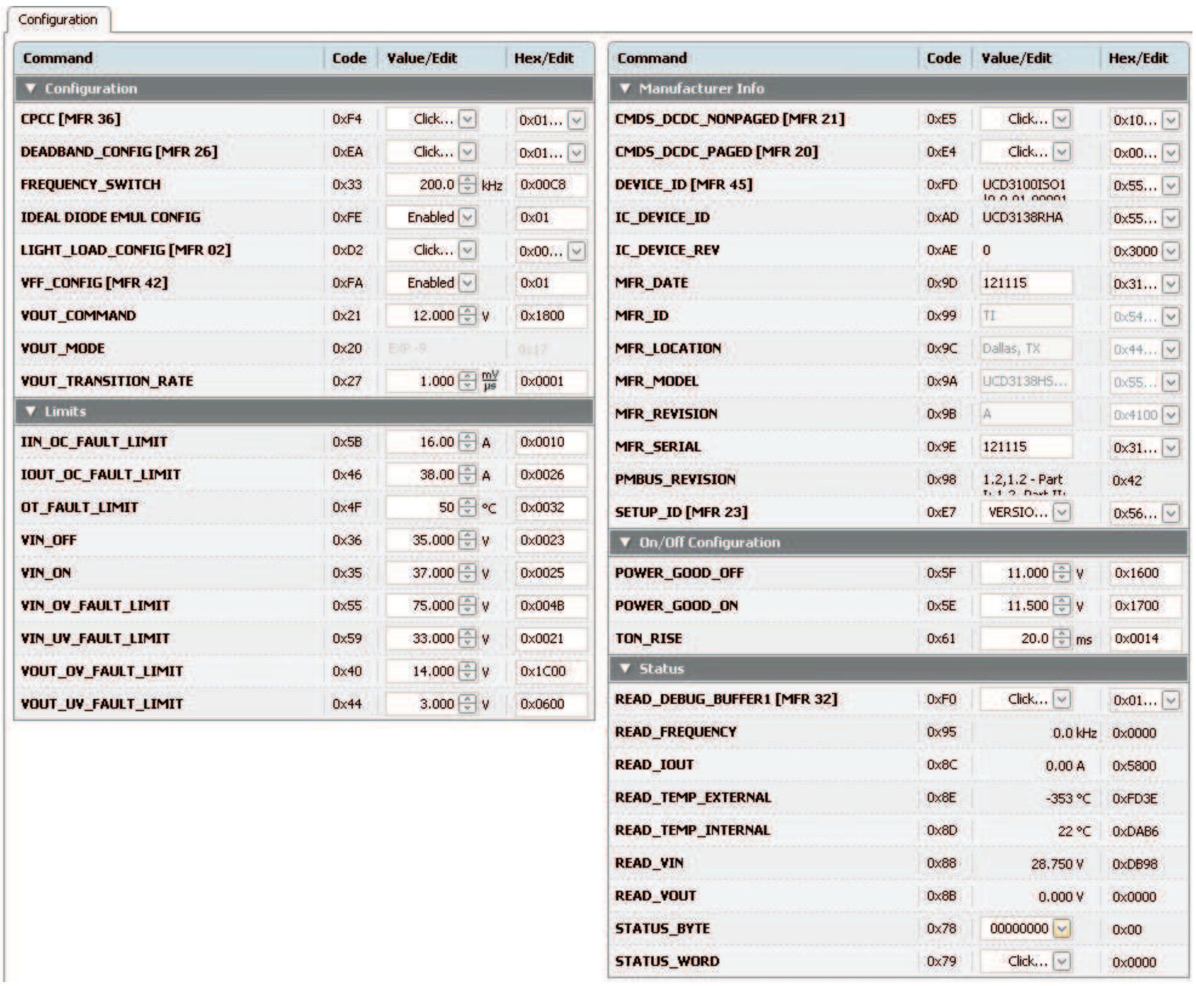


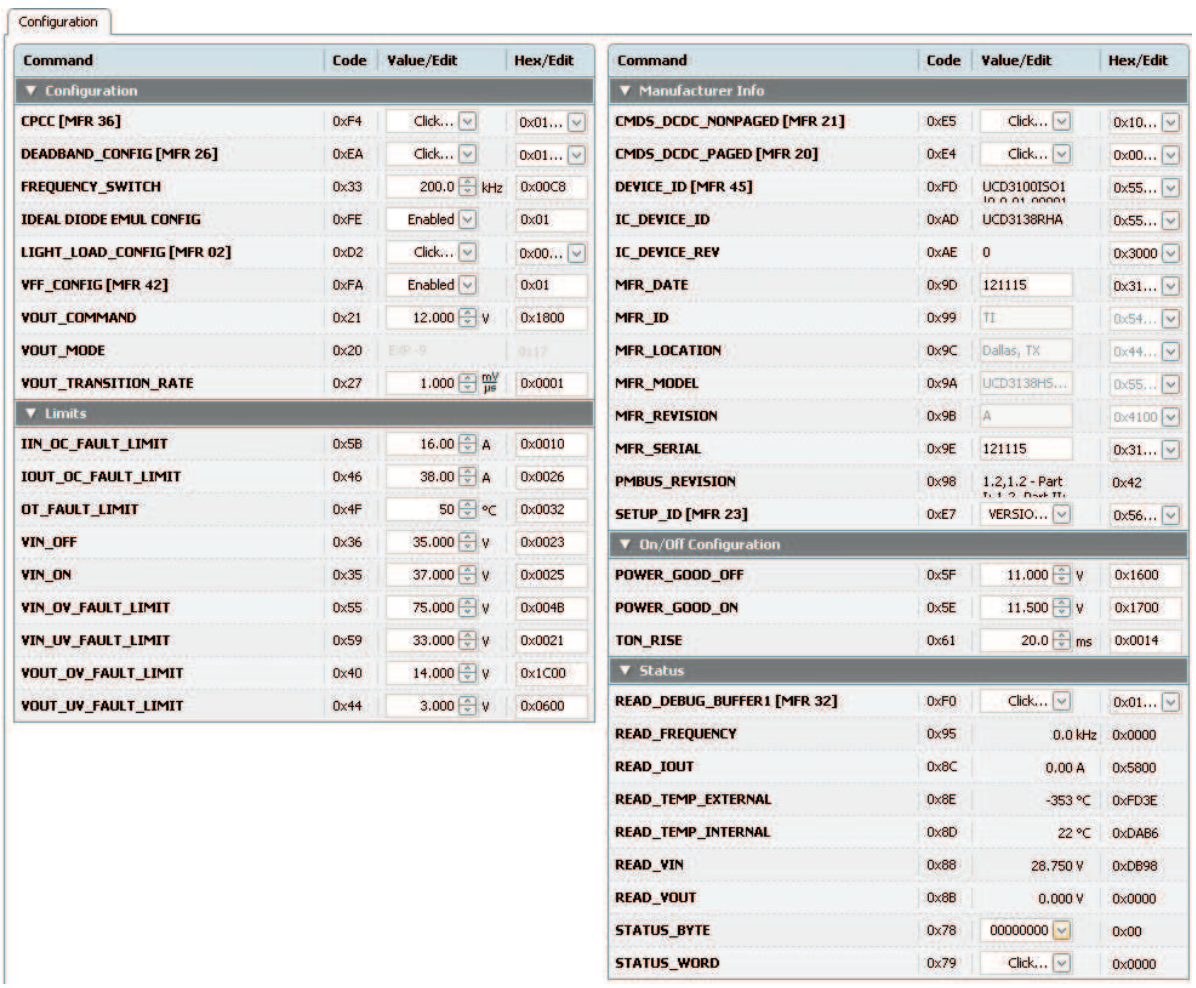
Figure 56. GUI Supported PMBus Commands

A.8.4.1 GUI Supported PMBus Commands

Figure 56 displays the various GUI based PMBus commands supported by the current version of the firmware. Adding additional standard commands is easy to do with the built in “Isolated Bit Mask” generator. This tool creates a coded index that the GUI reads from the device to determine what PMBus commands are supported. To add a standard command simply modify the bit mask and the GUI will automatically display the new command. Please contact Texas Instruments for details on the use of this tool.

A.8.4.2 Configuring EVM with GUI

In the Configure tab, change configuration is made simple. For example, to configure CPCC, the CPCC control can be accessed by clicking the drop down arrow next to the Value/Edit box on the CPCC[MFR 36] line as shown in Figure 57. As we mentioned before, maximum current 36A and maximum power 360W. Please consult Texas Instruments if there is any uncertainty to be resolved.



Configuration

Command	Code	Value/Edit	Hex/Edit
▼ Configuration			
CPCC [MFR 36]	0xF4	Click...	0x01...
DEADBAND_CONFIG [MFR 26]	0xEA	Click...	0x01...
FREQUENCY_SWITCH	0x33	200.0 kHz	0x00C8
IDEAL DIODE EMUL CONFIG	0xFE	Enabled	0x01
LIGHT_LOAD_CONFIG [MFR 02]	0xD2	Click...	0x00...
VFF_CONFIG [MFR 42]	0xFA	Enabled	0x01
VOUT_COMMAND	0x21	12.000 V	0x1800
VOUT_MODE	0x20	EXP -9	0x17
VOUT_TRANSITION_RATE	0x27	1.000 mV/µs	0x0001
▼ Limits			
IIN_OC_FAULT_LIMIT	0x5B	16.00 A	0x0010
IOUT_OC_FAULT_LIMIT	0x46	38.00 A	0x0026
OT_FAULT_LIMIT	0x4F	50 °C	0x0032
VIN_OFF	0x36	35.000 V	0x0023
VIN_ON	0x35	37.000 V	0x0025
VIN_OV_FAULT_LIMIT	0x55	75.000 V	0x004B
VIN_UV_FAULT_LIMIT	0x59	33.000 V	0x0021
VOUT_OV_FAULT_LIMIT	0x40	14.000 V	0x1C00
VOUT_UV_FAULT_LIMIT	0x44	3.000 V	0x0600

Command	Code	Value/Edit	Hex/Edit
▼ Manufacturer Info			
CMDS_DCDC_NONPAGED [MFR 21]	0xE5	Click...	0x10...
CMDS_DCDC_PAGED [MFR 20]	0xE4	Click...	0x00...
DEVICE_ID [MFR 45]	0xFD	UCD3100ISO1	0x55...
IC_DEVICE_ID	0xAD	UCD3138RHA	0x55...
IC_DEVICE_REV	0xAE	0	0x3000
MFR_DATE	0x9D	121115	0x31...
MFR_ID	0x99	TI	0x54...
MFR_LOCATION	0x9C	Dallas, TX	0x44...
MFR_MODEL	0x9A	UCD3138HS...	0x55...
MFR_REVISION	0x9B	A	0x4100
MFR_SERIAL	0x9E	121115	0x31...
PMBUS_REVISION	0x98	1.2,1.2 - Part	0x42
SETUP_ID [MFR 23]	0xE7	VERSIO...	0x56...
▼ On/Off Configuration			
POWER_GOOD_OFF	0x5F	11.000 V	0x1600
POWER_GOOD_ON	0x5E	11.500 V	0x1700
TON_RISE	0x61	20.0 ms	0x0014
▼ Status			
READ_DEBUG_BUFFER1 [MFR 32]	0xF0	Click...	0x01...
READ_FREQUENCY	0x95	0.0 kHz	0x0000
READ_IOUT	0x8C	0.00 A	0x5800
READ_TEMP_EXTERNAL	0x8E	-353 °C	0xFD3E
READ_TEMP_INTERNAL	0x8D	22 °C	0xDAB6
READ_VIN	0x88	28.750 V	0xDB98
READ_VOUT	0x8B	0.000 V	0x0000
STATUS_BYTE	0x78	00000000	0x00
STATUS_WORD	0x79	Click...	0x0000

Figure 57. Configure CPCC

As one more example, in the following, we will describe how to configure the dead time. Configure other functins are made in the simular way. Again, please consult Texas Instruments if there is any uncertainty to be resolved before making your configuration.

A.8.4.3 Configuring Dead Time

Click the drop down arrow next to the Value/Edit box on the DEADBAND_CONFIG [MFR 26] line, a dialogue box of Figure 58 is present to allow configuring the dead time.

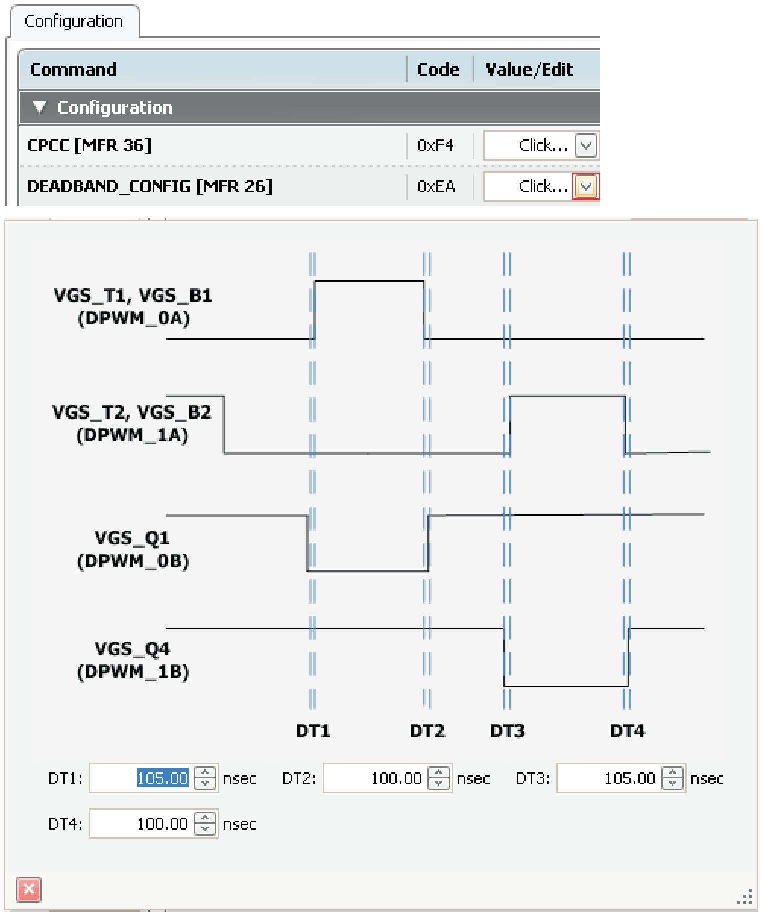


Figure 58. Configuring Dead Time

A.8.5 Tuning Control Loop Using GUI Design

A.8.5.1 Options to Program Digital Control Loop

The GUI comes equipped with 3 different ways to program the UCD3138 digital control loop compensator. Table 9 lists the three options, (a) using K_0, fz, Qz, and fp; (b) using K0, fz1, fz2, and fp; (c) using Kp, Ki, Kd, and α.

In option (c), the compensator is described by Device PID. In this context, Kp, Ki, Kd and α are the raw register values used to configure the positions of the poles and zeros of the compensator. SC is a gain scaling term. Although it is normally set to zero it provides additional gain for situations where the power stage gain may be low. PRD is used to configure the minimum operating period and KCOMP is used to configure the maximum operating period. In the context of the compensator they are simply gain terms that modify the overall transfer function by a fixed value. It is important to be aware that the proper way to configure PRD and KCOMP varies based on the control topology implemented.

Table 9. Programming Digital Control Loop

SYSTEM NAME	TRANSFER FUNCTIONS
Complex Zeros (K_0, f_z, Q_z, f_p)	$\dfrac{\dfrac{s^2}{(2\times\pi\times f_z)^2}+\dfrac{s}{2\times\pi\times f_z\times Q_z}+1}{\dfrac{s}{2\times\pi\times K_0}\times\left(\dfrac{s}{2\times\pi\times f_p}+1\right)}$
Real Zeros (K_0, f_{z1}, f_{z2}, f_p)	$\dfrac{\dfrac{s^2}{(2\times\pi\times f_z)^2}+\dfrac{s}{2\times\pi\times f_z\times Q_z}+1}{\dfrac{s}{2\times\pi\times K_0}\times\left(\dfrac{s}{2\times\pi\times f_p}+1\right)}$
Device PID (K_p, K_i, K_d, α)	$1000\times\left(K_p+K_i\times\dfrac{1+z^{-1}}{1-z^{-1}}+K_d\times\dfrac{1-z^{-1}}{1-\alpha\times2^{-8}\times z^{-1}}\right)\times2^{-SC}\times KCOMP\times2^{-19}\times\dfrac{1}{2^4\times(PRD+1)}$

The compensator of this EVM is configured to acquire one sample per switching cycle, Ts, as defined by Equation (17) where TDPWM = 250 ps,

$$T_s = 16\times(PRD+1)\times T_{DPWM} \tag{17}$$

When the converter operates in PWM mode KCOMP = PRD and the “Device PID” option in Table 9 is expressed in Equation (16) which correctly describes the behavior of the compensator. For clarity Equation (18) displays the exact transfer function used in PWM mode operation.

$$1000\times\left(K_p+K_i\times\frac{1+z^{-1}}{1-z^{-1}}+K_d\times\frac{1-z^{-1}}{1-\alpha\times2^{-8}\times z^{-1}}\right)\times\frac{2^{-SC}\times PRD\times2^{-19}}{2^4\times(PRD+1)} \tag{18}$$

Equation (18) is based on a fixed sample rate. This means Equation (18) is assumed with one switching frequency. The value of that frequency is inside the variable z;

$$z = e^{sT_s} \tag{19}$$

where Ts is the switching period, i.e., the reciprocal of the switching frequency. Let’s make it clear: in PWM mode, the switching frequency is fixed say at 200kHz such that Ts is a fixed and the only value. Figure 59 shows an example of Bode plot output from the GUI. Figure 60 shows the PID coefficients used. Figure 61 shows the schematics used to obtain the Bode Plots in Figure 59 with the PID coefficients shown in Figure 60.

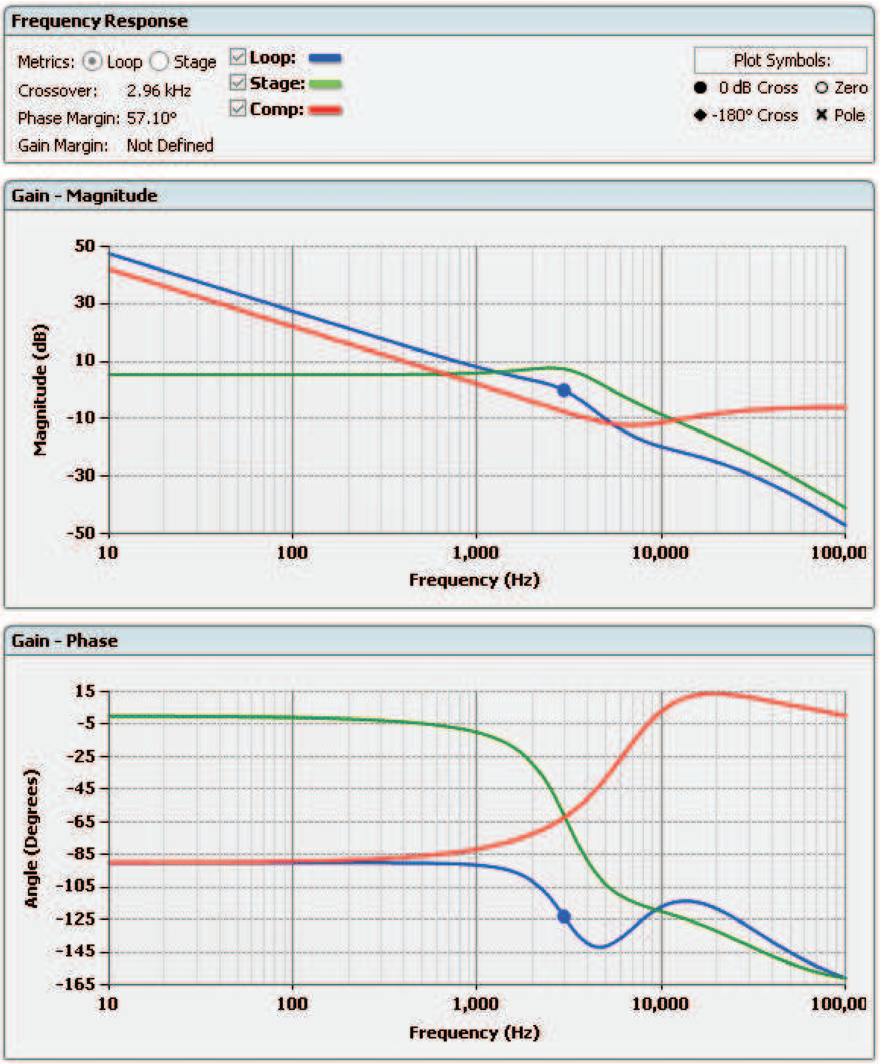


Figure 59. Bode Plots from GUI

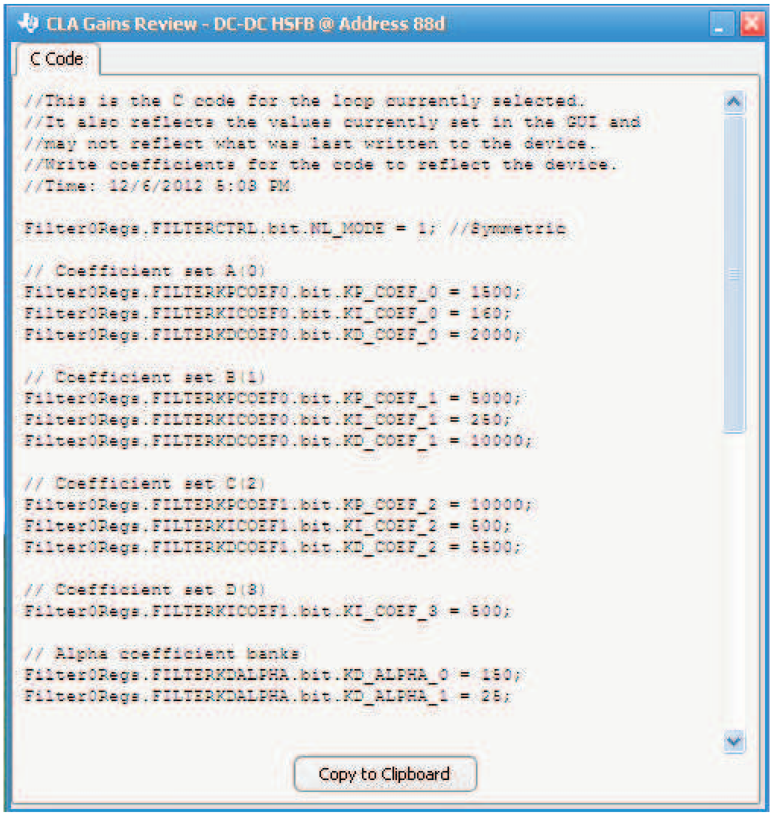


Figure 60. PID Coefficients Used in Voltage Loop

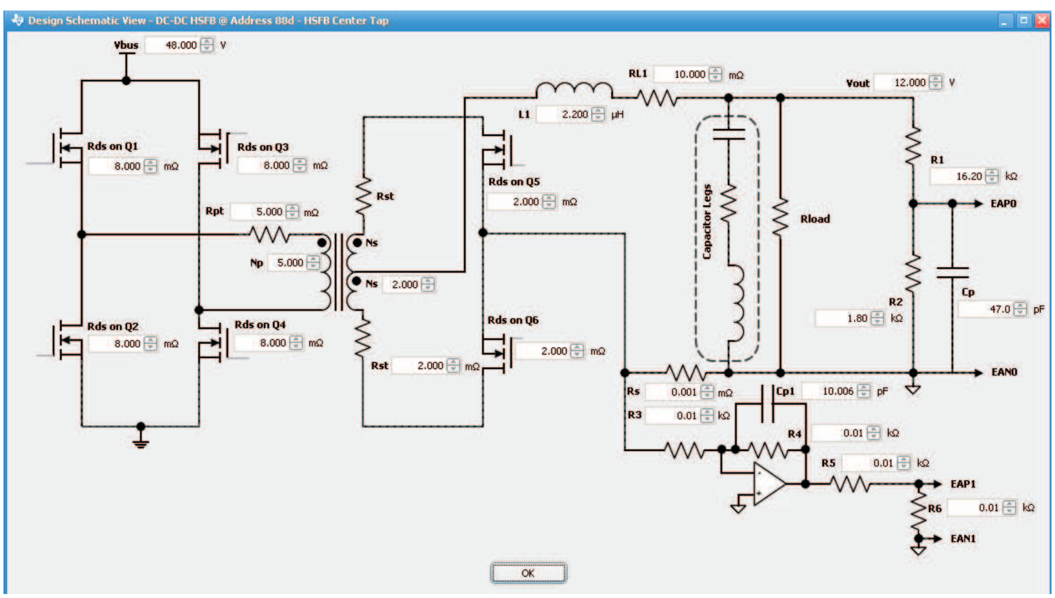


Figure 61. The Schematics Used in the Bode Plots Calculation

A.9 Firmware Development for HSFB Power Converter

Please contact TI for additional information regarding UCD3138 digital HSFB firmware development.

A.10 References

1. UCD3138 Datasheet, *Highly Integrated Digital Controller for Isolated Power*, (Texas Instruments, Literature Number SLUSAP2), 2012
2. UCD3138CC64EVM-030 Evaluation Module and User's Guide, *Programmable Digital Power Controller Control Card Evaluation Module*, (Texas Instruments Literature Number SLUU886), 2012
3. TI Application Manual, *UCD3138 Digital Power Peripherals Programmer's Manual*, (Texas Instruments Literature Number SLUU995)
4. TI Application Manual, *UCD3138 Monitoring and Communications Programmer's Manual*, (Texas Instruments Literature Number SLUU996)
5. TI Application Manual, *UCD3138 ARM and Digital System Programmer's Manual*, (Texas Instruments Literature Number SLUU994)
6. User Guide, *UCD3138 Isolated Power Fusion GUI*, (please contact TI). Note this User Guide is also available in the GUI after installation.

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- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
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