

CMOS Digital Integrated Circuit Silicon Monolithic

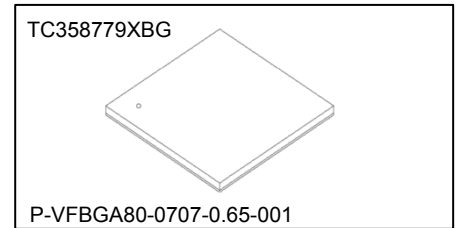
TC358779XBG

Mobile Peripheral Devices

Overview

The HDMI-RX to MIPI DSI-TX is a bridge device that converts HDMI® stream to MIPI® DSI while providing de-interlacing and auto-scaling features.

TC358779XBG share the same 80-pin package as that of TC358749XBG.



Weight: 77mg (Typ.)

Features

- HDMI-RX Interface
 - ✧ HDMI® 1.4b
 - Video Formats Support (Up to 1080P @60fps)
 - RGB, YCbCr444: 24-bpp @60fps
 - YCbCr422 24-bpp @60fps
 - Audio Supports
 - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
 - 3D Support
 - HDCP1.3 Support
 - EDID Support
 - Release A, Revision 1 (Feb 9, 2000)
 - First 128 byte (EDID 1.3 structure)
 - First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
 - Embedded 1 K-byte SRAM (EDID_SRAM)
 - Maximum HDMI® clock speed: 165 MHz
 - ✧ Does not support Audio Return Path and HDMI® Ethernet Channels
- DSI TX Interface
 - ✧ MIPI DSI compliant (Version 1.1 22 November 2011)
 - ✧ Supports up to 4 data lanes @1Gbps/lane
 - ✧ Supports video data formats
 - RGB888 or RGB666
- I²C Slave Interface
 - ✧ Support for normal (100 kHz), fast mode (400 kHz) and ultra-fast mode (2 MHz)
 - ✧ Configure all TC358779XBG internal registers
 - ✧ Support 2 I²C Slave Addresses (7'h0F & 7'h1F) selected through boot-strap pin (INT)
- Audio Output Interface

Any of the three audio interfaces are available: I2S, TDM or IEC60958 (pins are multiplexed)

 - ✧ I2S Audio Interface
 - Up to 4 data lanes for 8-channel data
 - Support Master Clock mode only
 - Support 16, 18, 20 or 24-bit data (depend on HDMI® input stream)
 - Support Left or Right-justify with MSB first
 - Support 32 bit-wide time-slot only
 - Output Audio Over Sampling clock (256fs)
 - Support IEC 60958 & 61937 formats (depending upon HDMI® input stream) over I2S
 - Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12 MHz
 - ✧ TDM (Time Division Multiplexed) Audio Interface
 - Fixed to 8 channels
 - Support Master Clock mode only
 - Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI® input stream)
 - Support 32 bit-wide time slot only
 - Output Audio OverSampling clock (256fs)
 - ✧ Digital Audio Interface
 - Supports 2 channels (any 2 of the total 8) (depend on HDMI® input stream)
 - Support IEC 60958 & 61937 formats (depending upon HDMI® input stream)
- Video Processing
 - ✧ Input formats accepted:
 - RGB or YCbCr422
 - Interlaced or Progressive
 - 2D or 3D
 - Limited to 165 MHz PClk, 640×480, 720×480, 720×576, 1280×720 or 1920×1080 are expected when scalar is used
 - ✧ Output formats supported:
 - RGB888 or RGB666
 - Interlaced (in case of no video processing) or Progressive
 - 2D or 3D
 - Limited by 4Gbps D-PHY bandwidth, 720×480, 1280×720 or 1920×1080 are expected when scalar is invoked

✧ Scaling:

- Hardware performs scaling automatically based on input and output frame size
 - HDMI Rx received input frame size and Panel size programmed in registers
 - Can be overwritten by Software if necessary
- Horizontal Scaling factors supported:
 - 3-to-2, 1-to-2, 3-to-4, 3-to-8, 9-to-4 and 9-to-16
 - 2-to-3 and 1-to-3
- Vertical Scaling factors supported:
 - 1-to-2, 3-to-2 and 3-to-4
 - 2-to-1 and 3-to-1
 - 2-to-3 and 4-to-9
 - 4-to-5 and 8-to-15
- Special handling of 3D formats FP, SBS & T&B to avoid boundary artifacts.

✧ Color Space Conversion

- RGB ⇔ YCbCr
- Two sets of coefficients provided – 1 set for each direction
- Both color space convertors can be enabled/disabled independent of each other.

● InfraRed (IR)

- ✧ Support NEC InfraRed protocol.

● System

- ✧ Internal core has two power domains (VDDC1 and VDDC2)
 - VDDC1 is “always-on” power domain
 - VDDC2 can be shut-off during deep sleep mode

● Power supply inputs

- ✧ Core and MIPI D-PHY: 1.2 V
- ✧ I/O: 1.8 V – 3.3 V
- ✧ HDMI@: 3.3 V
- ✧ VPLL: 1.2 V

Table of content

REFERENCES..... 5

1. Overview 6

2. Features 7

3. External Pins 10

 3.1. Pin Summary 12

 3.2. Pin Layout..... 12

4. Major Functional Blocks 13

5. Package 14

6. Electrical Characteristics 15

 6.1. Absolute Maximum Ratings 15

 6.2. Recommended Operating Condition..... 15

 6.3. DC Electrical Specification..... 16

7. Revision History 17

RESTRICTIONS ON PRODUCT USE 18

Table of Figures

Figure 1.1 TC358779XBG System Overview 6

Figure 3.1 TC358779XBG 80-Pin Layout Package (Top View)..... 12

Figure 4.1 Block Diagram of TC358779XBG..... 13

List of Tables

Table 3.1 TC358779XBG Pin Name..... 10

Table 3.2 Pin Count Summary – TC358779XBG 12

Table 5.1 Mechanical Dimension for TC358779XBG 14

Table 7.1 Revision History..... 17

- HDMI is a trademark or registered trademark of HDMI Licensing, LLC in the United States and/or other countries.
- MIPI and SLIMbus are registered trademarks of MIPI Alliance, Inc.

REFERENCES

1. MIPI D-PHY, “MIPI_D-PHY_specification_v01-00-00, May 14, 2009”
2. MIPI DSI, “MIPI Alliance Specification for Display Serial Interface (DSI) Version 1.1 Revision 22 Nov 2011”
3. HDMI®, “High-Definition Multimedia Interface Specification Version 1.4b March 4, 2010”
4. I²C bus specification, version 2.1, January 2000, Philips Semiconductor
5. IEC 60958, Digital Audio Interface, First Edition, 1999
6. IEC 61937, Digital audio – Interface for non-linear PCM encoded audio bit streams
7. MIPI SlimBus, “MIPI Alliance Specification for Serial Low-power Inter-chip Media Bus (SLIMbus) Version 1.01.01 – 14 July 2008”

1. Overview

The HDMI-RX to MIPI DSI-TX is a bridge device that converts HDMI® stream to MIPI® DSI while providing de-interlacing and auto-scaling features.

System Overview block diagrams are shown below. TC358779 XBG share the same 80-pin package as that of TC358749XBG.

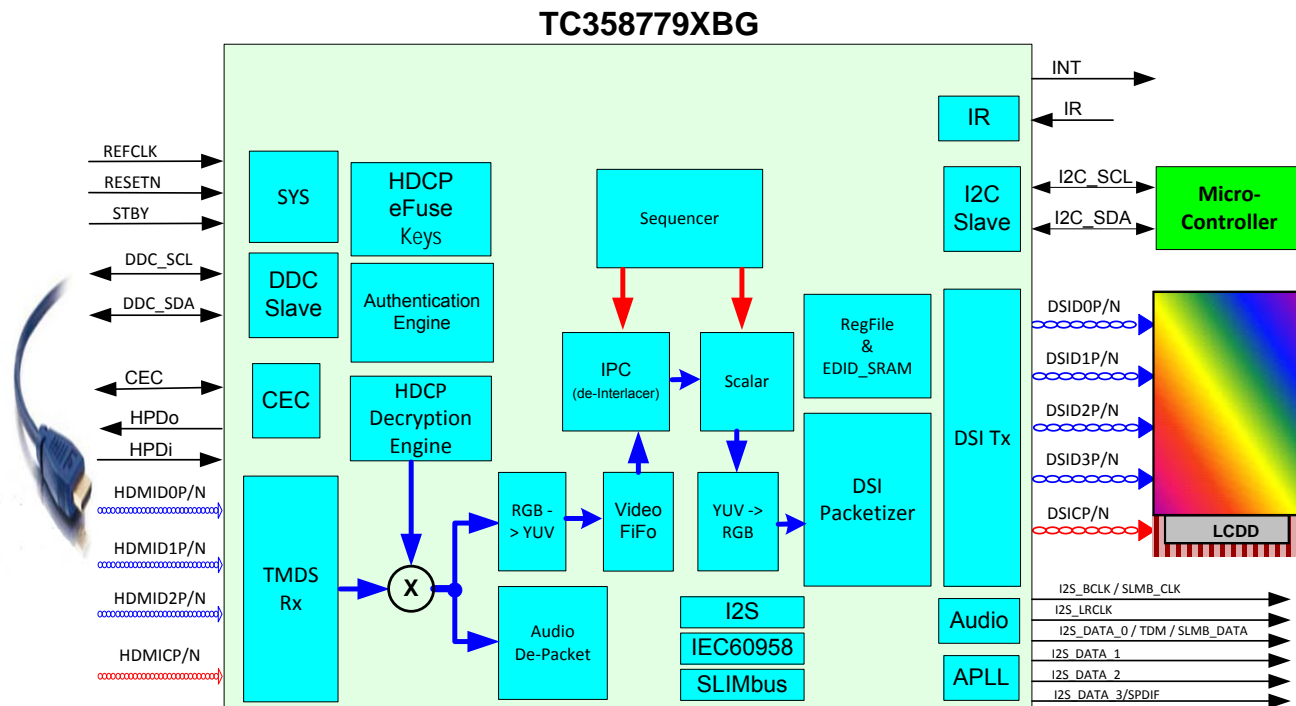


Figure 1.1 TC358779XBG System Overview

2. Features

Below are the main features supported by TC358779XBG.

- HDMI-RX Interface
 - ✧ HDMI® 1.4b
 - Video Formats Support (Up to 1080P @60fps)
 - RGB, YCbCr444: 24-bpp @60fps
 - YCbCr422 24-bpp @60fps
 - Audio Supports
 - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
 - 3D Support
 - HDCP1.3 Support
 - EDID Support
 - Release A, Revision 1 (Feb 9, 2000)
 - First 128 byte (EDID 1.3 structure)
 - First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
 - Embedded 1K-byte SRAM (EDID_SRAM)
 - Maximum HDMI® clock speed: 165 MHz
 - ✧ Does not support Audio Return Path and HDMI® Ethernet Channels
- DSI TX Interface
 - ✧ MIPI DSI compliant (Version 1.1 22 November 2011)
 - ✧ Supports up to 4 data lanes @1Gbps/lane
 - ✧ Supports video data formats
 - RGB888 or RGB666
- I²C Slave Interface
 - ✧ Support for normal (100 kHz), fast mode (400 kHz) and ultra-fast mode (2 MHz)
 - ✧ Configure all TC358779XBG internal registers
 - ✧ Support 2 I²C Slave Addresses (7'h0F & 7'h1F) selected through boot-strap pin (INT)
- Audio Output Interface

Any of the three audio interfaces are available: I2S, TDM or IEC60958 (pins are multiplexed)

 - ✧ I2S Audio Interface
 - Up to 4 data lanes for 8-channel data
 - Support Master Clock mode only
 - Support 16, 18, 20 or 24-bit data (depend on HDMI® input stream)
 - Support Left or Right-justify with MSB first
 - Support 32 bit-wide time-slot only
 - Output Audio Over Sampling clock (256fs)
 - Support IEC 60958 & 61937 formats (depending upon HDMI® input stream) over I2S
 - Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12 MHz

- ✧ TDM (Time Division Multiplexed) Audio Interface
 - Fixed to 8 channels
 - Support Master Clock mode only
 - Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI® input stream)
 - Support 32 bit-wide time slot only
 - Output Audio OverSampling clock (256fs)
- ✧ Digital Audio Interface
 - Supports 2 channels (any 2 of the total 8) (depend on HDMI® input stream)
 - Support IEC 60958 & 61937 formats (depending upon HDMI® input stream)
- Video Processing
 - ✧ Input formats accepted:
 - RGB or YCbCr422
 - Interlaced or Progressive
 - 2D or 3D
 - Limited to 165 MHz PClk, 640×480, 720×480, 720×576, 1280×720 or 1920×1080 are expected when scalar is used
 - ✧ Output formats supported:
 - RGB888 or RGB666
 - Interlaced (in case of no video processing) or Progressive
 - 2D or 3D
 - Limited by 4Gbps D-PHY bandwidth, 720×480, 1280×720 or 1920×1080 are expected when scalar is invoked
 - ✧ Scaling:
 - Hardware performs scaling automatically based on input and output frame size
 - HDMI Rx received input frame size and Panel size programmed in registers
 - Can be overwritten by Software if necessary
 - Horizontal Scaling factors supported:
 - 3-to-2, 1-to-2, 3-to-4, 3-to-8, 9-to-4 and 9-to-16
 - 2-to-3 and 1-to-3
 - Vertical Scaling factors supported:
 - 1-to-2, 3-to-2 and 3-to-4
 - 2-to-1 and 3-to-1
 - 2-to-3 and 4-to-9
 - 4-to-5 and 8-to-15
 - Special handling of 3D formats FP, SBS & T&B to avoid boundary artifacts.
 - ✧ Color Space Conversion
 - RGB ⇔ YCbCr
 - Two sets of coefficients provided – 1 set for each direction
 - Both color space convertors can be enabled/disabled independent of each other.

- InfraRed (IR)
 - ✧ Support NEC InfraRed protocol.

- System
 - ✧ Internal core has two power domains (VDDC1 and VDDC2)
 - VDDC1 is “always-on” power domain
 - VDDC2 can be shut-off during deep sleep mode

- Power supply inputs
 - ✧ Core and MIPI D-PHY: 1.2 V
 - ✧ I/O: 1.8 V – 3.3 V
 - ✧ HDMI®: 3.3 V
 - ✧ VPLL: 1.2 V
 - ✧ Power Consumption during typical operations at room temperature

		VDDC1	VDDC2	VDDIO1	VDDIO2	VDDMIPI	AVDD33	AVDD12	AVDDPLL	Total Power (mW)
		1.2V	1.2V	3.3V	1.8V	1.2V	3.3V	1.2V	1.2V	
1080P @ 60fps	Current (mA)	61.13	0.80	0.89	20.50	72.80	67.82	0.01	421.2	
	Power (mW)	73.36	2.65	1.60	24.60	240.25	81.39	0.01		
720p → 1080p @ 30fps	Current (mA)	170.40	0.80	0.89	20.02	72.66	56.67	1.12	539.23	
	Power (mW)	204.48	2.64	1.60	24.02	239.78	68.00	1.34		

Note:

- TC358779XBG does not perform YCbCr ⇔ YUV conversion. In this document YCbCr, HDMI® terminology, is used to indicate video color space.

3. External Pins

Following table gives the signals of TC358779XBG and their function.

Table 3.1 TC358779XBG Pin Name

Group	Pin Name	I/O	Init (O)	Type	Function	Note
System: Reset & Clock (5)	RESETN	I	-	Sch	System reset input, active low	1.8V -3.3V
	REFCLK	I	-	N	Reference clock input (27/26MHz or 42MHz range)	1.8V -3.3V
	TEST	I	-	N	0: Normal mode 1: Test mode	1.8V -3.3V
	STBY	I	-	N	Standby pin, active low	1.8V -3.3V
	INT	O	L	N	Interrupt Output signal – active high (Level) I ² C Slv_Addr_Sel at boot-strap	1.8V -3.3V
DSI TX (10)	MIPI_CP	O	H	MIPI-PHY	MIPI-DSI clock positive	1.2 V
	MIPI_CN	O	H	MIPI-PHY	MIPI-DSI clock negative	1.2 V
	MIPI_D0P	O	H	MIPI-PHY	MIPI-DSI Data 0 positive	1.2 V
	MIPI_D0N	O	H	MIPI-PHY	MIPI-DSI Data 0 negative	1.2 V
	MIPI_D1P	O	H	MIPI-PHY	MIPI-DSI Data 1 positive	1.2 V
	MIPI_D1N	O	H	MIPI-PHY	MIPI-DSI Data 1 negative	1.2 V
	MIPI_D2P	O	H	MIPI-PHY	MIPI-DSI Data 2 positive	1.2 V
	MIPI_D2N	O	H	MIPI-PHY	MIPI-DSI Data 2 negative	1.2 V
	MIPI_D3P	O	H	MIPI-PHY	MIPI-DSI Data 3 positive	1.2 V
MIPI_D3N	O	H	MIPI-PHY	MIPI-DSI Data 3 negative	1.2 V	
HDMI RX (8)	HDMICP	I	-	HDMI-PHY	HDMI Clock channel positive	3.3V
	HDMICN	I	-	HDMI-PHY	HDMI Clock channel negative	3.3V
	HDMID0P	I	-	HDMI-PHY	HDMI Data 0 channel positive	3.3V
	HDMID0N	I	-	HDMI-PHY	HDMI Data 0 channel negative	3.3V
	HDMID1P	I	-	HDMI-PHY	HDMI Data 1 channel positive	3.3V
	HDMID1N	I	-	HDMI-PHY	HDMI Data 1 channel negative	3.3V
	HDMID2P	I	-	HDMI-PHY	HDMI Data 2 channel positive	3.3V
HDMID2N	I	-	HDMI-PHY	HDMI Data 2 channel negative	3.3V	
DDC (2)	DDC_SCL	OD	-	FS-SOD	DDC Slave Clock	3.3V ^(Note1)
	DDC_SDA	OD	-	FS-SOD	DDC Slave data	3.3V ^(Note1)
CEC	CEC	OD	-	FS-SOD	CEC signal	3.3V
HPD (2)	HPDI	I	-	N	Hot Plug Detect Input	3.3V ^(Note1)
	HPDO	O	L	N	Hot Plug Detect Output	3.3V
Audio (7)	A_SCK	O	L	N	I2S/TDM Bit/SLIMbus Clock signal	1.8V -3.3V
	A_WFS	O	L	N	I2S Word Clock or TDM Frame Sync signal	1.8V -3.3V
	A_SD[0]	O	L	N	I2S (ch. 0,1)/TDM/SLIMbus data signal	1.8V -3.3V
	A_SD[2:1]	O	LL	N	I2S (ch. 2,3,4,5) data signal	1.8V -3.3V
	A_SD[3]	O	L	N	I2S (ch. 6,7) data/SPDIF signal	1.8V -3.3V
	A_OSCK	O	L	N	Audio Over Sampling Clock	1.8V -3.3V
IR	IR	I	-	Sch	InfraRed signal	1.8V -3.3V
I2C (2)	I2C_SCL	OD	-	FS-SOD	I ² C serial clock	1.8V -3.3V
	I2C_SDA	OD	-	FS-SOD	I ² C serial data	1.8V -3.3V
APLL (4)	BIASDA	O	L	-	BIAS signal	-
	DAOUT	O	H	-	Audio PLL clock Reference Output clock	-
	PCKIN	I	-	-	Audio PLL Reference Input clock	-
	PFIL	O	L	-	Audio PLL Low Pass Filter signal	-
POWER (11)	VDDC1	-	-	-	VDD for Internal Core (always ON) (1)	1.2V
	VDDC2	-	-	-	VDD for Internal Core (can be powered down) (2)	1.2V
	VDDIO1	-	-	-	VDDIO1 IO power supply (1)	3.3V
	VDDIO2	-	-	-	VDDIO2 IO power supply (1)	1.8V - 3.3V
	VDD_MIPI	-	-	-	VDD for the MIPI DSI (1)	1.2V
	VDD_PLL11	-	-	-	VDD for PLL11 (1)	1.2V
	AVDD12	-	-	-	HDMI PHY 1.2V power supply (2)	1.2V
	AVDD33	-	-	-	HDMI PHY & APLL 3.3V power supply (2)	3.3V
Ground (25)	VSS	-	-	-	Ground (25)	-
Misc	REXT ^(Note2)	-	-	-	External Reference Resistor	-
	VPGM ^(Note3)	-	-	-	eFuse program power supply	-

Total 80 pins

Note1: These IO are 5 V tolerant.

Note2: Please connect REXT to AVDD33 with a 2 k Ω resistor ($\pm 1\%$)

Note3: Please tie to ground

Buffer Type Abbreviation:

N: Normal IO

FS-SOD: Failed Safe Pseudo open-drain output, Schmitt input

Sch: Schmitt input buffer

MIPI-PHY: front-end analog IO for DSI

HDMI-PHY: front-end analog IO for HDMI®

3.1. Pin Summary

Table 3.2 Pin Count Summary – TC358779XBG

Group Name	Pin Count
SYSTEM	5
DSI TX	10
HDMI RX	8
DDC	2
CEC	1
Audio	2
I2C	7
IR	1
HPD	2
APLL	4
POWER	11
GROUND	25
Misc	2
TOTAL	80

3.2. Pin Layout

Top View (through the die)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
AVDD12	REXT	VDDC2	BIASDA	DAOUT	PFIL	VSS	VDD_PLL11	MIPI_D3N	MIPI_D3P
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
AVDD33	VSS	VSS	VSS	VSS	VSS	PCKIN	VSS	MIPI_D2N	MIPI_D2P
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
HDMICP	HDMICN							MIPI_CN	MIPI_CP
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
HDMID0P	HDMID0N		VSS	VSS	VSS	VSS		VSS	VDD_MIPI
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
HDMID1P	HDMID1N		VSS	VSS	VSS	VSS		MIPI_D1N	MIPI_D1P
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
HDMID2P	HDMID2N		VSS	VSS	VSS	VSS		MIPI_D0N	MIPI_D0P
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
AVDD33	VSS		VPGM	TEST	VSS	VSS		VSS	A_OSK
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	CEC							A_SD_0	A_WFS
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
DDC_SCL	DDC_SDA	HPDO	INT	I2C_SCL	IR	REFCLK	VSS	A_SCK	A_SD_1
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
VDDC1	VDDIO1	HPDI	STBY	I2C_SDA	RESETN	VDDIO2	A_SD_3	A_SD_2	VDDC2

Figure 3.1 TC358779XBG 80-Pin Layout Package (Top View)

4. Major Functional Blocks

TC358779XBG consists of the following major blocks: HDMI-RX, DSI Tx, RGB2YCbCr & YCbCr2RGB color convertors, De-Interlacer, Scalar, DDC, CEC, I2S, TDM, IEC60958, INT and I²C i/f.

DDC, CEC and I²C slave controller are always enabled which are required for configuring the TC358779XBG chip and to wake up TC358779XBG chip.

The following sections describe each block in detail. In addition, there is a section that describes Clock generation block.

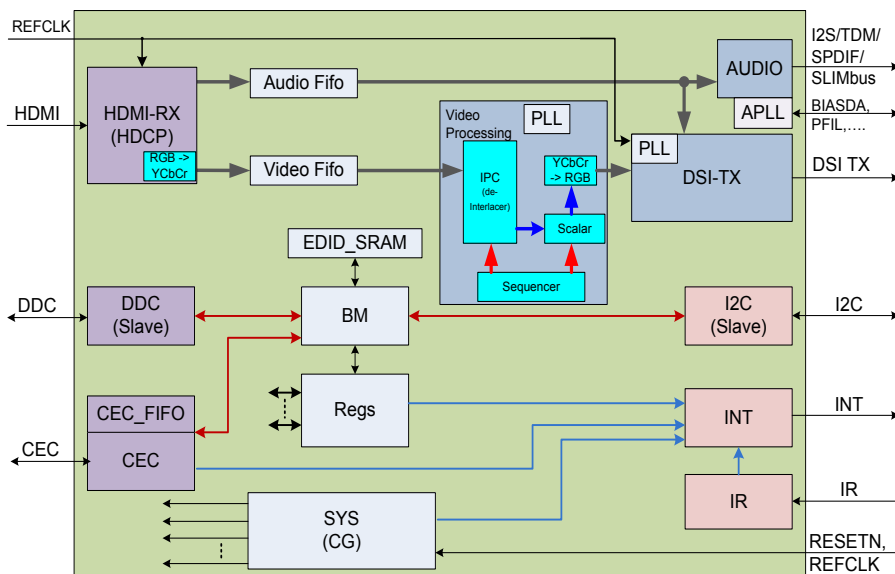
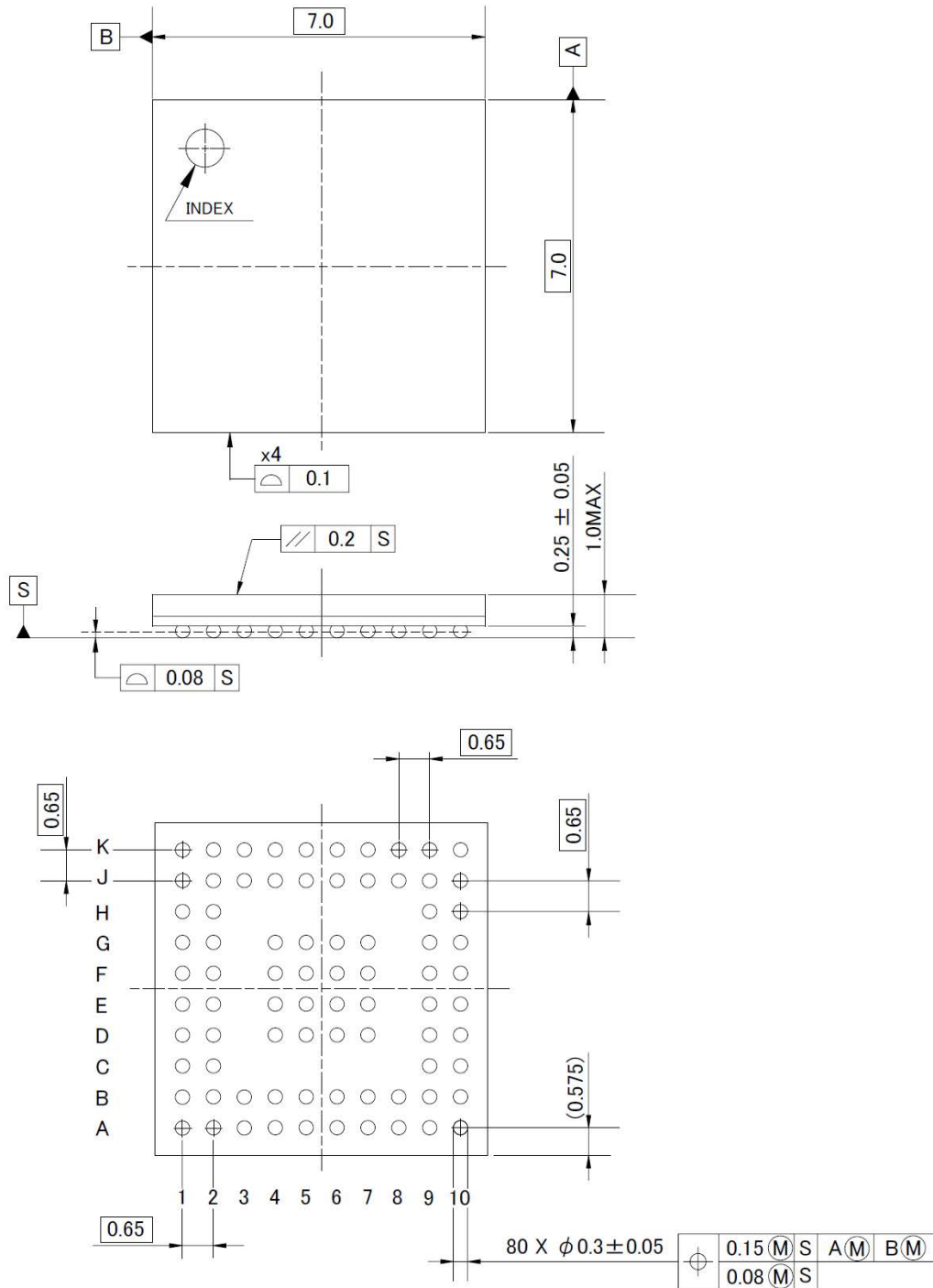


Figure 4.1 Block Diagram of TC358779XBG

5. Package

TC358779XBG Package (80-pin, P-VFBGA80-0707-0.65-001)

Unit: mm



Weight: 77mg (Typ.)

Table 5.1 Mechanical Dimension for TC358779XBG

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.65 mm	-
Package dimension	-	7.0 × 7.0 mm ²	-
Package height	-	-	1.0 mm

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

VSS = 0 V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V - Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2 V - Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2 V - MIPI DSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (3.3 V - HDMIRX PHY)	AVDD33	-0.3 to +3.9	V
Supply voltage (1.2 V - HDMIRX PHY)	AVDD12	-0.3 to +1.8	V
Input voltage (DSI IO)	V _{IN_DSI}	-0.3 to VDD_MIPI+0.3	V
Output voltage (DSI IO)	V _{OUT_DSI}	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	V _{IN_IO}	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	V _{OUT_IO}	-0.3 to VDDIO+0.3	V
Junction temperature	T _j	125	°C
Storage temperature	T _{stg}	-40 to +125	°C

6.2. Recommended Operating Condition

VSS = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8/3.3 V - Digital IO)	VDDIO2	1.65	1.8	3.6	V
Supply voltage (3.3 V - HDMI Digital IO)	VDDIO1	3.0	3.3	3.6	V
Supply voltage (1.2 V - Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (3.3 V - HDMIRX PHY)	AVDD33	3.135	3.3	3.465	V
Supply voltage (1.2 V - HDMIRX PHY)	AVDD12	1.15	1.2	1.25	V
Supply voltage (1.2 V - MIPI DSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T _a	-30	+25	+70	°C
Supply Noise Voltage	V _{SN}	-	-	100	mV _{pp}

6.3. DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input ^{Note1}	V_{IH}	$0.7 \times V_{DDIO}$	-	V_{DDIO}	V
Input voltage, Low level input ^{Note1}	V_{IL}	0	-	$0.3 \times V_{DDIO}$	V
Input voltage High level CMOS Schmitt Trigger ^{Note1,2}	V_{IHS}	$0.7 \times V_{DDIO}$	-	V_{DDIO}	V
Input voltage Low level CMOS Schmitt Trigger ^{Note1,2}	V_{ILS}	0	-	$0.3 \times V_{DDIO}$	V
Output voltage High level ^{Note1, Note2}	V_{OH}	$0.8 \times V_{DDIO}$	-	V_{DDIO}	V
Output voltage Low level ^{Note1, Note2}	V_{OL}	0	-	$0.2 \times V_{DDIO}$	V
Input leak current, High level (Condition: $V_{IN} = +V_{DDIO}$, $V_{DDIO} = 3.6 \text{ V}$)	I_{ILH1} ^(Note4)	-10	-	10	μA
Input leak current, Low level (Condition: $V_{IN} = 0 \text{ V}$, $V_{DDIO} = 3.6 \text{ V}$)	I_{ILL1} ^(Note5)	-10	-	10	μA

Note1: Each power source is operating within recommended operation condition.

Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note4: Normal pin or Pull-up IO pin applied V_{DDIO} supply voltage to V_{in} (input voltage)

Note5: Normal pin applied V_{SS} (0V) to V_{in} (input voltage)

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
0.75	2014-04-10	Newly released
0.821	2015-12-18	Typo Init(O) DAOUT pin in External Pins
0.822	2016-04-01	• Package's weight is rounding up digits after the decimal point to form an integer.
0.823	2016-09-01	1. Typo Correction on DSI-TX (10) on Table 3.1 2. Unified "Phy" to "PHY".

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**