#### 3.2.3.3 Load Test at Different Airflow Conditions

The testing is done with and without the heat sink at different airflow conditions and different duty cycles. The key results are summarized in Table 8 and the effect of airflow at different test conditions are plotted in Figure 32 to Figure 35.

**Table 8. Summary of Load Test Results at Different Conditions**

| VDC (V) | IDC (A) | WINDING CURRENT (RMS) (A) | INPUT POWER (W) | MAXIMUM FET TEMPERATURE | DUTY CYCLE | AIRFLOW (LFM) | TEST CONDITION |
|---|---|---|---|---|---|---|---|
| **TESTING WITHOUT HEAT SINK AT DUTY CYCLE = 1** | | | | | | | |
| 36 | 19.4 | 17.4 | 698.0 | 90.0°C | 1 | 0 | No heat sink |
| 36 | 24.8 | 22.6 | 892.8 | 89.0°C | 1 | 300 | No heat sink |
| 36 | 26.6 | 24.4 | 957.6 | 90.4°C | 1 | 400 | No heat sink |
| 36 | 28.0 | 25.7 | 1008.0 | 93.0°C | 1 | 500 | No heat sink |
| **TESTING WITHOUT HEAT SINK AT DUTY CYCLE = 0.95** | | | | | | | |
| 36 | 19.3 | 18.6 | 693.036 | 102°C | 0.95 | 0 | No heat sink |
| 36 | 26.1 | 25.2 | 938.952 | 103°C | 0.95 | 400 | No heat sink |
| **TESTING WITHOUT HEAT SINK AT DUTY CYCLE = 1** | | | | | | | |
| 36 | 30.1 | 27.1 | 1085 | 107°C | 1 | 0 | With heat sink |
| 36 | 30.0 | 27.1 | 1080 | 84°C | 1 | 100 | With heat sink |
| **TESTING WITH HEAT SINK AT DUTY CYCLE = 0.95** | | | | | | | |
| 36 | 26.2 | 25.3 | 942.678 | 99.0°C | 0.95 | 0 | With heat sink |
| 36 | 28.5 | 27.5 | 1024.650 | 81.0°C | 0.95 | 100 | With heat sink |
| 36 | 28.5 | 27.5 | 1024.650 | 70.2°C | 0.95 | 200 | With heat sink |

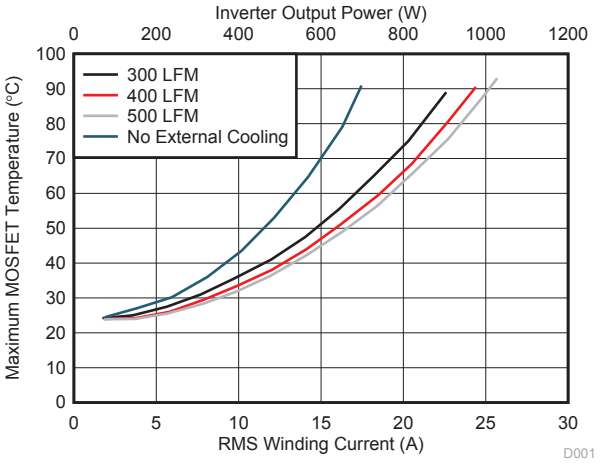


**Figure 32. Load Test Results at 36-V DC Input, 100% Duty Cycle Without Heat Sink at Different Airflow**

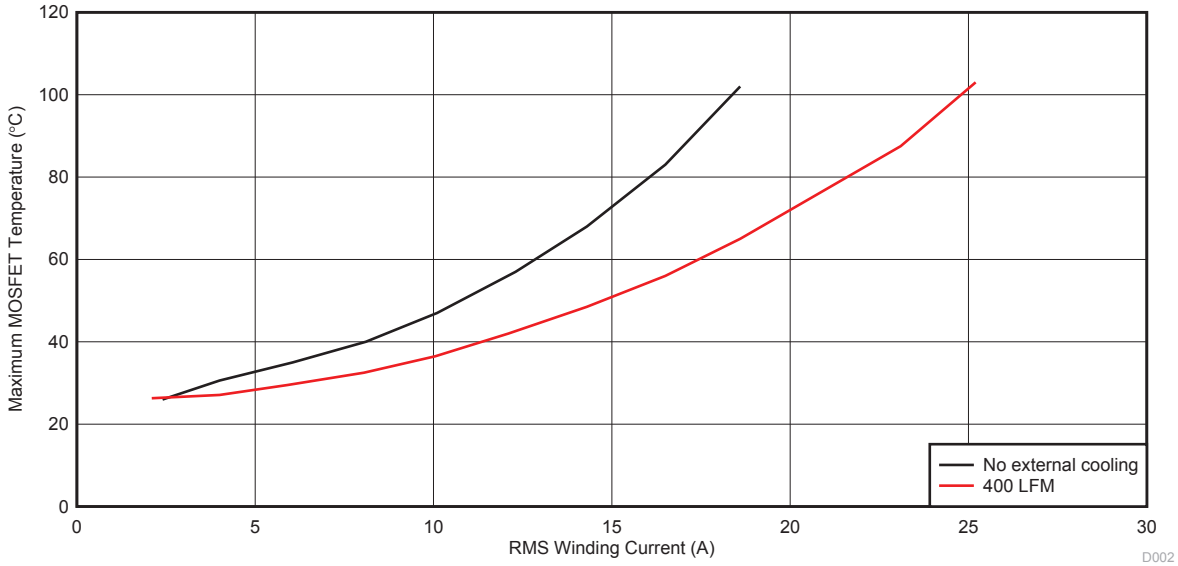


**Figure 33. Load Test Results at 36-V DC Input, 95% Duty Cycle Without Heat Sink at Different Airflow**

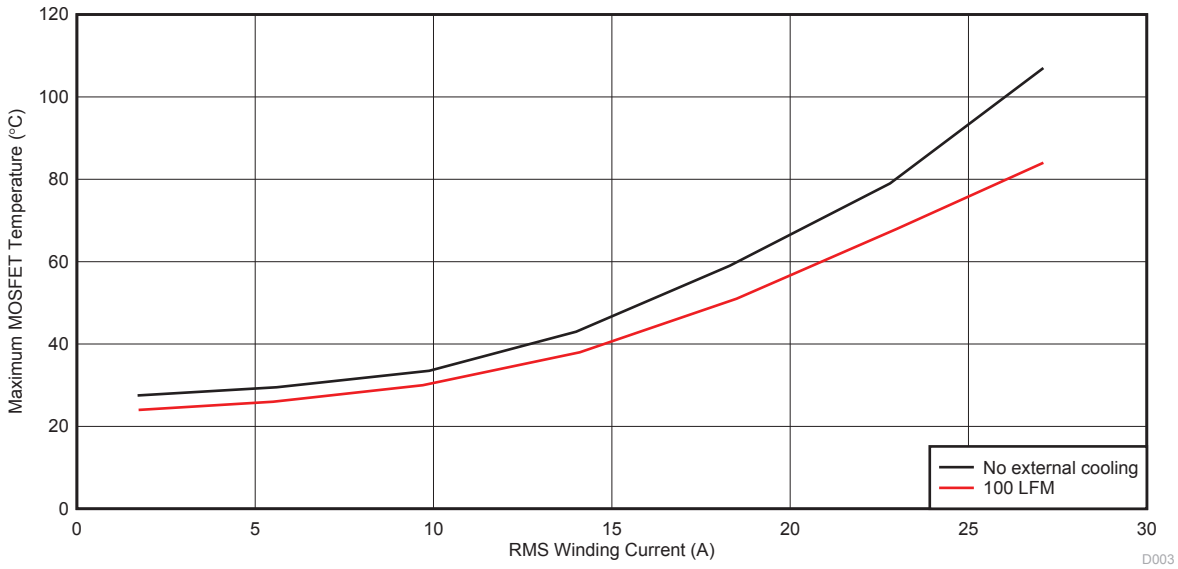


**Figure 34. Load Test Results at 36-V DC Input, 100% Duty Cycle With Heat Sink at Different Airflow**

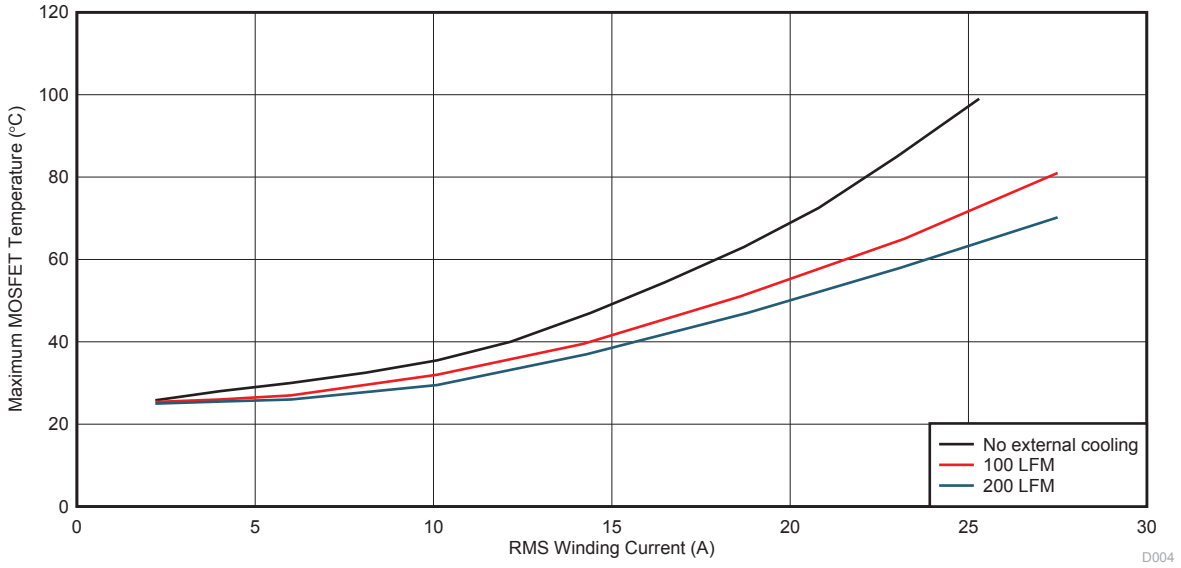


**Figure 35. Load Test Results at 36-V DC Input, 95% Duty Cycle With Heat Sink at Different Airflow**

### 3.2.4 Inverter Efficiency

The inverter efficiency is experimentally tested with a load setup as shown in Figure 15. The test results without a heat sink and at a 100% duty cycle are listed in Table 9. The test results without a heat sink and at a 95% duty cycle are listed in Table 10.

**Table 9. Inverter Efficiency Test Results at 100% Duty Cycle Without Heat Sink and Without Airflow**

| INPUT DC VOLTAGE (V) | INPUT DC CURRENT (A) | RMS WINDING CURRENT (A) | DC INPUT POWER (W) | INVERTER OUTPUT POWER (W) | INVERTER EFFICIENCY | INVERTER LOSS (W) |
|---|---|---|---|---|---|---|
| 36.11 | 2.53 | 2.12 | 91.44 | 90.99 | 99.51% | 0.45 |
| 35.95 | 7.10 | 5.99 | 255.32 | 254.46 | 99.66% | 0.86 |
| 35.91 | 11.77 | 10.13 | 422.76 | 420.81 | 99.54% | 1.95 |
| 35.92 | 16.34 | 14.31 | 586.91 | 582.81 | 99.30% | 4.10 |
| 35.81 | 20.83 | 18.57 | 745.80 | 739.10 | 99.10% | 6.70 |
| 35.75 | 25.33 | 22.87 | 905.51 | 895.15 | 98.86% | 10.36 |

**Table 10. Inverter Efficiency Test Results at 95% Duty Cycle Without Heat Sink and Without Airflow**

| INPUT DC VOLTAGE (V) | INPUT DC CURRENT (A) | RMS WINDING CURRENT (A) | DC INPUT POWER (W) | INVERTER OUTPUT POWER (W) | INVERTER EFFICIENCY | INVERTER LOSS (W) |
|---|---|---|---|---|---|---|
| 36.06 | 2.21 | 1.93 | 79.72 | 79.03 | 99.14% | 0.69 |
| 35.90 | 6.65 | 5.85 | 238.76 | 237.51 | 99.48% | 1.25 |
| 35.84 | 11.12 | 10.04 | 398.66 | 396.08 | 99.35% | 2.58 |
| 35.97 | 15.48 | 14.25 | 556.81 | 551.60 | 99.06% | 5.21 |
| 35.99 | 19.76 | 18.53 | 711.37 | 702.68 | 98.78% | 8.69 |
| 36.02 | 24.00 | 22.86 | 864.37 | 851.69 | 98.53% | 12.68 |

The test results without a heat sink but with a 300LFM airflow and at a 100% duty cycle are listed in Table 11. The test results without a heat sink but with a 300LFM airflow and at a 95% duty cycle are listed in Table 12.

**Table 11. Inverter Efficiency Test Results at 100% Duty Cycle Without Heat Sink and at 300LFM Airflow**

| INPUT DC VOLTAGE (V) | INPUT DC CURRENT (A) | RMS WINDING CURRENT (A) | DC INPUT POWER (W) | INVERTER OUTPUT POWER (W) | INVERTER EFFICIENCY | INVERTER LOSS (W) |
|---|---|---|---|---|---|---|
| 36.19 | 2.35 | 1.95 | 85.12 | 84.69 | 99.49% | 0.43 |
| 35.75 | 7.02 | 5.89 | 251.02 | 250.26 | 99.70% | 0.76 |
| 35.95 | 11.85 | 10.08 | 426.11 | 424.50 | 99.62% | 1.61 |
| 35.96 | 16.62 | 14.30 | 597.50 | 594.17 | 99.44% | 3.33 |
| 36.00 | 21.35 | 18.56 | 768.51 | 763.08 | 99.29% | 5.43 |
| 35.88 | 26.06 | 22.91 | 935.30 | 927.18 | 99.13% | 8.12 |
| 35.88 | 28.45 | 25.40 | 1020.54 | 1010.78 | 99.04% | 9.76 |

**Table 12. Inverter Efficiency Test Results at 95% Duty Cycle Without Heat Sink and at 300LFM Airflow**

| INPUT DC VOLTAGE (V) | INPUT DC CURRENT (A) | RMS WINDING CURRENT (A) | DC INPUT POWER (W) | INVERTER OUTPUT POWER (W) | INVERTER EFFICIENCY | INVERTER LOSS (W) |
|---|---|---|---|---|---|---|
| 36.16 | 2.07 | 1.81 | 74.77 | 74.10 | 99.11% | 0.67 |
| 36.04 | 6.59 | 5.80 | 237.45 | 236.29 | 99.51% | 1.16 |
| 36.02 | 11.08 | 10.02 | 399.27 | 397.02 | 99.43% | 2.26 |
| 36.00 | 15.46 | 14.26 | 556.34 | 552.22 | 99.26% | 4.12 |
| 35.94 | 19.73 | 18.57 | 708.96 | 702.00 | 99.02% | 6.96 |
| 35.90 | 24.07 | 22.89 | 864.20 | 853.33 | 98.74% | 10.87 |
| 35.98 | 26.13 | 25.13 | 940.30 | 927.55 | 98.64% | 12.74 |

The efficiency curve of these test conditions are plotted in Figure 36.

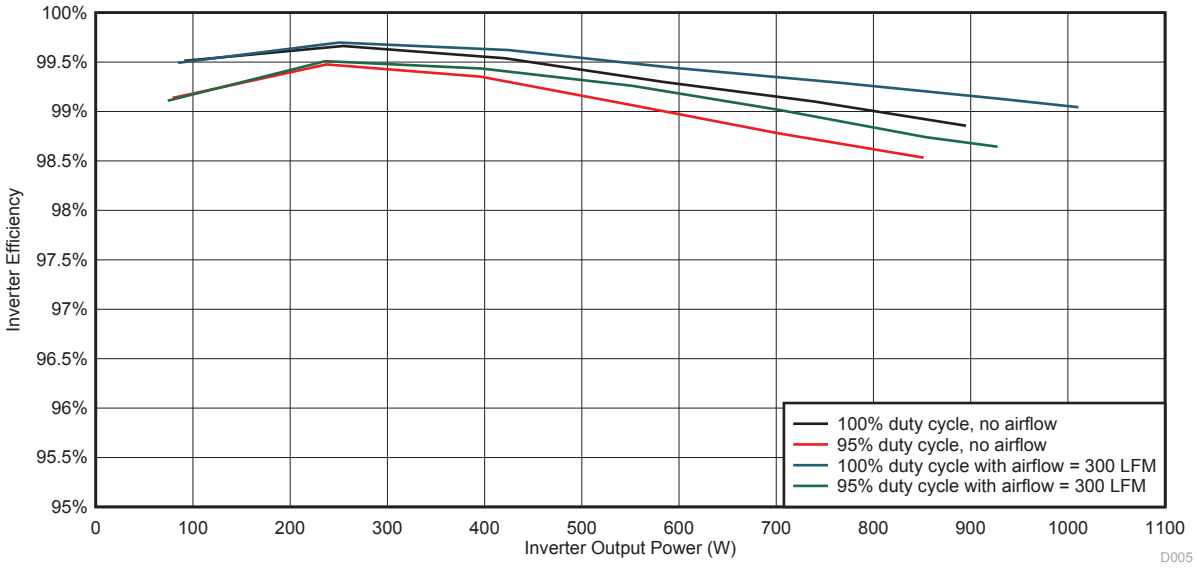


**Figure 36. Inverter Efficiency versus Output Power**

The reference design could achieve the high efficiency due to the following key factors:

- Low $R_{DS\_ON}$ of the MOSFET power block reducing the conduction losses
- Clean FET switching reducing the switching losses and diode losses
- Power block allows small PCB form factor and hence enable low PCB track resistance leads to

minimum PCB losses

- The $V_{GS}$ handshake feature of the gate driver allows minimum dead time, reducing the diode loss.

### 3.2.5 Inverter Current Sensing by $V_{DS}$ Amplification

The inverter leg current sensing is done by monitoring the $V_{DS}$ of the low-side MOSFETs. Figure 37 shows the test results at a 100% duty cycle. As shown in Figure 17, at a 100% duty cycle the low-side FET conducts for a 120-degree electrical period and that corresponds to the negative half cycle of the corresponding phase current waveform as shown in Figure 37. The waveform is captured at the test conditions given in Table 13.

**Table 13. Test Condition for Inverter Current Sensing by $V_{DS}$ Monitoring Using DRV8323**

| PARAMETER | VALUE |
|---|---|
| Measured MOSFET $R_{DS\_ON}$ at 25°C | 1.83 mΩ |
| DRV8323 current sense amplifier gain | 20 V/V |
| DRV8323 current sense amplifier reference voltage | $V_{REF}$/2 = 1.64 V (measured on the board) |
| DRV8323 – $t_{DRIVE}$ | 1 µs |

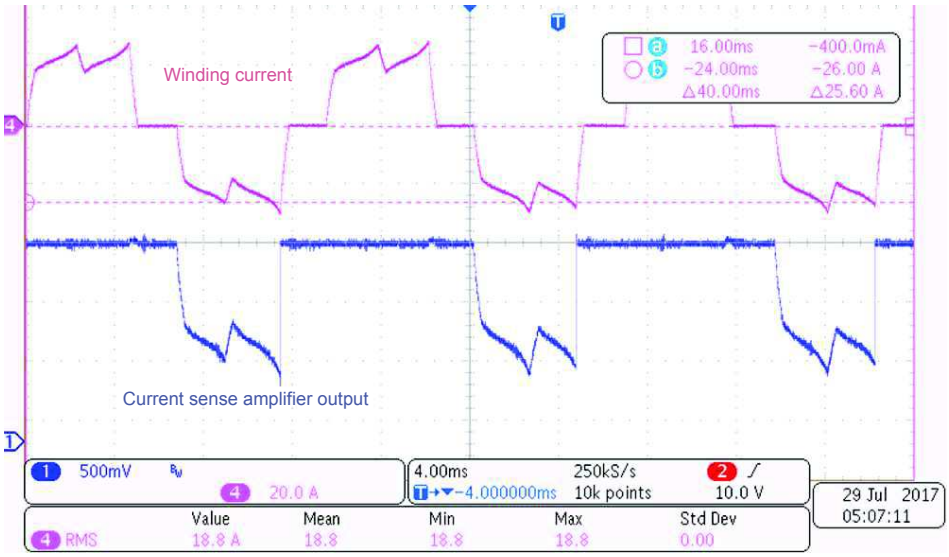


**Figure 37. DRV8323 Current Sense Amplifier Output at 100% Duty Cycle**

Figure 38 shows the test results at a 52% duty cycle. As shown in Figure 17, at a 52% duty cycle the low-side FET conducts for a 120-degree electrical period and conducts complimentary to the top-side PWM during the positive winding current. The waveforms are captured at same conditions as given in Table 13.

Figure 39 shows the PWM zoomed view with these conditions and shows that the sense amplifier output is pretty clean with minimum switching noise, allowing a fast and accurate current sample.

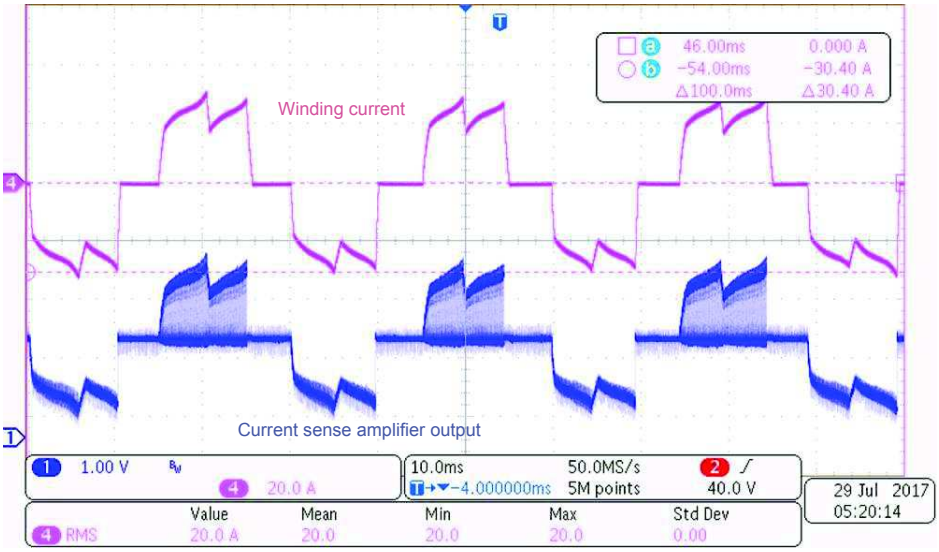


**Figure 38. DRV8323 Current Sense Amplifier Output at 52% Duty Cycle**

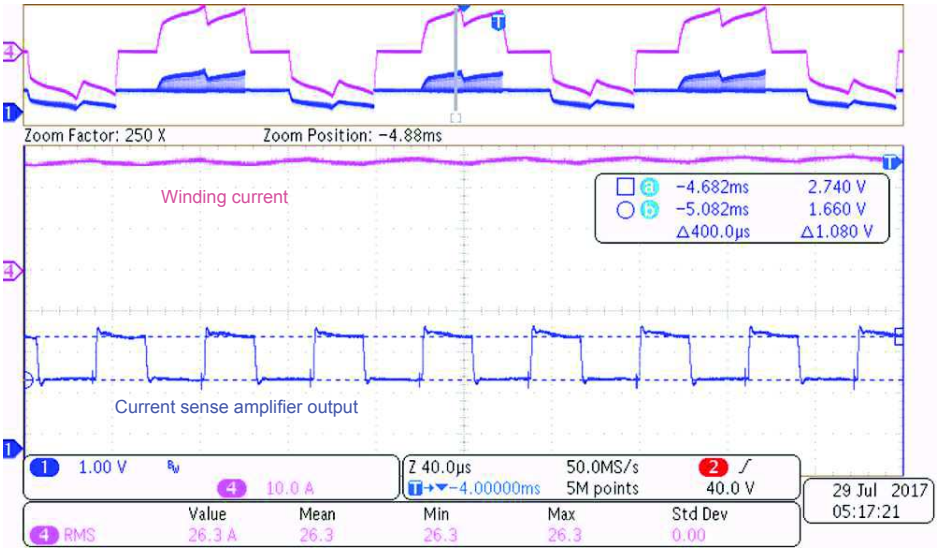


**Figure 39. PWM Cycle View of DRV8323 Current Sense Amplifier Output at 52% Duty Cycle**

### 3.2.6 Overcurrent and Short-Circuit Protection Test

#### *3.2.6.1 Cycle-by-Cycle Overcurrent Protection by $V_{DS}$ Monitoring*

Figure 40 shows the cycle-by-cycle peak current limit by the DRV8323 when the motor is loaded more than the set current limit. The test conditions are specified in Table 14.

**Table 14. Test Condition for Cycle-by-Cycle Overcurrent Protection by DRV8323**

| PARAMETER | VALUE |
|---|---|
| Measured MOSFET $R_{DS\_ON}$ at 25°C | 1.83 mΩ |
| $V_{DS}$ threshold | 0.06 V |
| DRV8323 – $t_{DRIVE}$ | 1 µs |

**Table 14. Test Condition for Cycle-by-Cycle Overcurrent Protection by DRV8323 (continued)**

| PARAMETER | VALUE |
|---|---|
| Duty cycle deglitch time (OCP_DEG) | 2 µs |
| DRV8323 – TDRIVE overcurrent protection mode (OCP_MODE) | Overcurrent causes an automatic retrying fault |

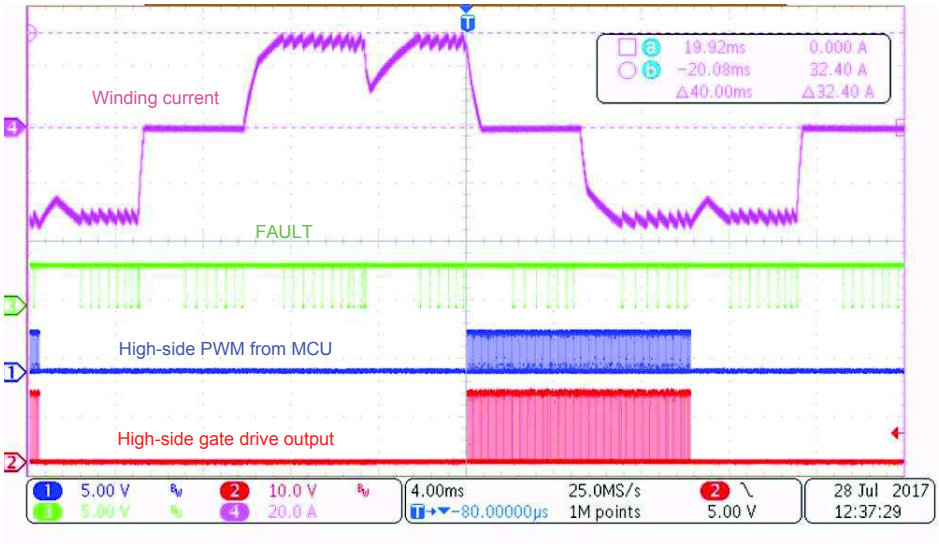


**Figure 40. Cycle-by-Cycle Overcurrent Limit by DRV8323**

Assuming the junction temperature of 75°C, the $R_{DS\_ON}$ at 75°C ≈ 2.379 mΩ (approximately 1.3 times the $R_{DS\_ON}$ at 25°C, from the CSD88599Q5DC datasheet).

Current limit threshold = $V_{DS}$ threshold / $R_{DS\_ON}$ = 25.22 A

Figure 40 shows that the current is limited at 32.4 A. Figure 41 shows the zoomed view where the PWM shuts off when the current hits 32.4 A and the fault is created. The fault reset at the next PWM rising edge.

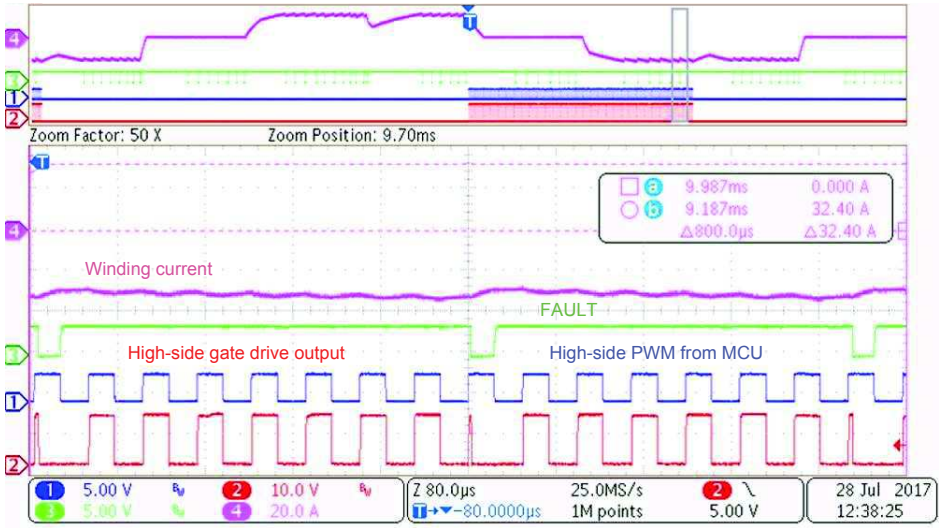


**Figure 41. Cycle-by-Cycle Overcurrent Limit Showing PWM Shutoff**

### 3.2.6.2 Cycle-by-Cycle Short-Circuit Protection by $V_{DS}$ Monitoring

The test conditions as per Table 15 are used for all the test results in this section and Section 3.2.6.3.

**Table 15. Test Conditions for Short-Circuit Protection by $V_{DS}$ Monitoring**

| PARAMETER | VALUE |
|---|---|
| Measured MOSFET $R_{DS\_ON}$ at 25°C | 1.83 mΩ |
| $V_{DS}$ threshold | 0.06 V |
| DRV8323 – $t_{DRIVE}$ | 1 µs |
| Deglitch time (OCP_DEG) | 2 µs |
| Supply voltage | 36 V |

Current limit threshold = $V_{DS}$ threshold / $R_{DS\_ON}$ = 32.7 A

This means once the current of 32.7 A reaches the $V_{DS}$ comparator in the gate driver trips and wait for a delay deglitch period set by OCP_DEG, before turning off the MOSFET, to ensure that the overcurrent trip is caused by actual overcurrent event and not by any noise signal. But the circuit current increases from 32.7 A to a higher value within the deglitch time. The increase in current is determined by OCP_DEG, short circuit resistance, inductance, and applied DC bus voltage.

For example, assuming:

- Short circuit inductance, $L_{SC}$ = 2 µH
- Driving voltage during short circuit = 36 V (VDC)
- Short circuit resistance, $R_{SC}$ = 0 Ω (for simplicity of analysis)

The increase in current in OCP_DEG can be calculated as in Equation 8.

$$\Delta I = \frac{V_{SC}}{L_{SC}} \times \Delta t = 36 \text{ A} \tag{8}$$

The inverter is shorted with a copper wire at the output of the three-phase inverter of this reference design. The expected peak current setting ≈ 32.7 + 36 = 68.7 A

Figure 42 shows the test setup to simulate a short circuit at the inverter output.

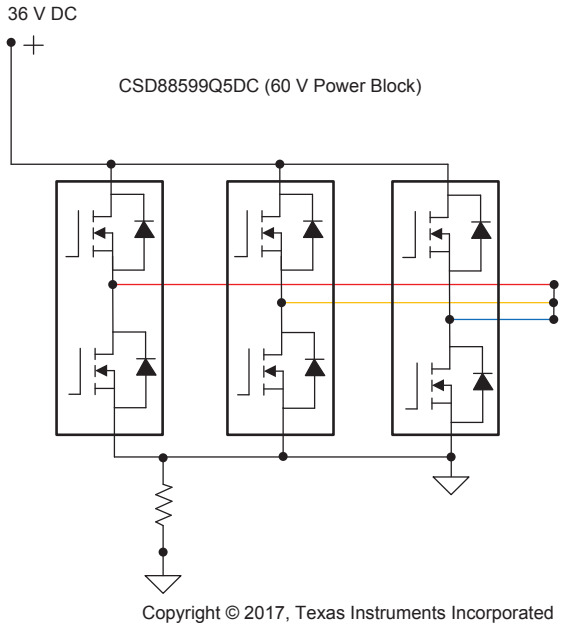




**Figure 42. Test Setup to Simulate Inverter Short Circuit**

Figure 43 shows the overcurrent protection acted at around 65 A. Once the current hits 65 A, the PWM shuts off immediately and the response time is less than 1 µs.

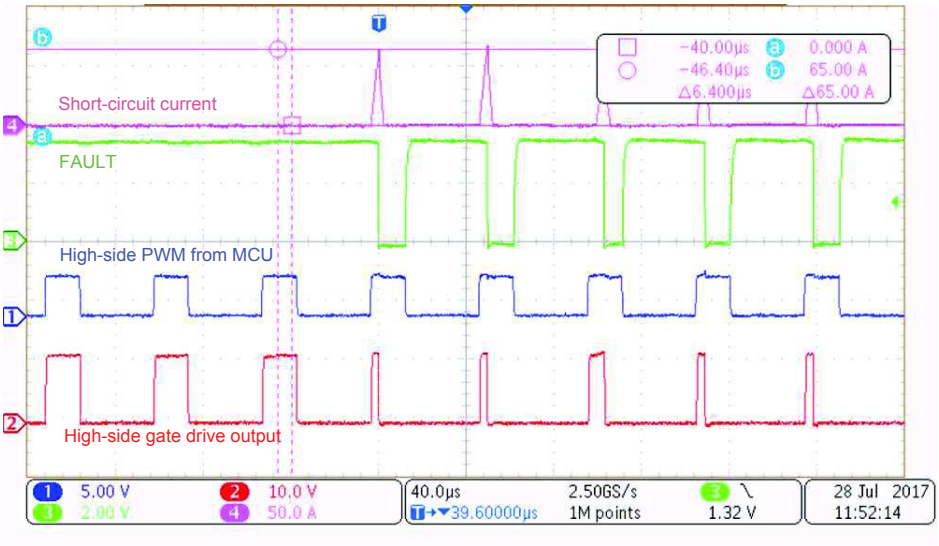


**Figure 43. Cycle-by-Cycle Overcurrent Protection With Inverter Output Shorted**

Figure 44 shows the test setup to simulate a stall current when the motor is rotating. SW is a single-throw, double-pole switch connect between the motor terminals. This switch is used to create a motor winding to a winding short.

Before SW is closed, the motor was rotating at a steady speed. Figure 45 shows the waveforms obtained when the switch SW is closed. When SW is closed, SW carries the short-circuit current. During this condition the motor stops, which causes the Hall state to continue at the current commutation state; therefore, the controller continues to generate the PWM corresponding to this commutation state. The overcurrent protection acted at around 70 A and the PWM shuts off immediately with response time less than 1 µs. Figure 45 shows the test results with motor stall condition.

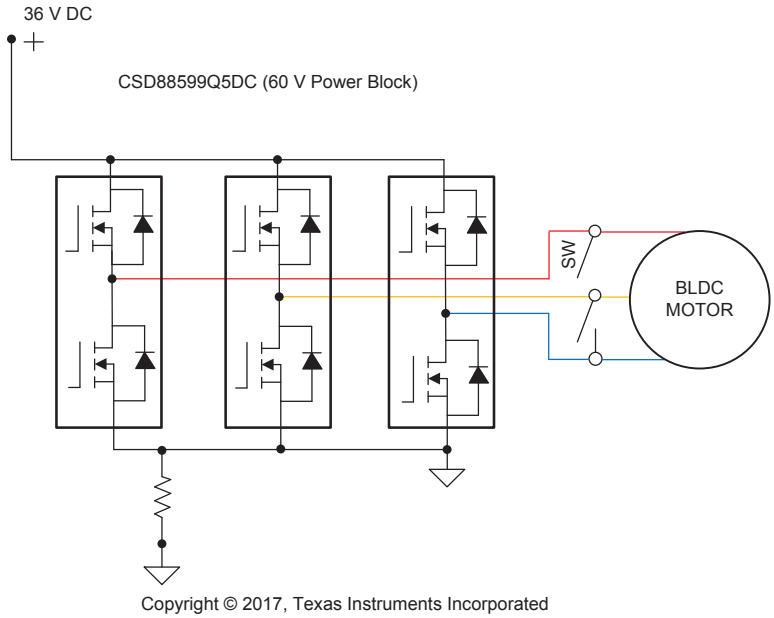




**Figure 44. Test Setup to Simulate Stall Current When Motor is Running**

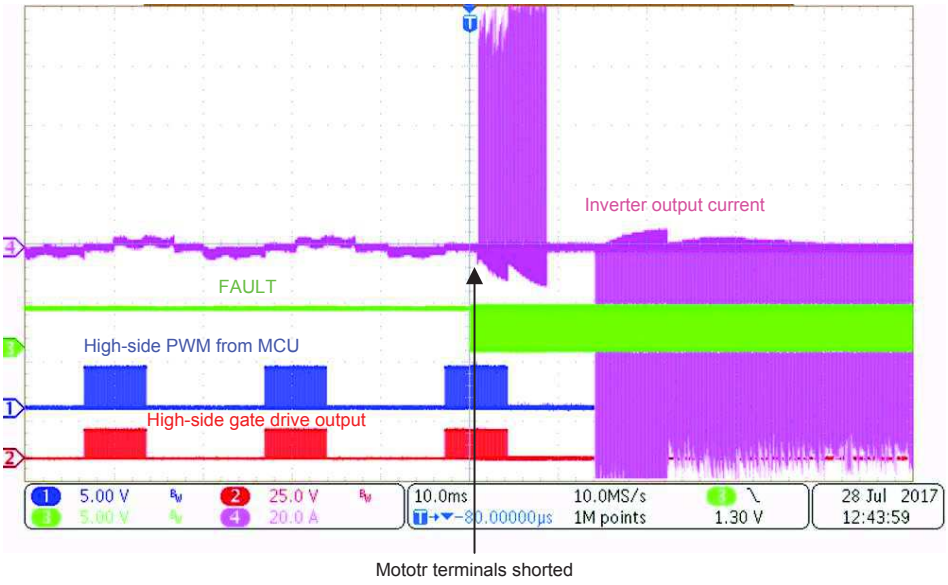


**Figure 45. Cycle-by-Cycle Overcurrent Protection With Motor Stall**

### 3.2.6.3 *Stall Current Latch Protection by DRV8323 $V_{DS}$ Monitoring*

The same test setup in Figure 44 is used for the stall current protection. Figure 46 shows the test results with latch protection by $V_{DS}$ sensing. When a $V_{DS}$ overcurrent event occurs, the device pulls all gate drive outputs low to put all six external MOSFETs into high-impedance mode. The fault is reported on the nFAULT pin with the specific MOSFET in which the overcurrent event detected is reported through the SPI status registers. Figure 47 shows a zoomed view of Figure 46. The response time from overcurrent detection to the turnoff of the gate drive output is less than 1 µs and the peak current observed is 72 A.

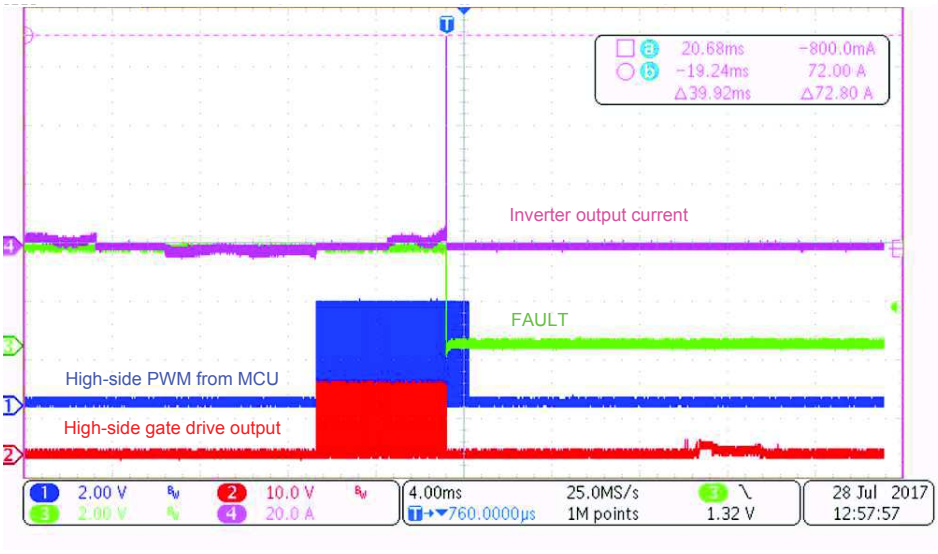


**Figure 46. Overcurrent Latch Protection With Motor Stall by $V_{DS}$ Monitoring**

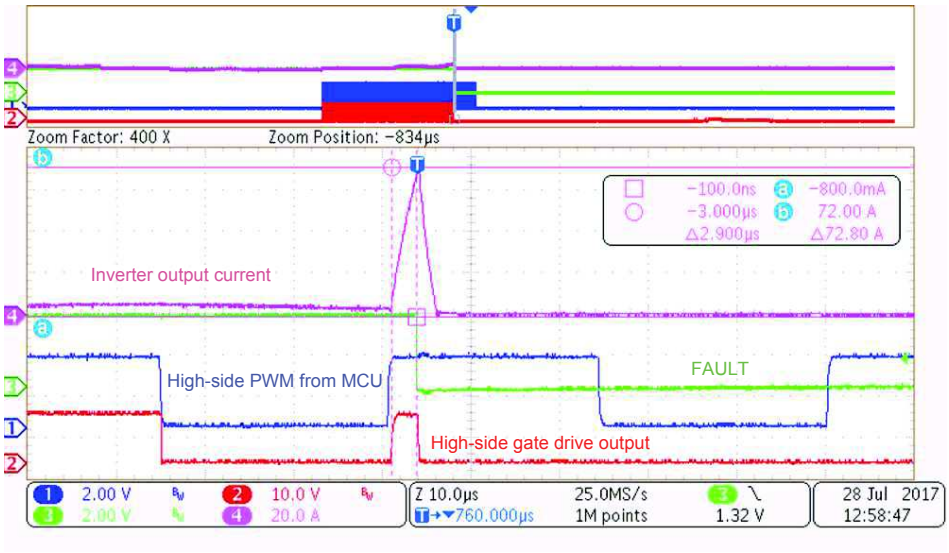


**Figure 47. Zoomed View of Overcurrent Latch Protection With Motor Stall by $V_{DS}$ Monitoring**

Figure 48 shows the test results of latch protection when the inverter output is shorted. The same test setup in Figure 42 is used for the short-circuit simulation. The latch protection acted at 65 A with $V_{DS}$ reference of 0.06 V.

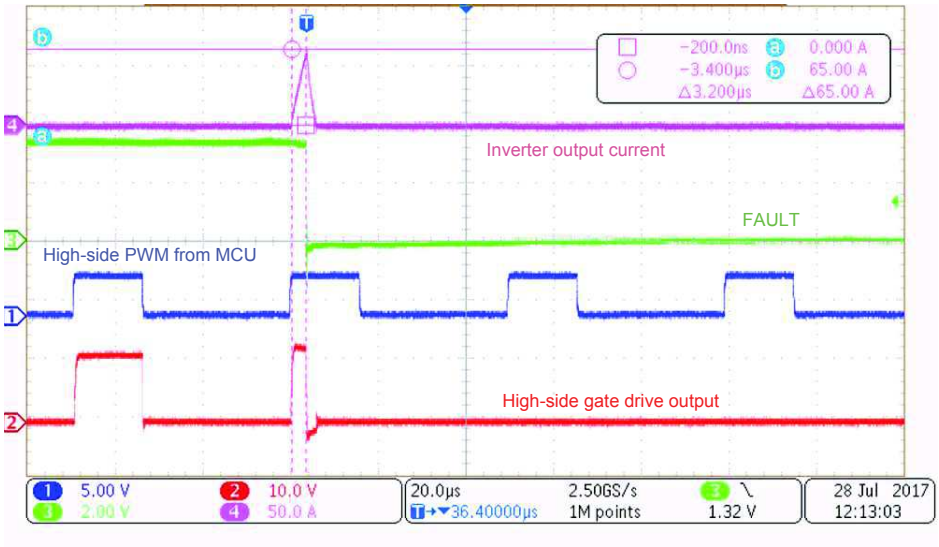


**Figure 48. Overcurrent Latch Protection With Inverter Output Shorted**

### 3.2.7 Testing for Peak Current Capability

Figure 49 shows the winding current of 60 A when the motor is stalled for 2 seconds. Figure 50 shows the thermal image of the board after 2 seconds.

Figure 51 shows the winding current of 100 A when the motor is stalled for 400 ms. Figure 52 shows the thermal image of the board after 400 ms.

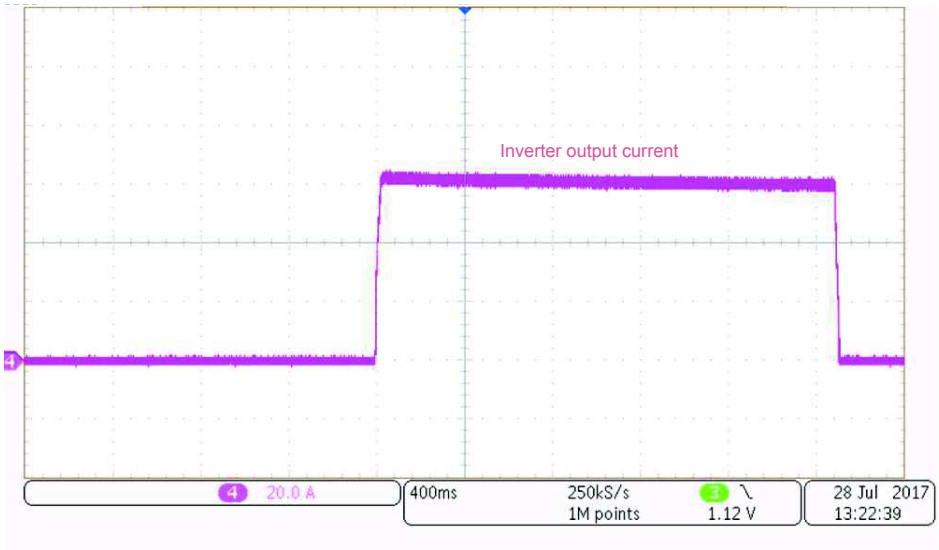


**Figure 49. Peak Current of 60-A Peak Current in Motor Winding During Motor Stall**

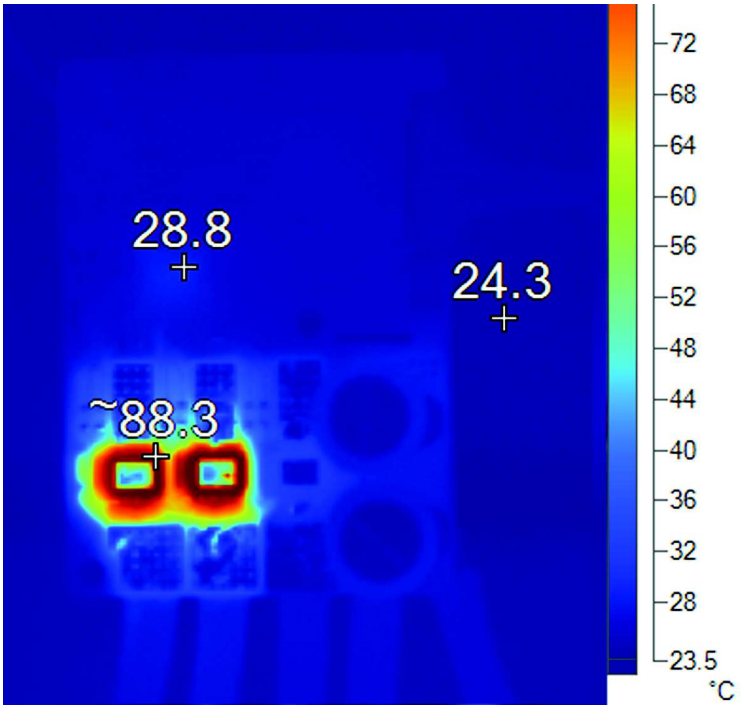


**Figure 50. Thermal Image of Board After 2 Seconds With 60-A Peak Current in Motor Winding**