NCP1399-150W--TEST REPORT

Implementing High Power Notebook Adapter Evaluation Board User's Manual

High Power Notebook Adapter with the NCP1399, NCP1602, NCP4305, NCP4354 and NCP4810

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EVAL BOARD USER'S MANUAL

Table 1. GENERAL PARAMETERS

Devices	Applications	Input Voltage	Output Power	Topology	Board Size
NCP1399 NCP1602 NCP4305 NCP4354 NCP4810	High Power NB Adapter	85 – 260 V_{AC}	150 W	CRM PFC & LLC	142 × 67.5 × 19.5 mm 13.16 W/inch^3
Output Voltage	**V_{OUT} Ripple**	**Efficiency**	**Operating Temperature**	**Cooling**	**Standby Power**
19.5 V/7.7 A (9 A Curr. Limit)	< 150 mV 3 to 7 A Load Steps	Above 91% @ I_{LOAD} > 2 A	0–50°C	Convection Open Frame	< 130 mW

Description

This evaluation board user's manual provides elementary information about a high efficiency, low no-load power consumption reference design that is targeting power laptop adapter or similar type of equipment that accepts 19.5 V_{DC} on the input.

The power supply implements PFC front stage to assure unity power factor and low THD, current mode LLC power stage to enhance transient response and secondary side synchronous rectification to maximize efficiency. This design focuses mainly on the NCP1399 current mode LLC controller description – please refer to NCP1602 and NCP4305 material to gain more information about these devices.

The NCP1399 is a current mode LLC controller which means that the operating frequency of an LLC converter is not controlled via voltage (or current) controlled oscillator but is directly derived from the resonant capacitor voltage signal and actual feedback level. This control technique brings several benefits compare to traditional voltage mode controllers like improved line and load transient response and inherent out of zero voltage switching protection. The LLC controller also features built-in high voltage startup and PFC operation control pins that ease implementation of a power supply with PFC front stage and no standby power supply on board.

The enhanced light lad operation of the LLC controller allows SMPS design to pass the latest no-load and light load consumption limits and still keeping output regulated with excellent transient response from no-load to full-load steps.

Key Features

- Wide Input Voltage Range
- Small Form Factor/High Power Density
- High Efficiency
- Low No-load Power Consumption
- Fast Startup
- X2 Capacitor Discharge Function
- Near Unity Power Factor
- Low Mains Operation Protection
- Overload Protection
- Secondary Short Circuit Protected
- Thermal Protection
- Regulated Output Under any Conditions
- Excellent Load and Line Transient Response
- Capability to Implement Off-mode for Extremely Low No-load Power Consumption

February, 2016 − Rev. 1
Publication Order Number:
EVBUM2341/D

Detail Demo-board Schematic Description

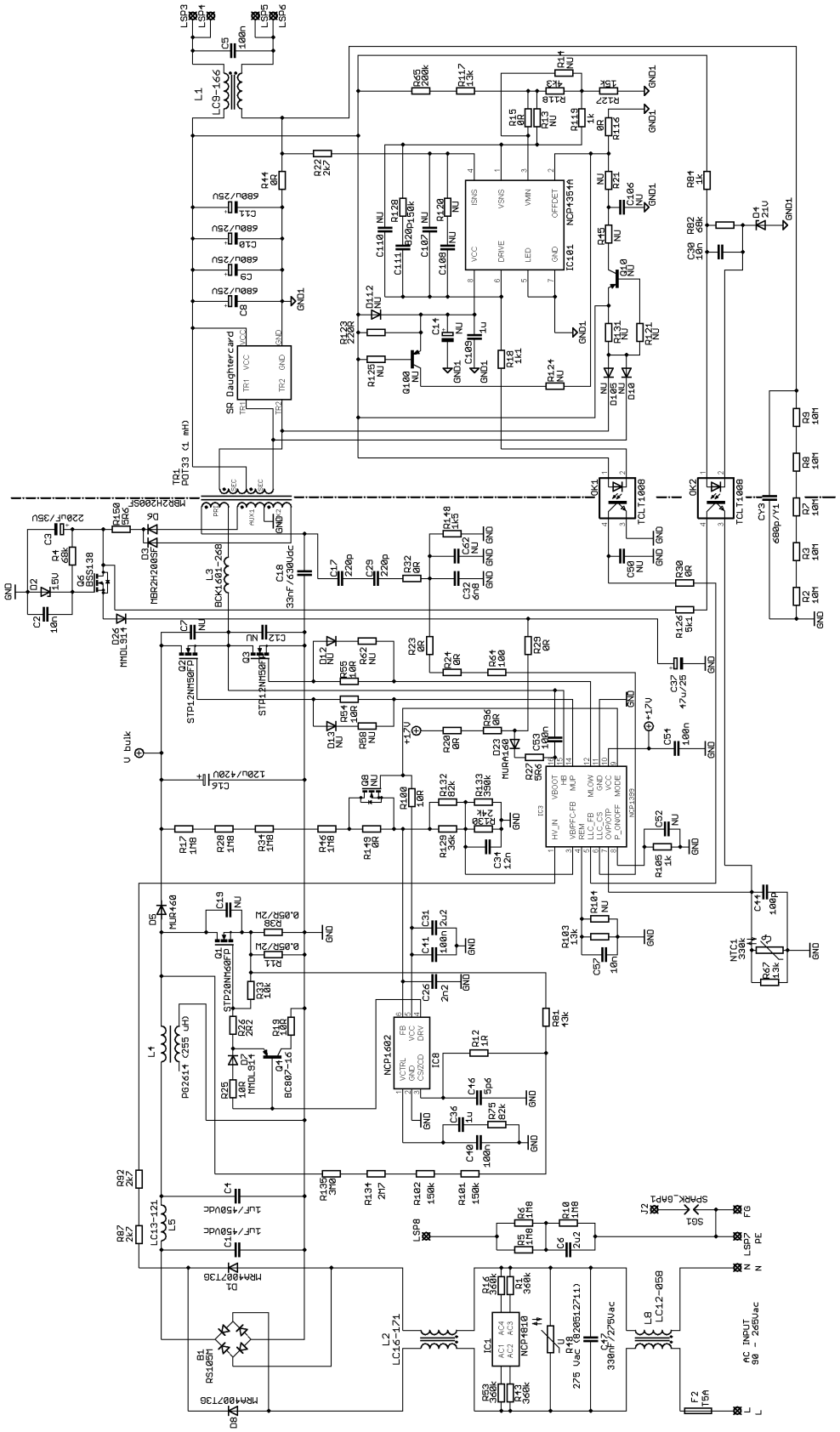

Figure 1. Laptop Adapter Demo-board − Main Board Schematic

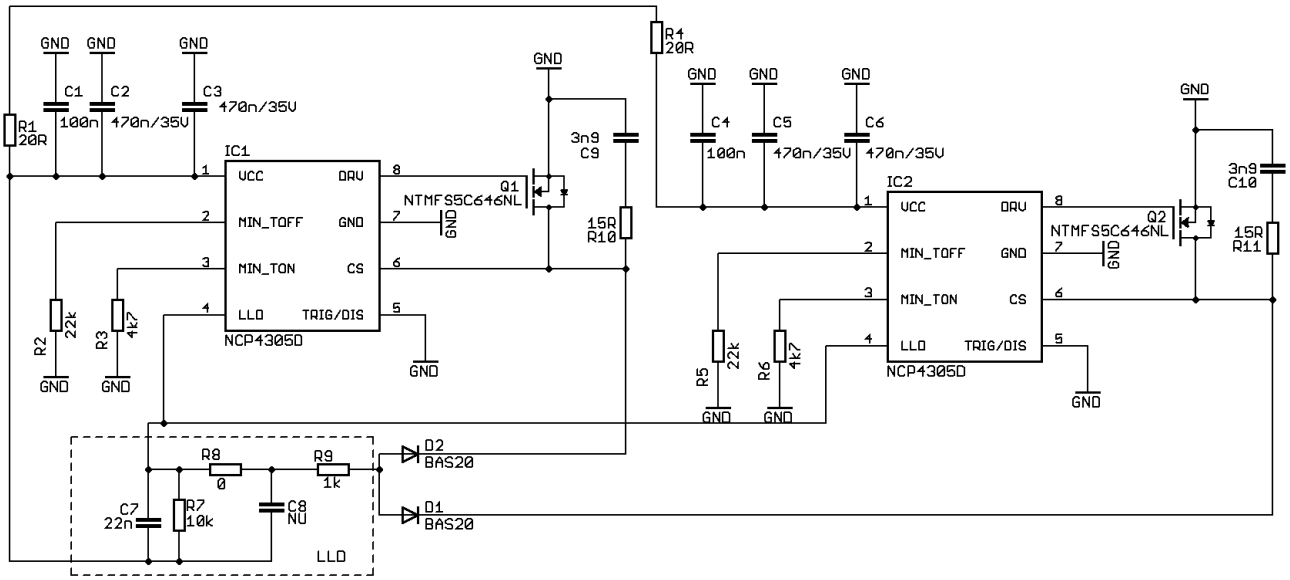

Figure 2. Laptop Adapter Demo-board − SR Daughtercard Schematic

The input EMI filter is formed by components L_8, L_2, L_5, C_{47}, C_1, C_4, C_6, R_5, R_6, R_{10} and R_{48}. The IC_1 (NCP4810) with safety resistors R_1, R_{16}, R_{43}, R_{53} is used to assure lose-less X2 capacitor discharge function after application is disconnected from the mains.

The PFC power stage uses standard boost PFC topology formed by power components B_1, L_1, D_5, Q_1, R_{11}, R_{38}, and bulk capacitor C_{16}. The PFC controller IC_8 (NCP1602) senses input voltage indirectly – via PFC power MOSFET drain voltage sensing network R_{135}, R_{134}, R_{102} and R_{101}. The PFC coil current is sensed by the shunt resistors R_{11} and R_{38}. The series resistor R_{81} defines maximum PFC front stage peak current. The PFC feedback divider is shared with LLC brown-out sensing network in order to reduce application no-load power consumption. The PFC FB/LLC BO divider is formed by resistors R_{17}, R_{28}, R_{34}, R_{46}, R_{129}, R_{130}, R_{132}, R_{133} and R_{149}. The FB signal is filtered by capacitor C_{26} to overcome possible troubles caused by the parasitic capacitive coupling between pin and other nodes that handle high dV/dt signals. The internal bulk voltage regulator compensation C_{40}, C_{36} and R_{75} is connected to the IC_8 pin 1. The PFC MOSFET is driven via circuitry R_{19}, R_{25}, R_{26}, R_{33}, D_7 and Q_4. This solution allows to select needed turn-on and turn-off process speed for Q_1 and also to handle gate discharge current in local loop – minimizing EMI caused by the driver loop.

The LLC power stage primary side composes from these devices: MOSFETs Q_2, Q_3, external resonant coil L_3, transformer TR_1 and resonant capacitor C_{18}. The IC_3 (NCP1399Ax) LLC controller senses primary current indirectly – via resonant capacitor voltage monitoring which is divided down by capacitive divider R_{32}, C_{17}, C_{29}, C_{32} and C_{62}. The capacitive divider has to provide minimum phase shift between resonant capacitor signal and divided signal on the LLC_CS pin. The capacitive divide has to be loaded in the same time to assure fast LLC_CS pin signal stabilization after application startup – this is achieved by resistor R_{148}. The series resistor R_{23}, R_{24}, and R_{64} is used to limit maximum current that can flow into the LLC_CS pin. The FB optoucoupler OK_1 is connected to the LLC_FB pin and defines converter output by pulling down this pin when lower output power is needed. Capacitor C_{50} forms high frequency pole in FB loop characteristics and helps to eliminate eventual noise that could be coupled to the FB pin by parasitic coupling paths. The Brow-Out resistor sensing network was already described in PFC section as it is shared with PFC feedback sensing. The Skip/REM pin of the NCP1399 is used for skip threshold adjustment in this demo-board option. Resistors R_{103} and R_{104} are used for this purpose together with noise filtering capacitor C_{57}. The over-voltage and over-temperature protections are implemented via OVP/OTP pin by using resistor R_{67}, temperature dependent resistor NTC1, filtering capacitor C_{44} and optocoupler OK_2. The OVP comparator is located on the secondary side to assure maximum OVP circuitry accuracy. The PFC ON/OFF function is not used in this revision of demo-board – i.e. the bulk voltage is regulated to nominal level during entire board operation (full, medium, light or no-load conditions) thus the P_ON/OFF pin is connected to ground via resistor R_{105}. The PFC_MODE pin provides bias to the PFC controller via series resistor R_{100} after high enough voltage is available on the LLC VCC capacitors C_{37}. The VCC decoupling capacitor C_{54} and also bootstrap capacitor for high side driver powering C_{53} are located as close to the LLC controller package as possible to minimize parasitic inductive coupling to other IC adjust components due to high driver current peaks that are present in the circuit during drivers rising and falling edges transitions. The bootstrap capacitor is charged via HV bootstrap diode D_{23} and series resistor R_{96} which limits

charging current and V_{boot} to HB power supply slope during initial C_{53} charging process. The gate driver currents are reducer by added series resistors R_{54}, R_{55} to optimize EMI signature of the application.

The primary controllers bias voltage limiter circuitry is used in order to restrict upper value of the primary V_{CC} voltage to approximately 13 V. The VCC limiter composes of these components: resistors R_4, R_{150}, capacitors C_2, C_3, diodes D_3, D_2, D_6, D_{26} and transistor Q_6.

The secondary side synchronous rectification is located on separated Daughter-card and uses IC_1 and IC_2 SR controllers – NCP4305D. The SR MOSFTEs for each SR channel are Q_1 and Q_2. RC snubber circuits C_9, R_1, C_{10} and R_{11}, are used to damp down the parasitic ringing and thus limit the maximum peak voltage on the SR MOSFETs. The SR controllers are supplied from converter output via resistors R_1 and R_4. These resistors form RC filter with decoupling capacitors C_1 to C_6. The minimum on-time – R_3, R_6 and minimum off-time – R_2, R_5 resistors define needed blanking periods that help to overcome SR controllers false triggering to ringing in the SR power stage. The light load detection circuit (LLD) is formed by resistors R_7, R_8, R_9 capacitor C_7, C_8, and diodes D_1, D_2. The SR controllers are disabled by LLD circuitry when application enters skip mode – this helps to reduce no-load power consumption of application. The trigger/disable function of NCP4305 is not used in this application thus the corresponding pins are grounded.

The output voltage of the converter is regulated by Secondary Side Sleep mode Controller NCP4354A − IC_{101}. The regulation optocoupler OK_1 is driven via resistor R_{18} which defines loop gain. The NCP4354 is biased via resistor R_{123} with decoupling capacitor C_{109}. The output voltage is adjusted by divider R_{65}, R_{117}, R_{118}, R_{127} and R_{119}. The feedback loop compensation network is formed partially by these components, resistor R_{128} and capacitor C_{111}. The output filtering capacitor bank composes from low ESR capacitors C_8 to C_{11}. Output filter L_1, C_5 is used to clean out output voltage from switching glitches.

The secondary side OVP sense circuitry is using zener diode D_4, resistors R_{82}, R_{84} and capacitor C_{30}. The OVP threshold is adjusted by selected type of zener diode.

There are several options prepared in the PCB layout so that customer can modify demo-board according to his target application needs. Mentioned options for instance allow implementation of off-mode control from secondary side to further reduce no-load power consumption or different PFC front stage controller implementation.

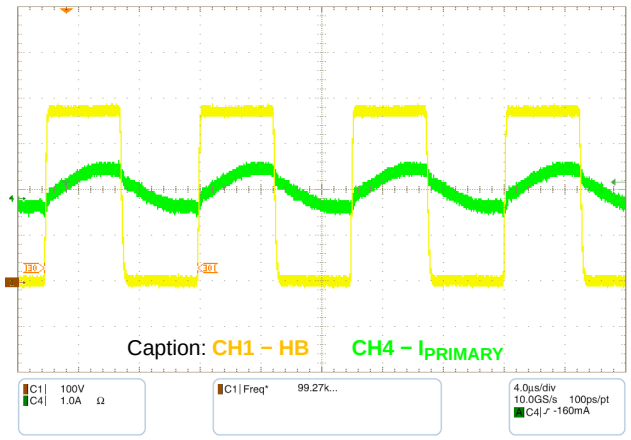

Figure 13. Steady Stage – I_{LOAD} = 2 A

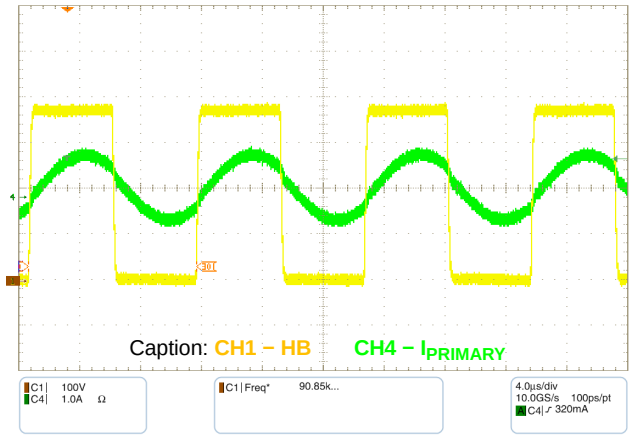

Figure 14. Steady Stage – I_{LOAD} = 4 A

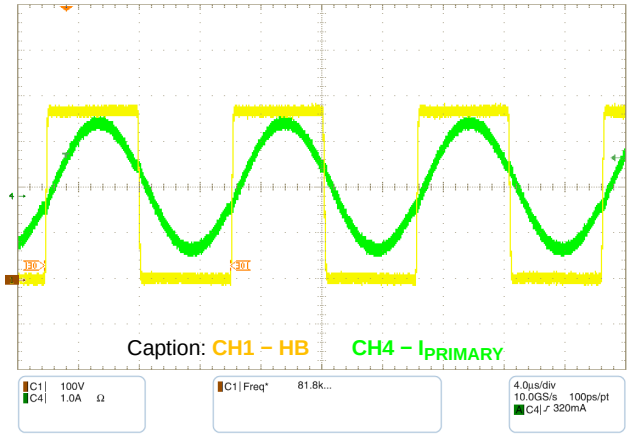

Figure 15. Steady Stage – I_{LOAD} = 8 A

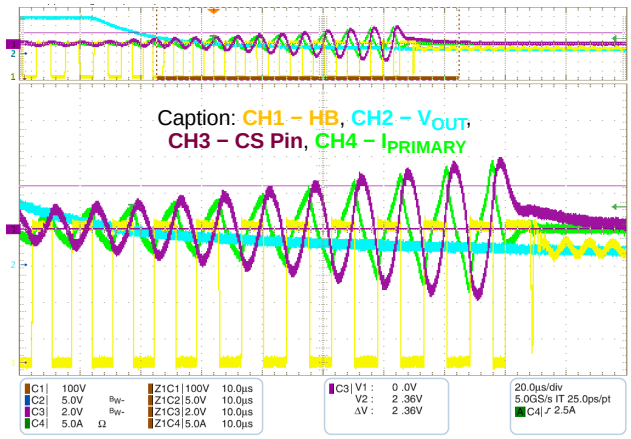

Figure 16. Secondary Short Transition

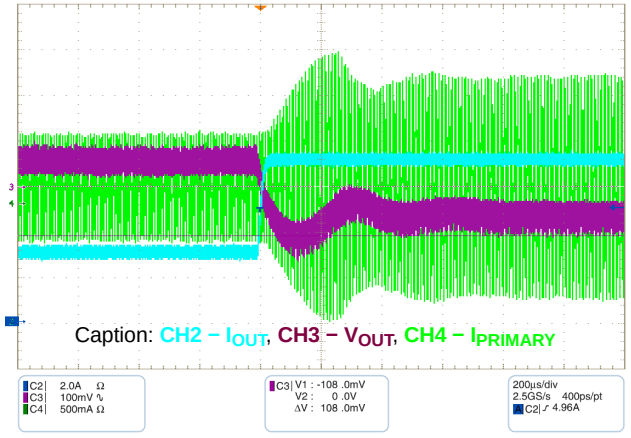

Figure 17. Transition Response − Load Step from 3 to 7 A

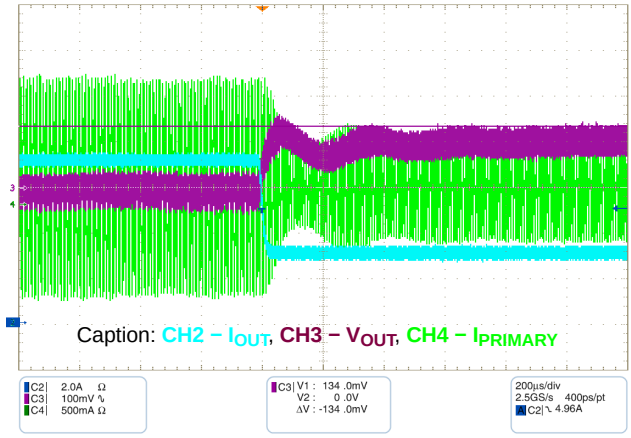

Figure 18. Transition Response − Load Step from 7 to 3 A

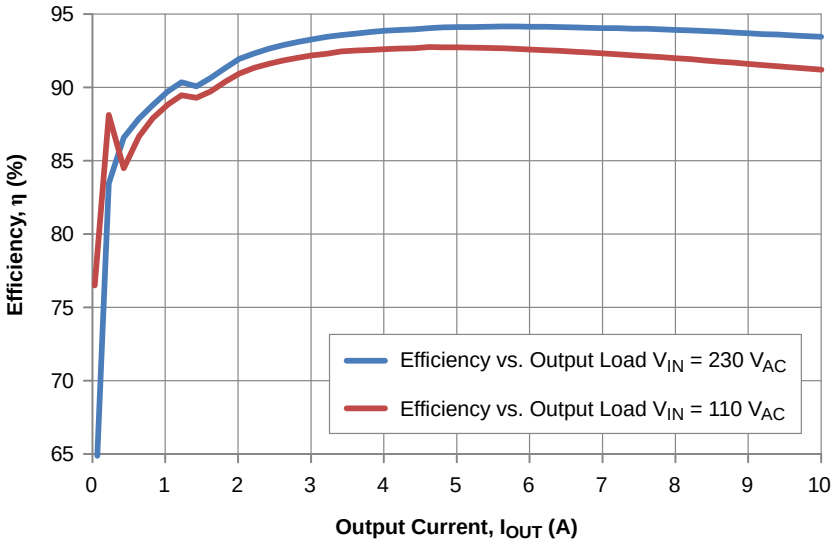

Figure 19. Board Efficiency – Including PFC Stage

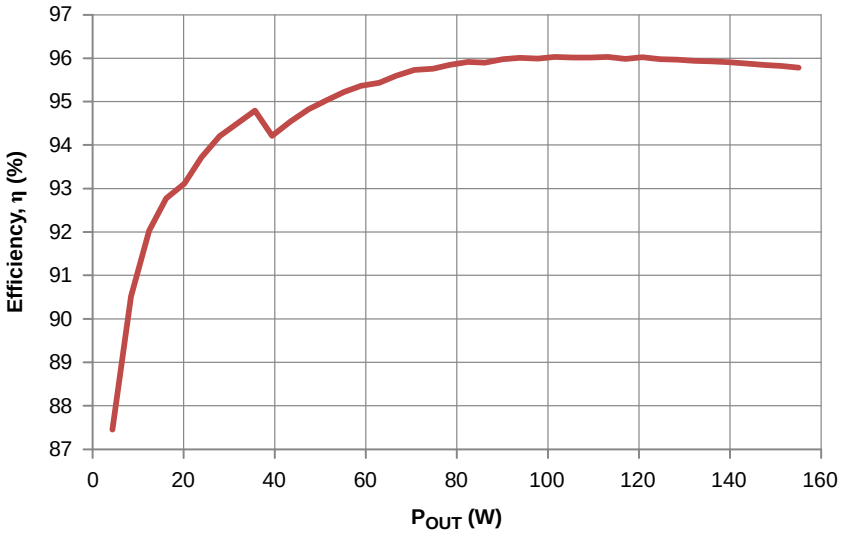

Figure 20. Board Power Stage with SR Efficiency V_{IN} = 385 V_{DC}

Table 2. NO-LOAD INPUT POWER CONSUMPTION

Input Voltage	Power Consumption
110 V_{AC}	114 mW
230 V_{AC}	123 mW