3.2 Testing and Results

3.2.1 Test Setup

Figure 15 shows the load setup used to test the motor. The load is an electrodynamometer-type load by which the load torque applied to the motor can be controlled.

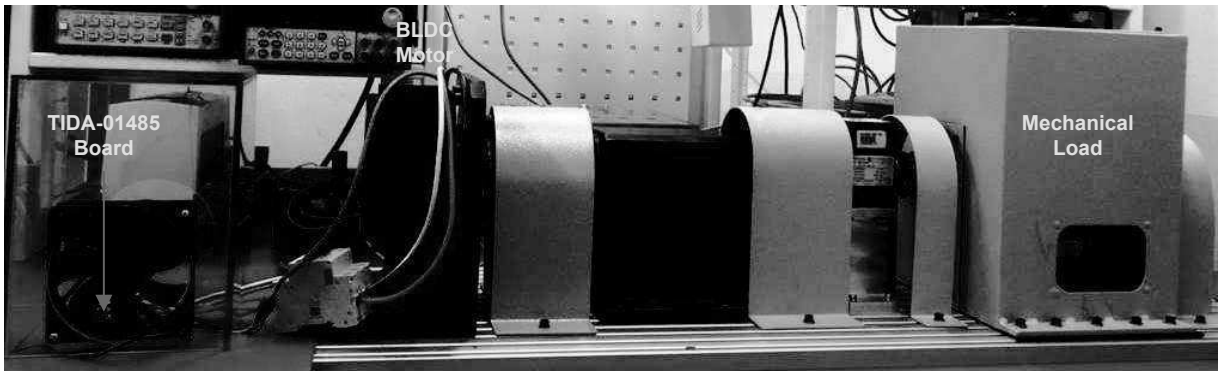

Figure 15. Board and Motor Test Setup

3.2.2 Functional Tests

3.2.2.1 3.3-V Power Supply Generated by Step-Down Converter

Figure 16 shows the 3.3 V generated from the step-down converter and the ripple in the 3.3-V rail.

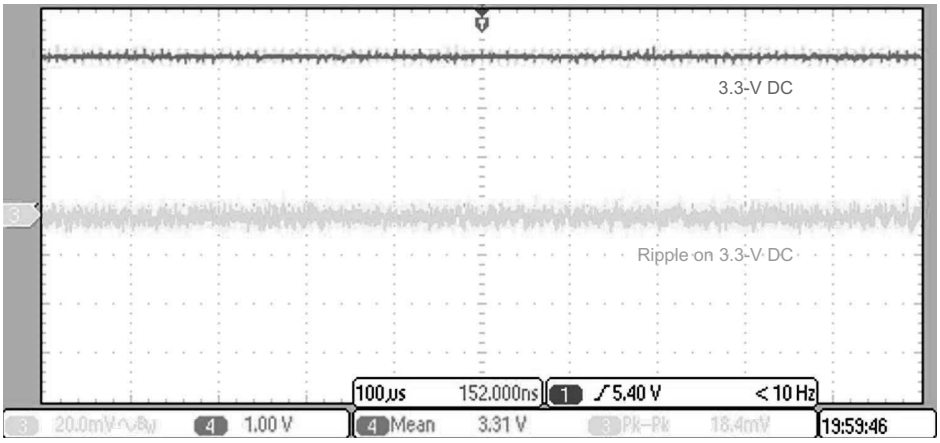

Figure 16. Output Voltage of 3.3 V From Step-Down Converter and 3.3-V Voltage Ripple

3.2.2.2 Microcontroller PWM and Gate Driver Output

Figure 17 shows the PWM scheme used in the board for trapezoidal control of the BLDC motor. The controls is a six-step block commutation where PWM is applied to top switch and bottom switch is operated in active freewheeling.

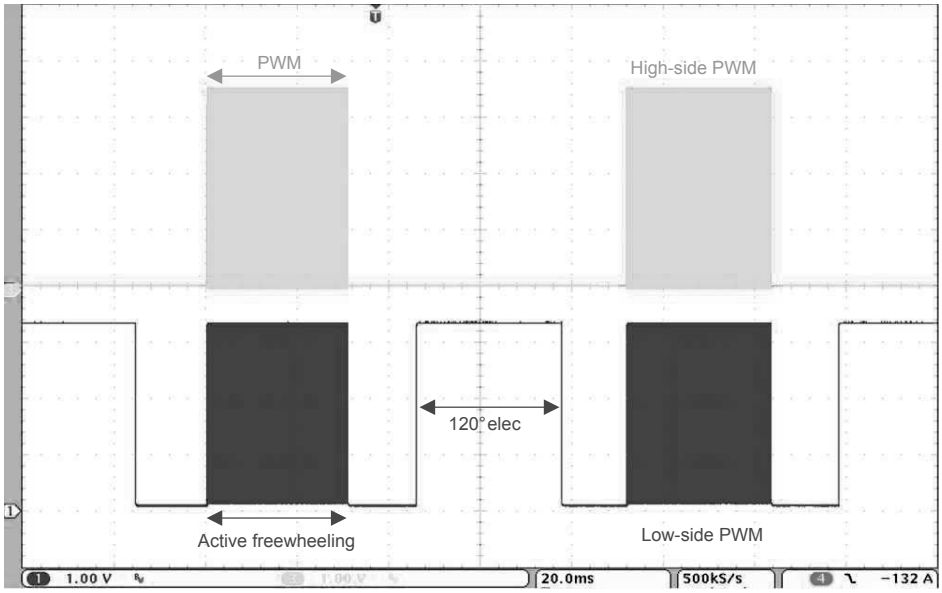

Figure 17. Low- and High-Side FET PWM Generated by MCU for Trapezoidal Control

Figure 18 shows the gate drive output voltage of the DRV8323 and the corresponding MCU PWM signals at a DC bus voltage of 36-V DC. The gate drive voltage is approximately 11 V, which means effective gate driving of standard MOSFETs. Figure 19 shows the gate drive voltage of the DRV8323 at a DC bus voltage of 8 V. The gate drive output voltage is approximately 6.5 V.

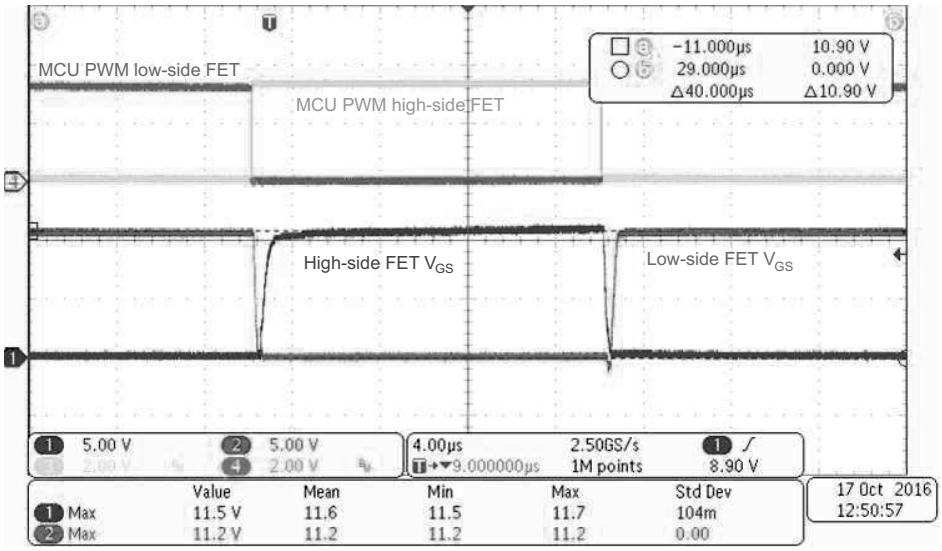

Figure 18. Low- and High-Side Gate Drive Voltage at 36-V DC

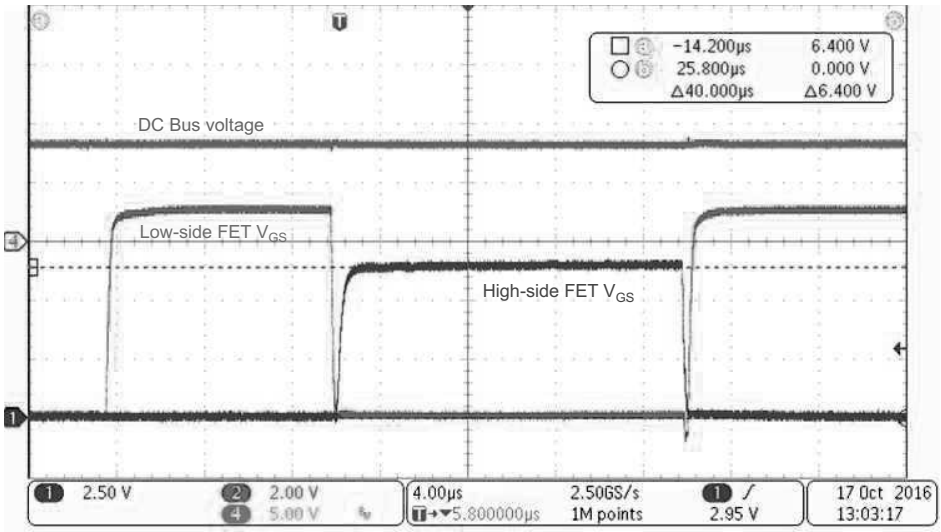

Figure 19. High- and Low-Side Gate Drive Voltage at 8-V DC

3.2.2.3 Dead Time From DRV8323

Figure 20 and Figure 21 shows the high-side and low-side gate source voltage from the DRV8323, which shows the dead time inserted by the DRV8323 at the both the edges of the PWM. The dead is programmed to 100 ns. The DRV8323 inserts the dead time after the V_{GS} handshake.

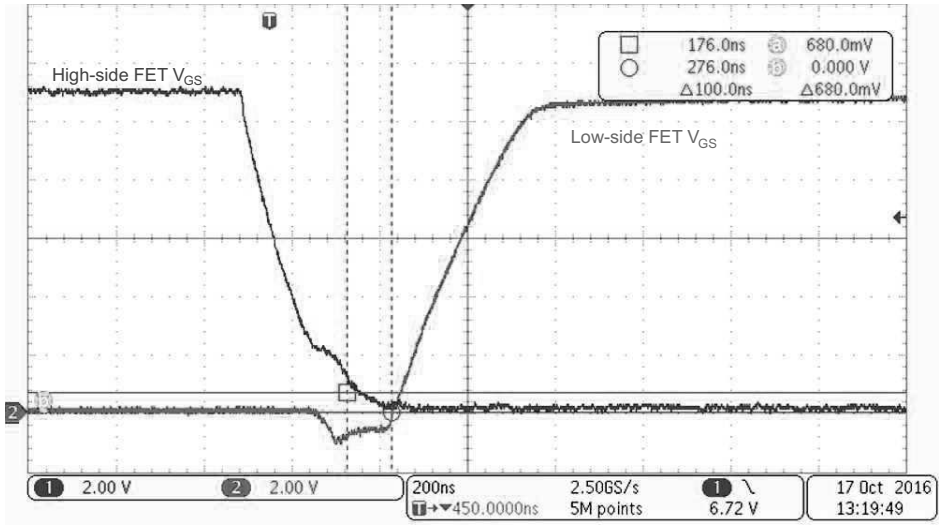

Figure 20. Dead Time at Rising Edge of Low-Side V_{GS}

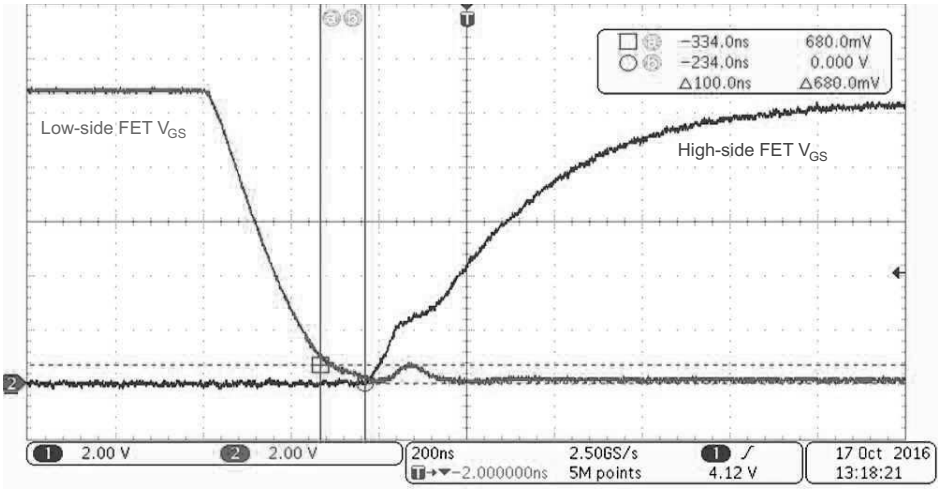

Figure 21. Dead Time at Trailing Edge of Low-Side V_{GS}

3.2.2.4 MOSFET Switching Waveforms

Figure 22 to Figure 25 show the V_{DS} and V_{GS} waveforms of the low-side and high-side MOSFETs at a gate current of the DRV8323 (IDRIVE) is set at a 120-mA source (the low gate charge of the CSD88599 allows low source current) and a 2-A sink current. Switching waveforms are clean without much overvoltage ringing due to the following:

- The power block has both the high-side and low-side switches in same package, which reduces the parasitic inductance and hence reduces the phase node voltage ringing.
- The current controlled gate driver with slew rate control helps to optimize the switching.
- The IDRIVE and TDRIVE features of the gate driver helps to shape the gate current to optimize the switching.

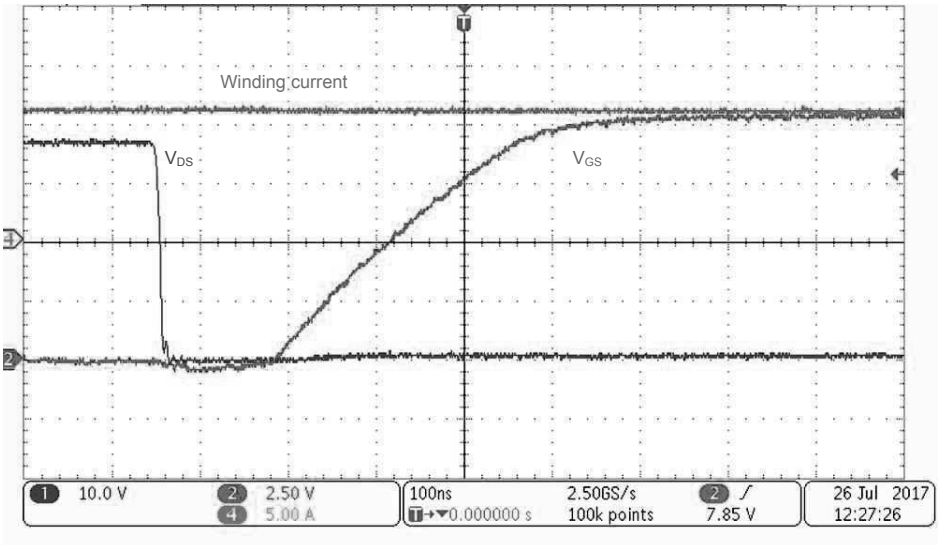

Figure 22. Turnon: Low-Side V_{GS} and V_{DS} at 12-A Winding Current

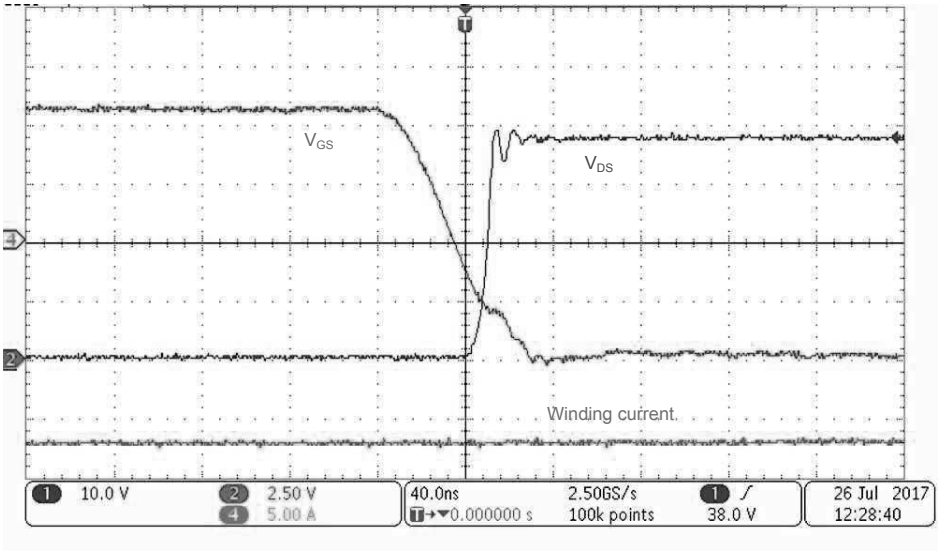

Figure 23. Turnoff: Low-Side V_{GS} and V_{DS} at 18-A Winding Current

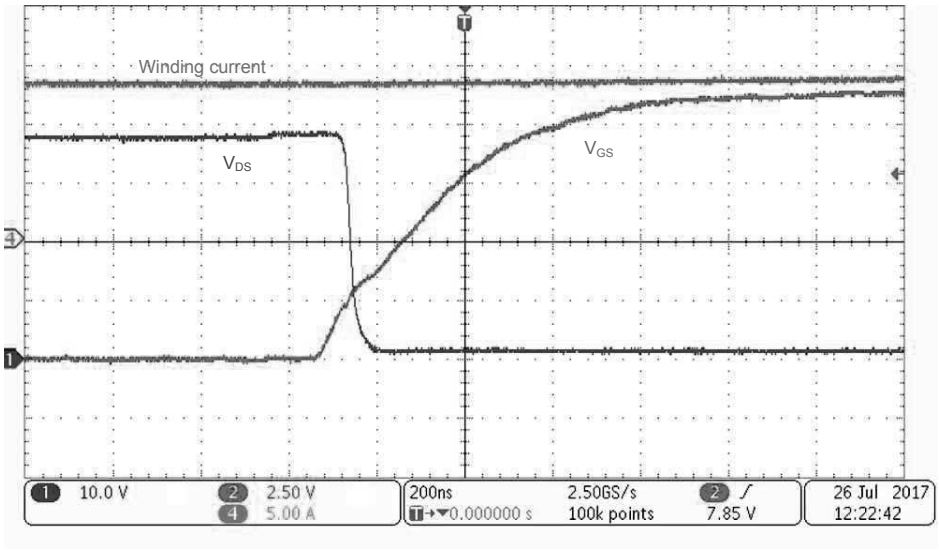

Figure 24. Turnon: High-Side V_{GS} and V_{DS} at 14-A Winding Current

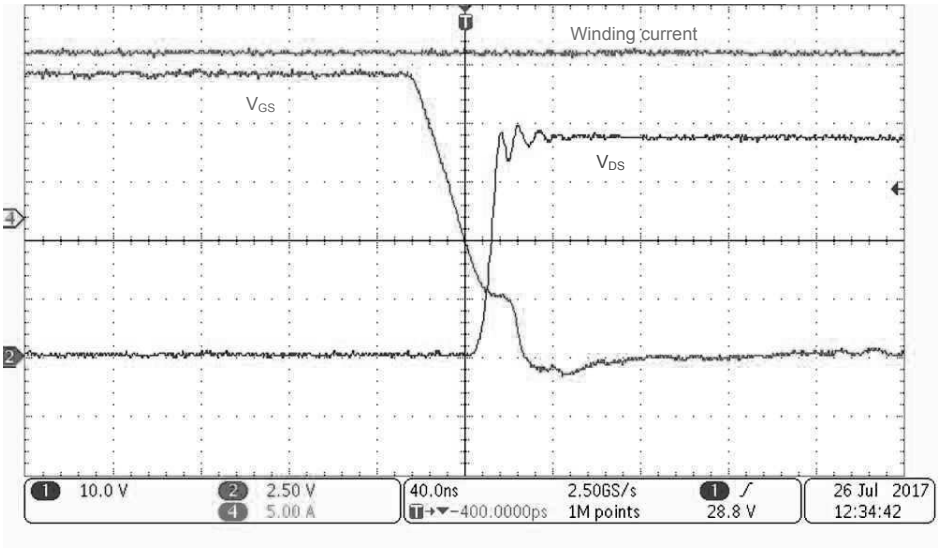

Figure 25. Turnoff: High-Side V_{GS} and V_{DS} at 16 A Winding Current

3.2.3 Load Test

The reference design board is tested with an external BLDC motor and load using the test setup in Figure 15. The testing is done with and without heat sink at different airflow conditions and different duty cycles. The key results are summarized in Section 3.2.3.1 through Section 3.2.3.3.

3.2.3.1 Load Test Without Heat Sink

Figure 26 shows the motor winding current and winding voltage waveforms at a 36-V DC input and a 17.4-A_{RMS} winding current. The result is listed in Table 5. The testing is done at 100% duty cycle. Figure 27 shows the steady state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 88°C.

Table 5. Load Test Results at 100% Duty Cycle Without Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	MAXIMUM FET TEMPERATURE
36	19.4	17.4	698	88°C

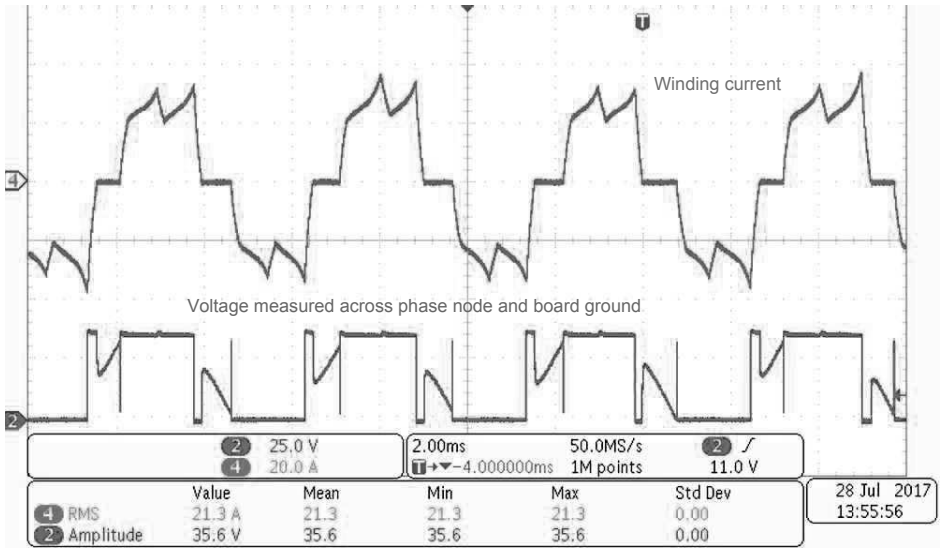

Figure 26. Load Test Results at 36-V DC Input, 17.4-A_{RMS} Winding Current, 100% Duty Cycle

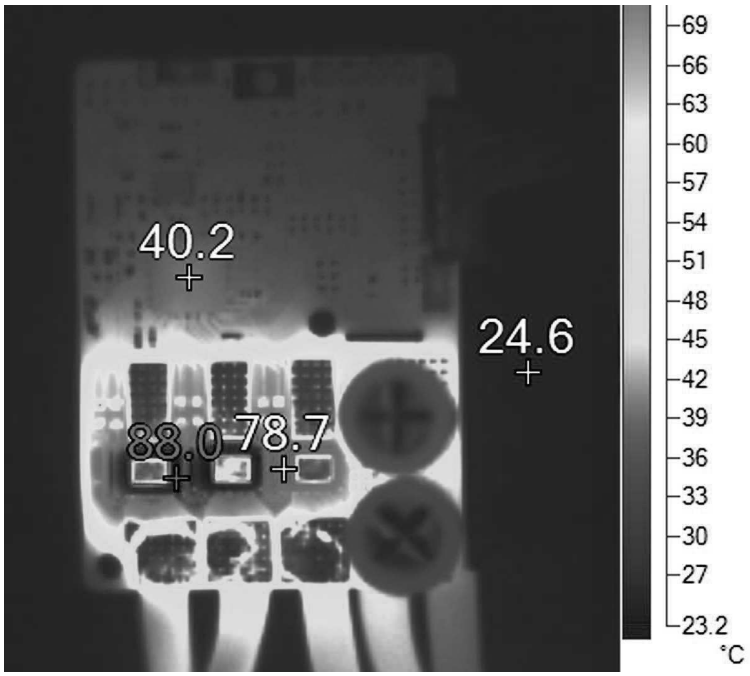

Figure 27. Thermal Image at 36-V DC Input, 17.4-A_{RMS} Winding Current, 100% Duty Cycle

Figure 28 shows the motor winding current and winding voltage waveforms at a 36-V DC input and a 18.6-A_{RMS} winding current at 95% duty cycle. The result is listed in Table 6. The testing is done at 95% duty cycle. Figure 29 shows the steady state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 102°C.

Table 6. Load Test Results at 95% Duty Cycle Without Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	MAXIMUM FET TEMPERATURE
36	19.3	18.6	695	102°C

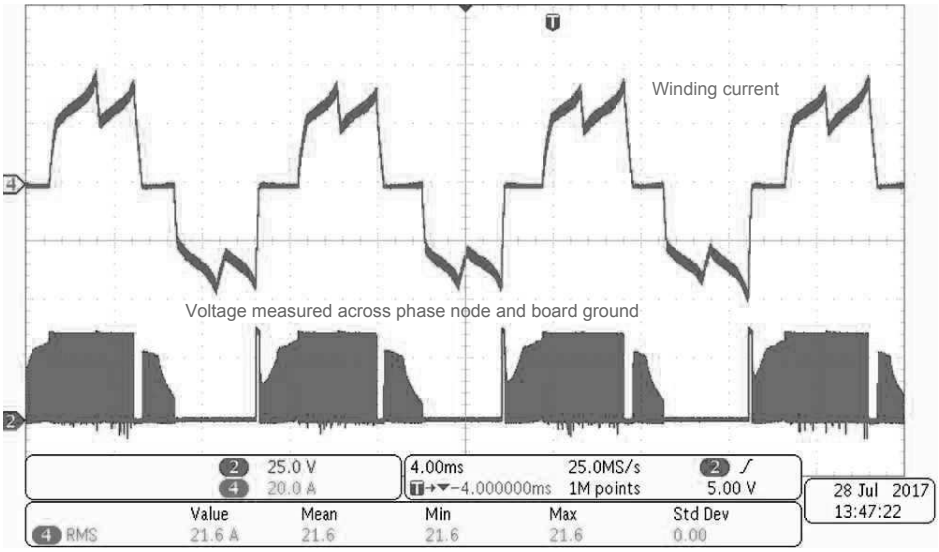

Figure 28. Load Test Results at 36-V DC Input, 18.6-A_{RMS} Winding Current, 95% Duty Cycle

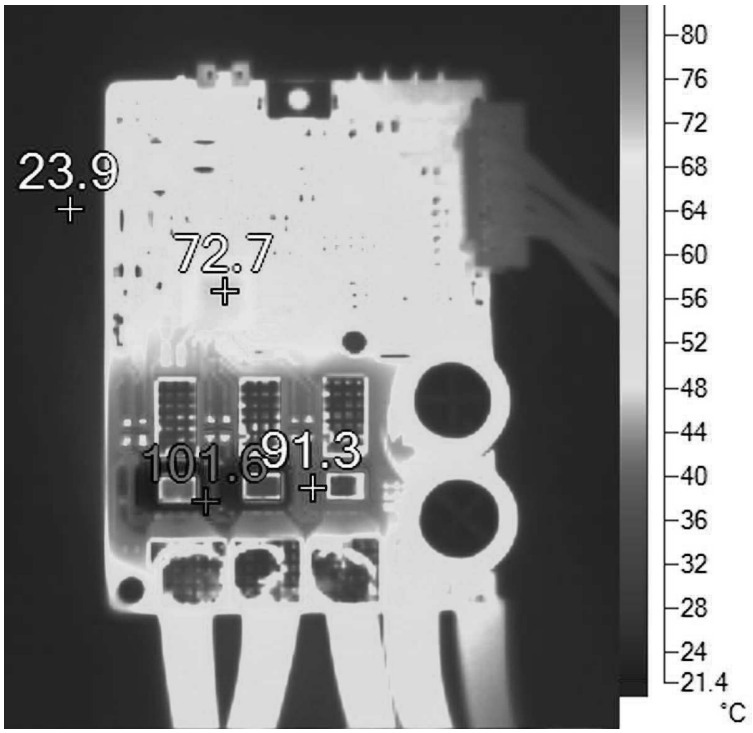

Figure 29. Thermal Image at 36-V DC Input, 18.6-A_{RMS} Winding Current, 95% Duty Cycle

3.2.3.2 Load Test With Heat Sink

Figure 30 shows a board image with the heat sink connected. The testing is done at a 95% duty cycle with the top-side heat sink connected. The result is listed in Table 7. Figure 31 shows the steady-state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 98°C.

Table 7. Load Test Results at 95% Duty Cycle With Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	MAXIMUM FET TEMPERATURE
36	26.2	25.3	943	98°C

Figure 30. Board Image With Heat Sink

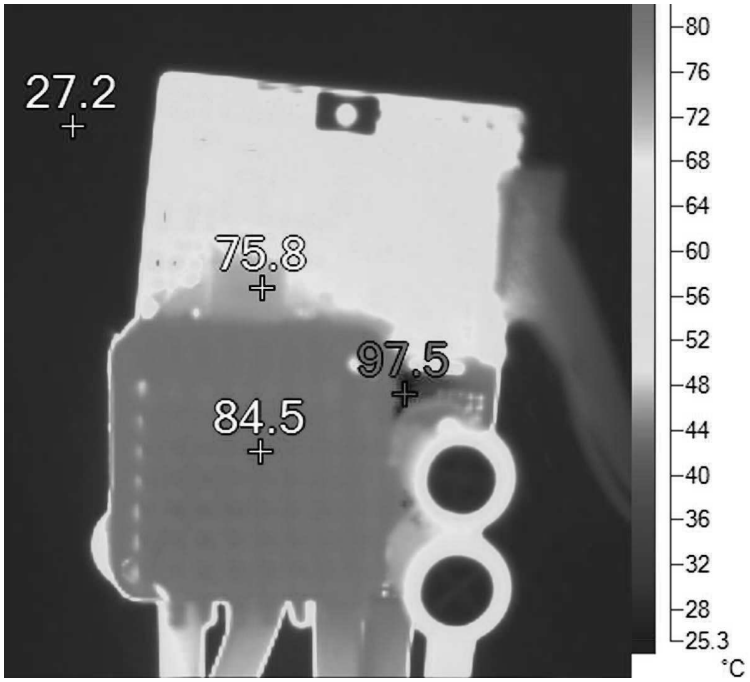

Figure 31. Thermal Image at 36-V DC Input, 25.3-A_{RMS} Winding Current, 95% Duty Cycle

3.2.3.3 Load Test at Different Airflow Conditions

The testing is done with and without the heat sink at different airflow conditions and different duty cycles. The key results are summarized in Table 8 and the effect of airflow at different test conditions are plotted in Figure 32 to Figure 35.

Table 8. Summary of Load Test Results at Different Conditions

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	MAXIMUM FET TEMPERATURE	DUTY CYCLE	AIRFLOW (LFM)	TEST CONDITION
TESTING WITHOUT HEAT SINK AT DUTY CYCLE = 1							
36	19.4	17.4	698.0	90.0°C	1	0	No heat sink
36	24.8	22.6	892.8	89.0°C	1	300	No heat sink
36	26.6	24.4	957.6	90.4°C	1	400	No heat sink
36	28.0	25.7	1008.0	93.0°C	1	500	No heat sink
TESTING WITHOUT HEAT SINK AT DUTY CYCLE = 0.95							
36	19.3	18.6	693.036	102°C	0.95	0	No heat sink
36	26.1	25.2	938.952	103°C	0.95	400	No heat sink
TESTING WITHOUT HEAT SINK AT DUTY CYCLE = 1							
36	30.1	27.1	1085	107°C	1	0	With heat sink
36	30.0	27.1	1080	84°C	1	100	With heat sink
TESTING WITH HEAT SINK AT DUTY CYCLE = 0.95							
36	26.2	25.3	942.678	99.0°C	0.95	0	With heat sink
36	28.5	27.5	1024.650	81.0°C	0.95	100	With heat sink
36	28.5	27.5	1024.650	70.2°C	0.95	200	With heat sink

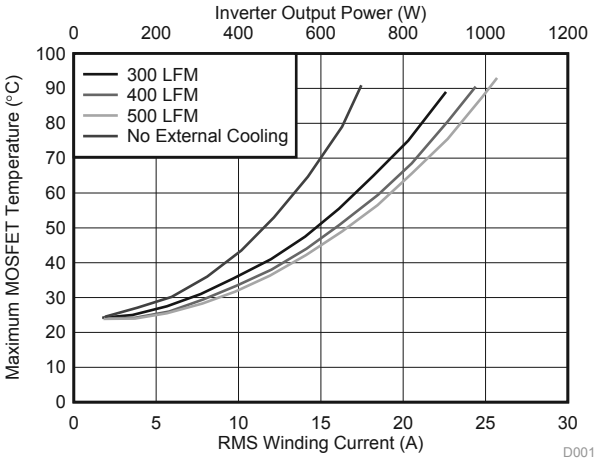

Figure 32. Load Test Results at 36-V DC Input, 100% Duty Cycle Without Heat Sink at Different Airflow

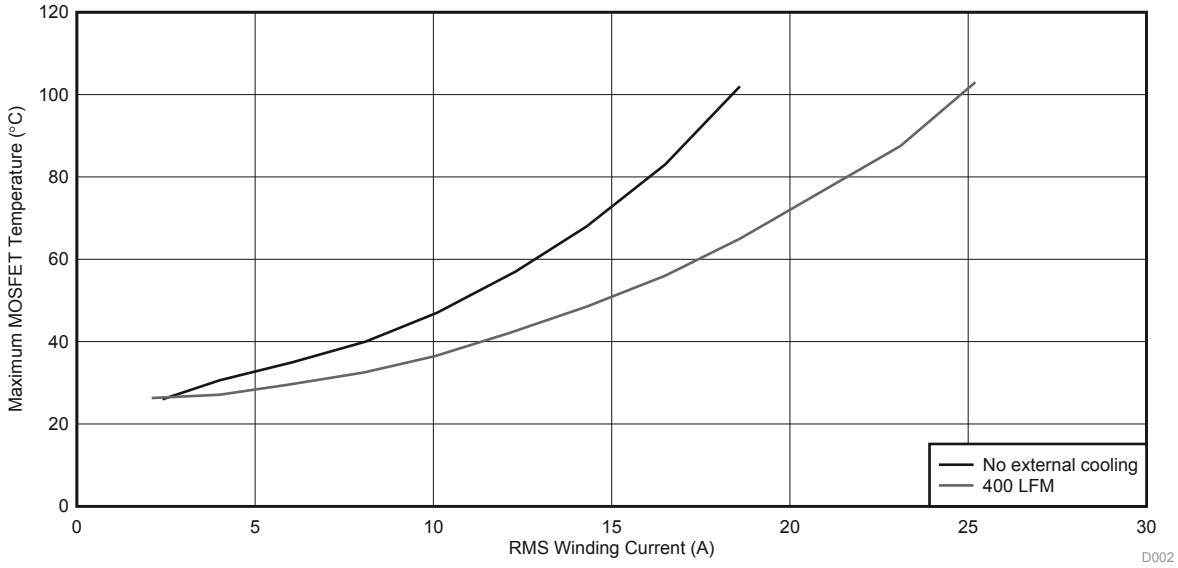

Figure 33. Load Test Results at 36-V DC Input, 95% Duty Cycle Without Heat Sink at Different Airflow

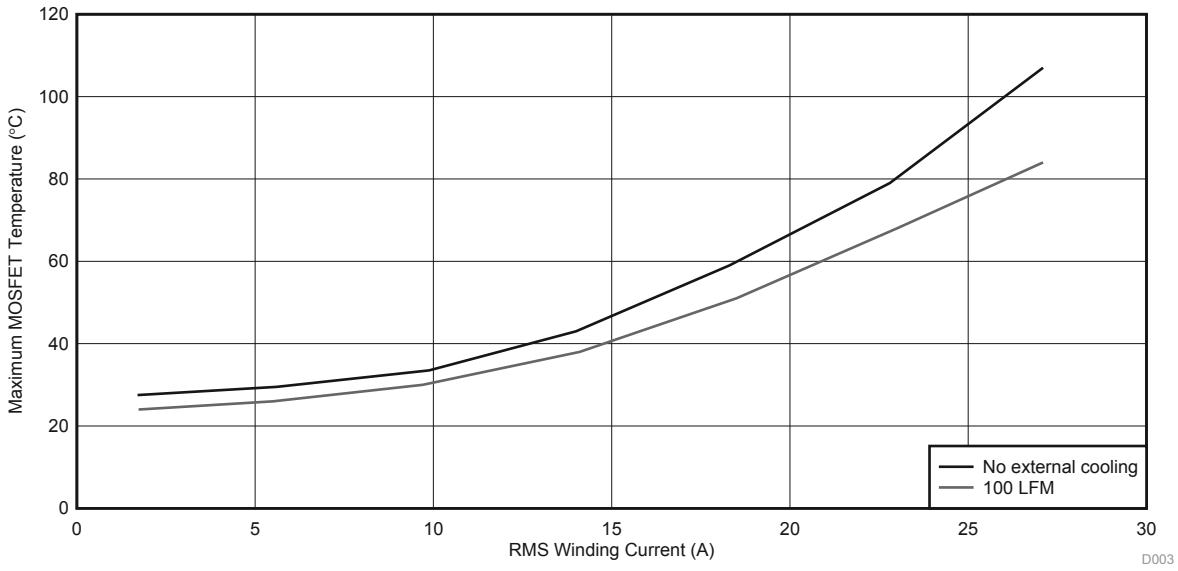

Figure 34. Load Test Results at 36-V DC Input, 100% Duty Cycle With Heat Sink at Different Airflow

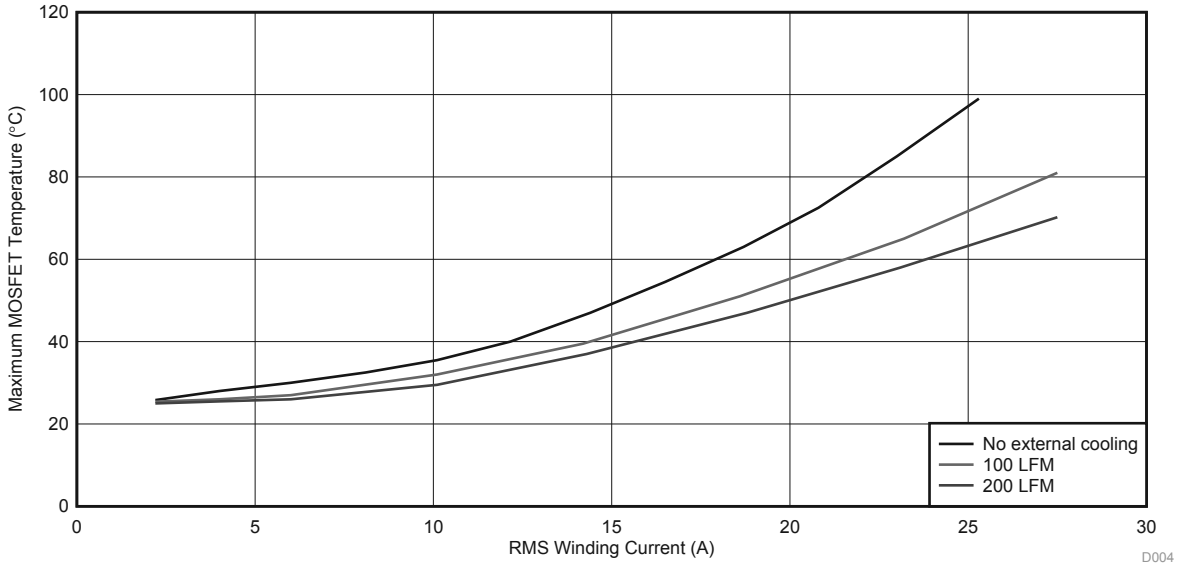

Figure 35. Load Test Results at 36-V DC Input, 95% Duty Cycle With Heat Sink at Different Airflow

3.2.4 Inverter Efficiency

The inverter efficiency is experimentally tested with a load setup as shown in Figure 15. The test results without a heat sink and at a 100% duty cycle are listed in Table 9. The test results without a heat sink and at a 95% duty cycle are listed in Table 10.

Table 9. Inverter Efficiency Test Results at 100% Duty Cycle Without Heat Sink and Without Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY	INVERTER LOSS (W)
36.11	2.53	2.12	91.44	90.99	99.51%	0.45
35.95	7.10	5.99	255.32	254.46	99.66%	0.86
35.91	11.77	10.13	422.76	420.81	99.54%	1.95
35.92	16.34	14.31	586.91	582.81	99.30%	4.10
35.81	20.83	18.57	745.80	739.10	99.10%	6.70
35.75	25.33	22.87	905.51	895.15	98.86%	10.36

Table 10. Inverter Efficiency Test Results at 95% Duty Cycle Without Heat Sink and Without Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY	INVERTER LOSS (W)
36.06	2.21	1.93	79.72	79.03	99.14%	0.69
35.90	6.65	5.85	238.76	237.51	99.48%	1.25
35.84	11.12	10.04	398.66	396.08	99.35%	2.58
35.97	15.48	14.25	556.81	551.60	99.06%	5.21
35.99	19.76	18.53	711.37	702.68	98.78%	8.69
36.02	24.00	22.86	864.37	851.69	98.53%	12.68

The test results without a heat sink but with a 300LFM airflow and at a 100% duty cycle are listed in Table 11. The test results without a heat sink but with a 300LFM airflow and at a 95% duty cycle are listed in Table 12.

Table 11. Inverter Efficiency Test Results at 100% Duty Cycle Without Heat Sink and at 300LFM Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY	INVERTER LOSS (W)
36.19	2.35	1.95	85.12	84.69	99.49%	0.43
35.75	7.02	5.89	251.02	250.26	99.70%	0.76
35.95	11.85	10.08	426.11	424.50	99.62%	1.61
35.96	16.62	14.30	597.50	594.17	99.44%	3.33
36.00	21.35	18.56	768.51	763.08	99.29%	5.43
35.88	26.06	22.91	935.30	927.18	99.13%	8.12
35.88	28.45	25.40	1020.54	1010.78	99.04%	9.76

Table 12. Inverter Efficiency Test Results at 95% Duty Cycle Without Heat Sink and at 300LFM Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY	INVERTER LOSS (W)
36.16	2.07	1.81	74.77	74.10	99.11%	0.67
36.04	6.59	5.80	237.45	236.29	99.51%	1.16
36.02	11.08	10.02	399.27	397.02	99.43%	2.26
36.00	15.46	14.26	556.34	552.22	99.26%	4.12
35.94	19.73	18.57	708.96	702.00	99.02%	6.96
35.90	24.07	22.89	864.20	853.33	98.74%	10.87
35.98	26.13	25.13	940.30	927.55	98.64%	12.74

The efficiency curve of these test conditions are plotted in Figure 36.

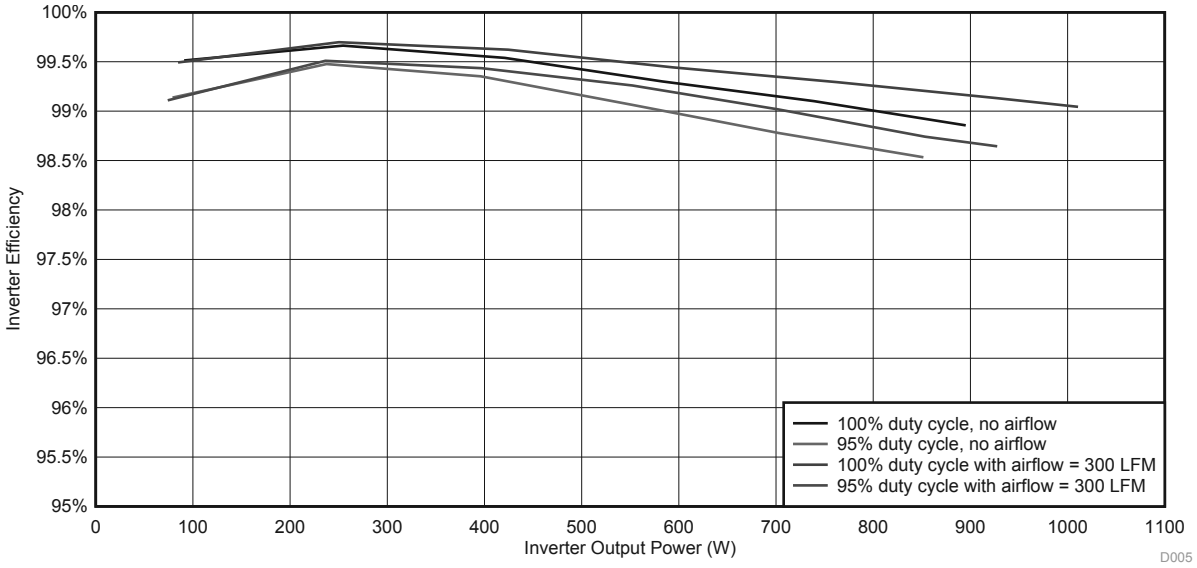

Figure 36. Inverter Efficiency versus Output Power

The reference design could achieve the high efficiency due to the following key factors:

- Low R_{DS_ON} of the MOSFET power block reducing the conduction losses
- Clean FET switching reducing the switching losses and diode losses
- Power block allows small PCB form factor and hence enable low PCB track resistance leads to