XDPL8220 PFC+Flyback Dual-Stage Multi-Mode Controller
50W Reference Design with CDM10V Isolated Dimming Interface

XDP™ digital power

About this document

Scope and purpose

This document contains the specification, schematic, bill of materials and measurement results of the 50W LED driver for LED lighting using the Infineon XDPL8220 dual-stage multi-mode flyback + PFC combo controller. It also includes fine-tuning guide and frequently asked questions to ease the process of designing a customized LED driver based on own project requirement.

Intended audience

This document is intended for anyone wishing to design high-performance dual-stage digital flyback AC-DC converters for LED lighting based on the PFC+Flyback combo controller XDPL8220.

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Revision 1.1
2016-11-28

1 Introduction

XDPL8220 50 W reference design is a digitally configurable LED driver which has universal input of 90-305 V_{AC}, wide output load range of 16-48 V_{DC} and isolated dimming interface (with CDM10V). Please refer next page for the main design features of this board based on XDPL8220 and CDM10V.

Note: The 50W reference design is ready for evaluation without the need of any pre-programming by the user as the XDPL8220 chip on PCB has already been burned with the default full set of working parameters configuration. Please connect the AC Input, LED output and dimming input as shown in ***Figure 1****, for the test setup.*

Attention: If a low DC source with voltage output 0~10V is used for the dimming function evaluation at the dimming interface, please witch on DC output first before the XDPL8220 50W reference board operates (LED engine does not light) or the dimming IC CDM10V (IC201) could be damaged. (The input of the CDM10V should not be higher than the Vcc supply voltage.)

Figure 1 XDPL8220 50W reference design with isolated dimming interface and configuration connector

2 Design Features

- Dual-stage flyback with power factor correction (PFC) and high-precision primary side-controlled constant voltage (CV), constant current (CC) and limited power (LP) output.
- Excellent current accuracy of typical +/-2% across universal input voltage range (90 to 305Vac) and wide output voltage range (from 16 V – 48 V)
- Integrated 600 V HV cell and PFC aux winding charge pump power supply for fast startup start time under 250ms
- Multi-mode control (QR+DCM) flyback stage enables high efficiency and low dimming output
- High power factor (PF>0.9) and low input current total harmonic distortion (iTHD < 15%) across universal input voltage range (90 to 305Vac) and down to 30% load
- Short time-to-light down to 250ms
- Low Bill Of Materials (BOM)
- Configurable dimming curve to either linear or quadratic (eye-adaptive).
- Configurable minimum dimming current from 10% to 5%
- Intelligent thermal management with adaptive temperature protection
- Active bleeder for dim-to-off function
- Output independent forward mode auxiliary power supply for controller
- Isolated dimming interface with CDM10V

Note: *CDM10V is a fully integrated 0-10V dimming interface IC from Infineon which transmits secondary side analog voltage based signals from 0-10V dimmer to primary side, by driving an external opto-coupler with a 5mA current based PWM signal. For more details about CDM10V, please visit Infineon website: http://www.infineon.com/cdm10v.*

3 Design Specification

Table 1 and **Table 2** list the electrical specification and system protection of this reference design.

Table 1 Electrical Specification

Specification	Symbol	Value	Unit
AC Input voltage range	V_{IN_AC}	100 ~ 277 (+/-10%)	Vrms
DC Input voltage range	V_{IN_DC}	100 ~ 277 (+/-10%)	V
Output LED load range (includes dimming)[1]	V_{LED}	16 ~ 48	V
Non-dimmed full output current setting[2]	I_{out_set}	1500	mA
Total line and load regulation tolerance	-	± 2	%
Dimming input voltage range	V_{DIM}	0 ~ 10	V
PWM Dimming Frequency	f_{dim}	500 ~1500	Hz
Minimum output current setting[2]	$I_{out\_dim\_min}$	76	mA
Output current dimming curve[2]	C_{dim}	Linear/Quadratic	-
Efficiency (V_{out}: 48V, I_{out}: 1A, non-dimming)	η	< 89	%
Power factor (V_{in}: 90~277Vac +/-10%, V_{out}: 29~48V, >30% load)	PF	> 0.9	-
Input current total harmonic distortion (V_{in}: 90~277Vac +/-10%, V_{out}: 29~48V, >30% load)	iTHD	< 15	%

[1] Configurable in XPDL8220
[2] Configurable in XPDL8220

Table 2 System Protections

Protection	Symbol	Value	Unit
Nominal Input over-voltage protection level[1]	V_{in_OV}	320	Vrms
Nominal Input under-voltage protection level[2]	V_{in_UV}	72	Vrms
Nominal output over-voltage protection level[2]	V_{out_OV}	53	V
Nominal output over-current (average) protection level	$I_{out\_max\_avg}$	1800	mA
IC internal over-temperature detection threshold[2]	$T_{critical}$	119	°C
Input over-voltage protection reaction	$Reaction_{\_OVP\_Vin}$	Latch mode	-
Input under-voltage protection reaction	$Reaction_{\_UVP\_Vin}$	Auto-restart	-
Output over-voltage (output open) protection reaction[3]	$Reaction_{\_OVP\_Vout}$	Auto-restart	-
Output under-voltage (output short) protection reaction	$Reaction_{\_UVP\_Vout}$	Auto-restart	-
Output over-current (average) protection reaction	$Reaction_{\_Iout\_max\_avg}$	Auto-restart	-
IC over-temperature protection reaction	$Reaction_{\_TP}$	Latch mode	-
Auto-restart idle time[4]	$t_{auto\_restart}$	1	s
Fast auto-restart idle time[5]	$t_{fast\_auto\_restart}$	150	ms

[1] Protection can be disabled and its level can be configured.

[2] Protection cannot be disabled but its level can be configured.

[3] Protection reaction can be configured to either auto-restart or latch mode.

[4] Auto-restart time can be configured.

[5] Auto-restart time can be configured.

4 Schematic and Description

Figure 2 shows the complete schematic of the 50W reference design:

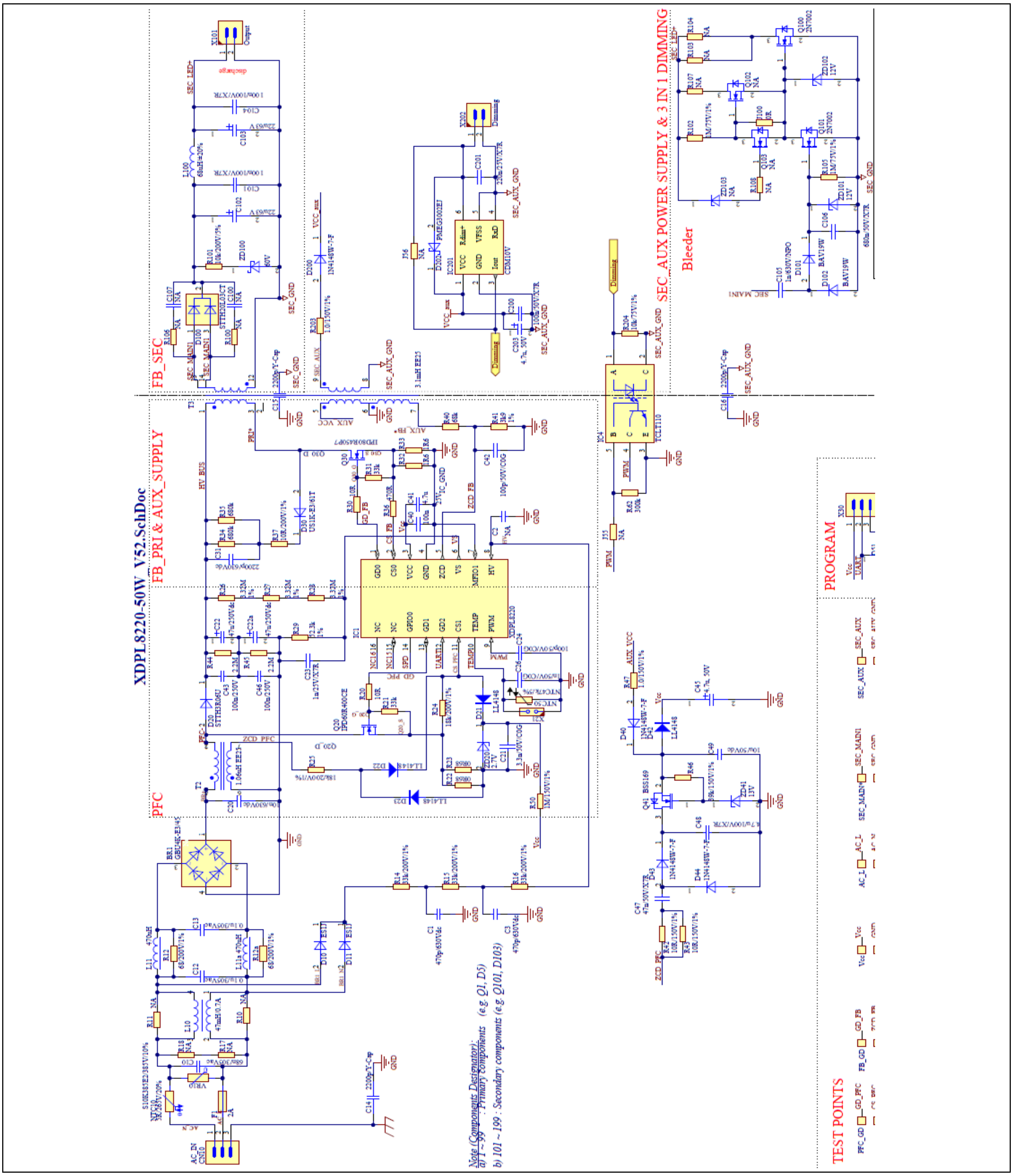


Figure 2 Schematic of the 50W reference design

The 50W reference design is made of 4 main parts: input filter stage, PFC stage, flyback stage and dimming stage.

4.1 Input Stage

Input stage provides the protection not only for the application circuit, but also for the AC net from switching noises. At the same time, it rectifies the AC input to DC for the PFC stage and provides the power for the IC controller before it can be supplied by the application circuit itself.

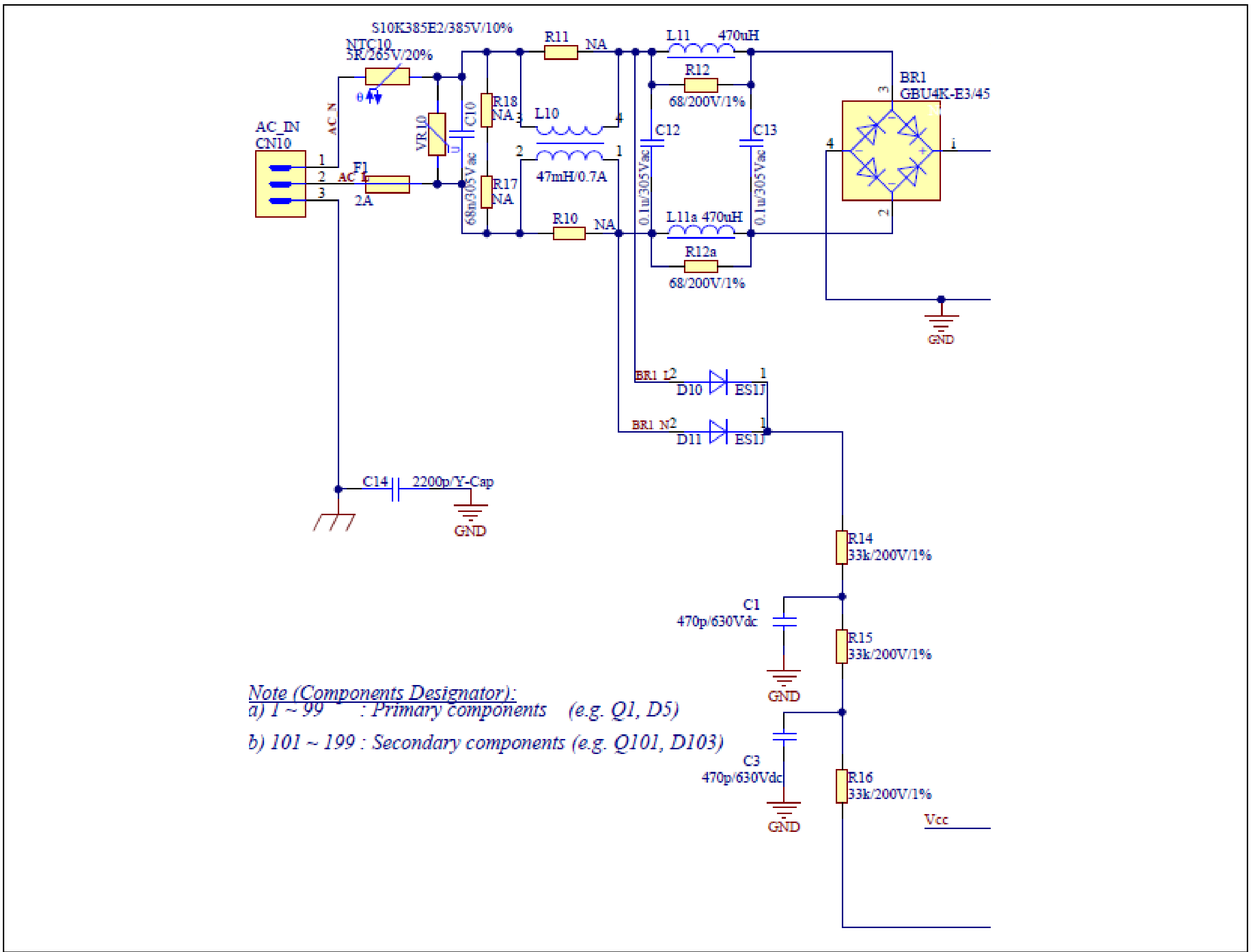


Figure 3 Input Stage

It includes the following parts:

1) NTC to limits the inrush current which charges the bus capacitors at AC plug in
2) Varistor VR10 to protect the primary circuit from AC input over-voltage
3) X-cap discharge resistor R17, R18
4) Common mode choke to suppress the common mode noise to the mains
5) Differential filter to suppress the differential mode noise to the mains
6) Full bridge rectifier
7) Full wave AC rectification D10, D11 and current limitation R14, R15, R16 for the IC high voltage start-up cell via HV pin to charge the Vcc capacitor at the cold start-up before PFC and Flyback running

4.2 PFC Stage

PFC stage boosts the rectified AC voltage to a higher DC voltage with much smaller ripple. Meanwhile it shapes the input current to comply with the regulatory requirements and reduces the harmonic distortion back to the AC mains.

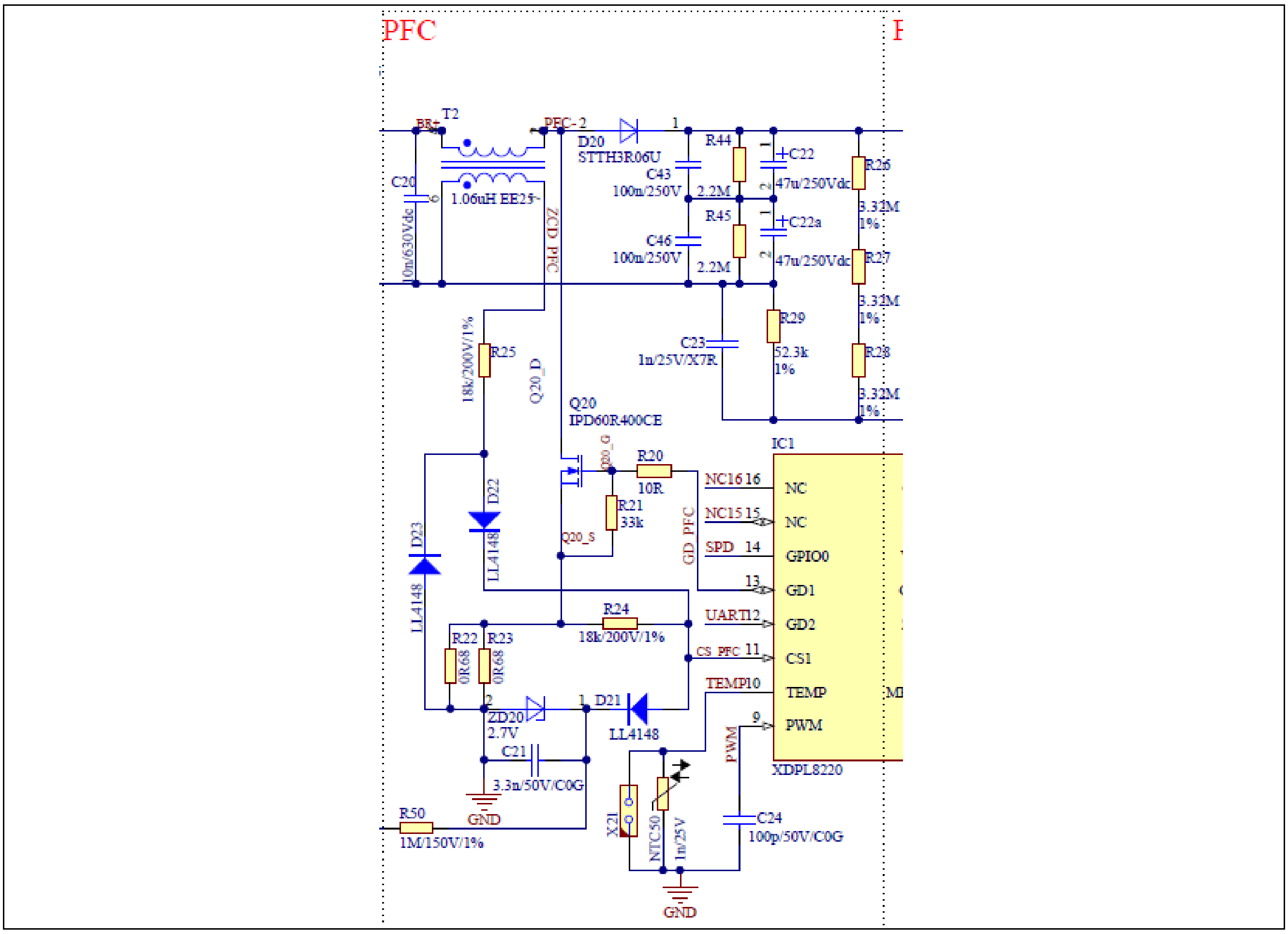


Figure 4 PFC Stage

It includes following parts:

1) Main PFC components with PFC choke T2, PFC power block diode D20 and PFC MOS-FET Q20
2) Clamping circuit network for integration of Zero Crossing Detection(ZCD) and Current Sense (CS) for PFC at the same CS pin
3) High frequency bypass capacitor C43, C46 and DC bus capacitor C22, C22a
4) Bus voltage sensing divider R26, R27, R28, R29 for DC bus voltage regulation
5) Aux winding of the PFC choke for ZCD function and provides the power for the IC at the same time before the flyback stage is active. Together with charge pump, it reduces the Vcc capacitor value and so that the charging time for the Vcc capacitor through the start-up cell is very short which enable a very fast time-to-light around 250ms at low line.

4.3 Flyback Stage

Flyback stage converts the boosted DC bus voltage down to a lower DC voltage in a range of 16V to 48VDC for the LED light engine. It can be split into four parts: primary side, primary aux side, secondary side and secondary aux side:

1) Both output voltage and current are sensed at the primary aux winding and then regulated by the controller XDPL8220.
2) Secondary side provides power for the LED engine with filter and protection functions.
3) Secondary aux winding provides power for the CDM10V which enables the dimming function.
4) Primary aux winding provides the power for the controller XDPL8220 after flyback stage is active.

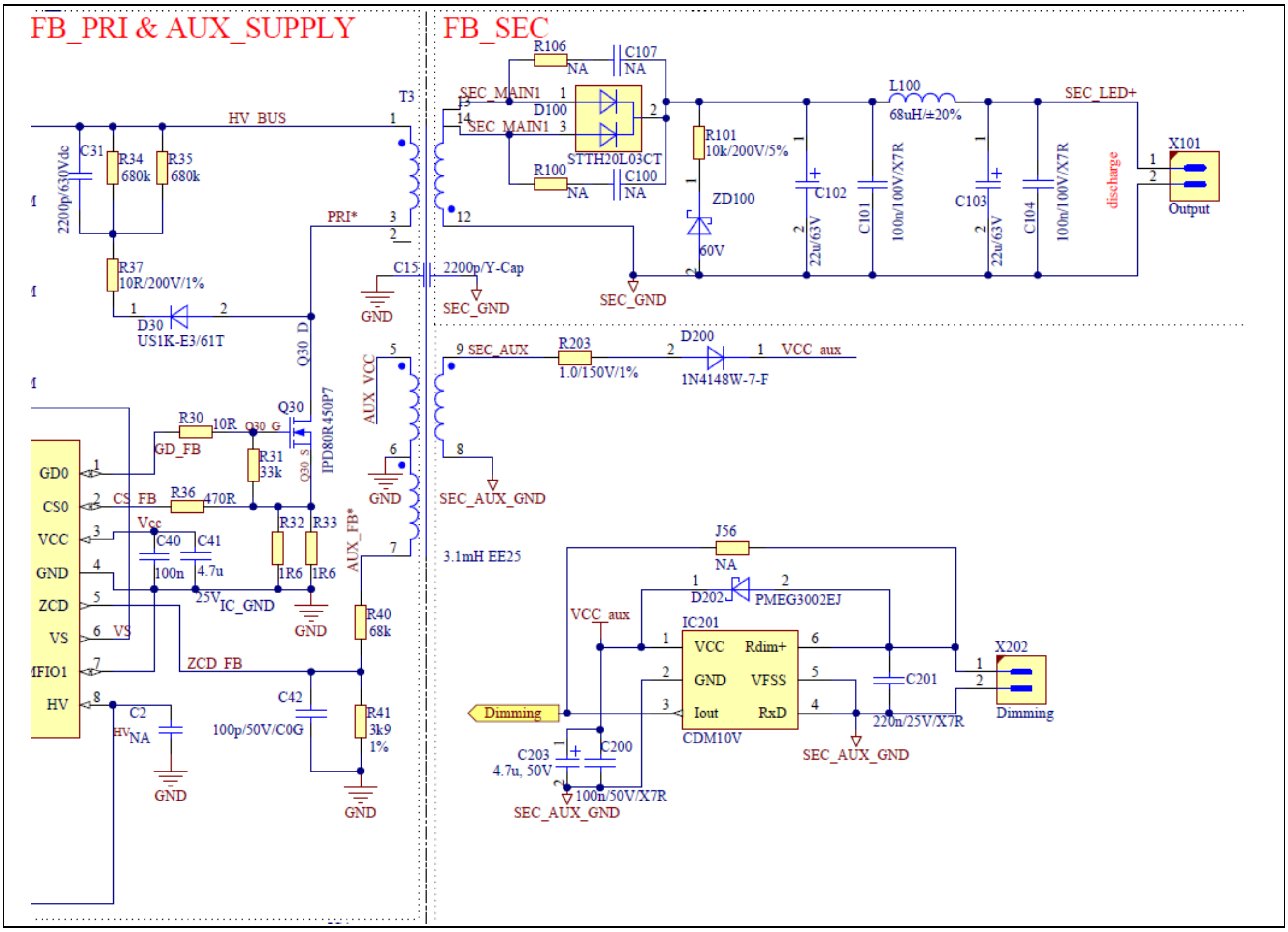


Figure 5 Flyback Stage

4.3.1 Flyback Primary Side

Flyback primary side includes following parts:

1) The regulated power to the secondary side is controlled through the transformer T3 by switching of the power MOS-FET Q30.
2) Snubber network suppress the oscillation in the flyback main power path while MOS-FET Q30 turns off.
3) Current shunt resistors R32 and R33

4.3.2 Flyback Primary Aux Side

Flyback primary aux side includes following parts:

1) ZCD divider R40 and R41 for the zero crossing detection function which enables the valley switching
2) Forward mode power supply for the controller XDPL8220. This makes the Vcc power supply independent from the wide output voltage range and a regulator is not required.

4.3.3 Flyback Secondary Side

Flyback primary aux side includes following parts:

1) Rectifier D100 with snubber network R100 and C100
2) R101 and ZD100 protects the output from over-voltage
3) PI filter network suppresses the output noise

4.3.4 Flyback Secondary Aux Side

The dimming controller CDM10V is supplied by forward mode at the secondary aux winding. This makes the power supply independent from the wide output voltage range and a regulator is not necessary.

4.4 IC Power Supply

The IC power supply comprises three parts as shown in the **Figure 6**:

- After the AC/DC input is plugged and before XDPL8220 is active, the IC is power supplied by the depletion cell which connected to the input via HV pin. Vcc capacitors are charged till the voltage reaches around 20.5V. After the XDPL8220 is active, there is no power supply until the PFC stage is active. So the Vcc will drop during this period. It is important to design the Vcc capacitors properly so that the Vcc voltage does not drop below the under voltage threshold.
- When the PFC stage is active, XDPL8220 gets the power supply from the PFC aux winding through the charge pump consists of R42, C47, D44, D43. The advantage of PFC aux winding supply with charge pump is that the Vcc capacitors don't need to be designed so large so that Vcc should be hold above under voltage threshold until the Flyback stage is active. This helps to achieve a fast time to light at the low line condition.
- After the bus voltage reaches the defined threshold at which flyback stage is active, the power supply for XDPL8220 is then taken over by flyback aux winding in the forward mode.

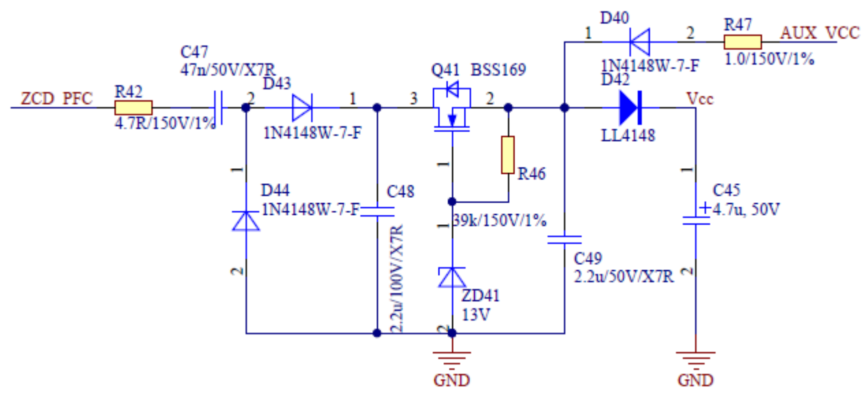


Figure 6 Forward Mode Vcc Power Supply

4.5 Dimming Stage

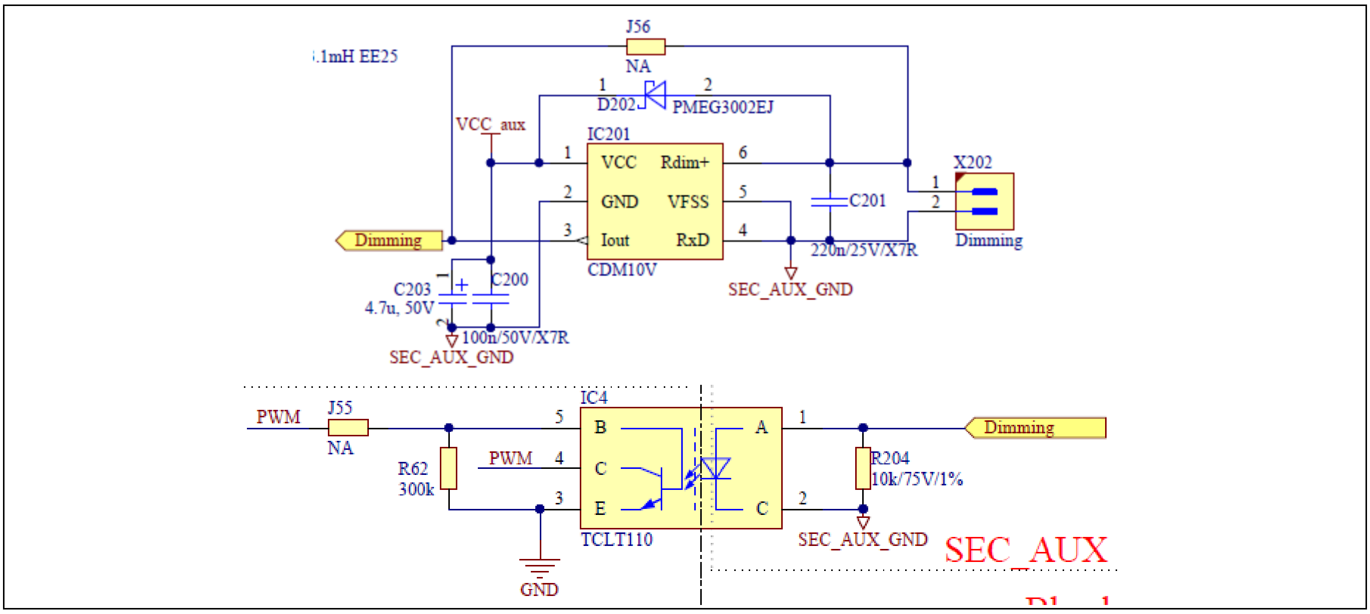


Figure 7

Dimming stages is controlled by the CDM10V as shown in the **Figure 7**. This controller enables isolated dimming function:

1) The PWM dimming signal can be directly supplied at the connector X202 or
2) An analog 0-10V/1-10V dimmer can be connected directly at X202 and sink current is supplied by the CDM10V.
3) An opto-coupler is needed for the communication from the secondary side by CDM10V to the primary side to XDPL8220.
4) Resistor R204 provides bypass for the leakage current out of CDM10V
5) Resistor R62 ensures the fast turn-off of the opto-coupler.

4.6 Bleeder

The bleeder block as shown in the figure 8 is used to discharge the LED output capacitors in the following conditions:

1) Fast auto-restart mode: in the dim-to-off condition, XDPL8220 enters the fast auto-restart mode and output voltage is discharged to around 12V and stabilize there so that the LED engine will not light
2) Auto-restart mode: if XDPL8220 enters the protection mode and output will be periodically discharged so that the output voltage will not exceed the output over voltage protection level.
3) Latch mode: if XDPL8220 enters latch mode due to certain critical failure, output voltage will be completely discharged.
4) Input unplugged: if the AC/DC input power supply is unplugged, the output voltage will be completely discharged.

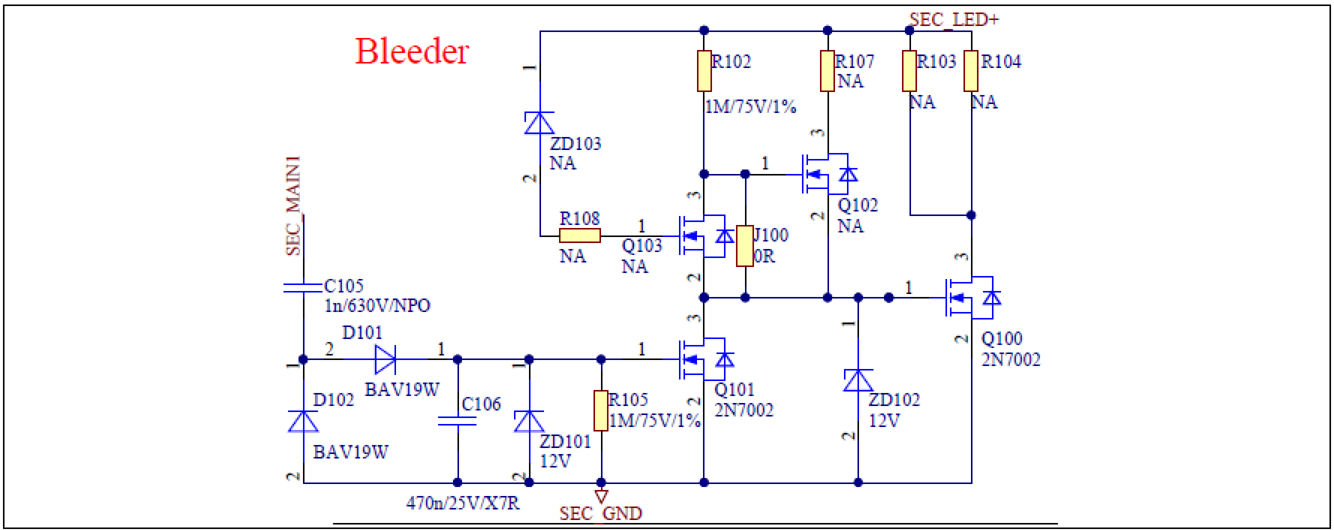


Figure 8 Active Bleeder

It includes following part:

1) Charge pump (C105, D102, D101) charges the C106 every switching cycle till it stabilizes at 12V
2) ZD101 clamps the voltage at C106 not higher than 12V
3) Passive bleeder resistor R102 discharges the LED output always slowly
4) Active bleeder resistors R103 and R104 discharge the LED output only when C106 is not charged anymore and discharged by R105 and Q101 switches off.
5) Q101 is on as long as flyback stage is in the normal operation so that Q100 is switched off
6) Anytime if the flyback stage stops the operation, Q101 is turned off and Q100 is on, output is discharged through R103, R104 and Q100.

4.7 External Adaptive Temperature Protection

External adaptive temperature protection function is realized by connect an external NTC resistor to the TEMP pin of XDPL8220. This NTC resistor usually locates near the LED engine so that it can be protected from the over-temperature. The controller XDPL8220 senses the NTC resistor value change caused by the temperature variation and regulates the output current for LED engine according to its temperature.

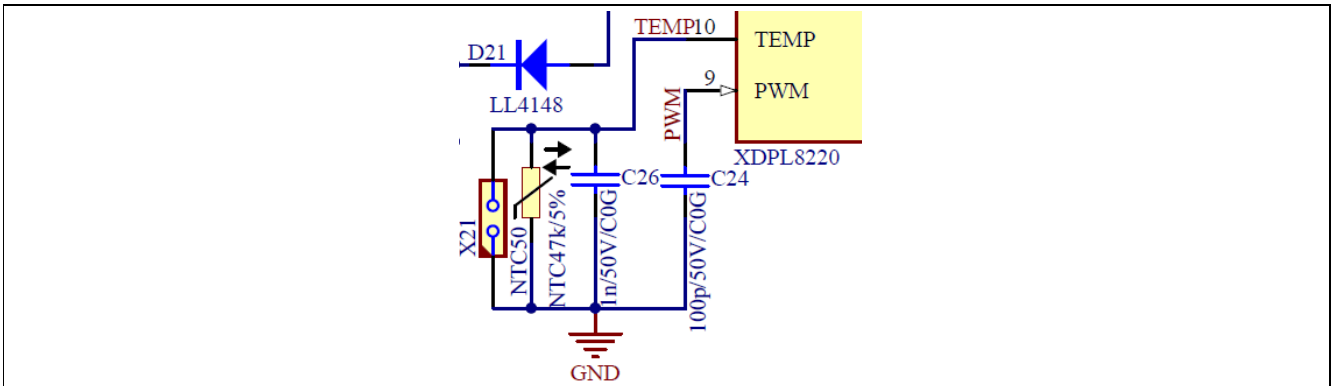


Figure 9 External NTC connection

4.8 Programming Interface

Programming interface is at the connector X30. This interface is necessary for configuration of the application related parameters through the hardware .dp Interface Gen2 and the software .dpVision.

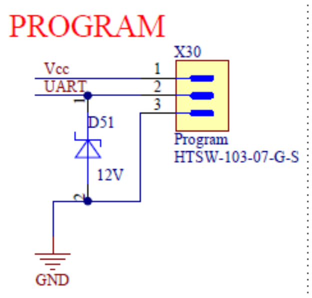


Figure 10 Programming Interface

5 PCB Layout

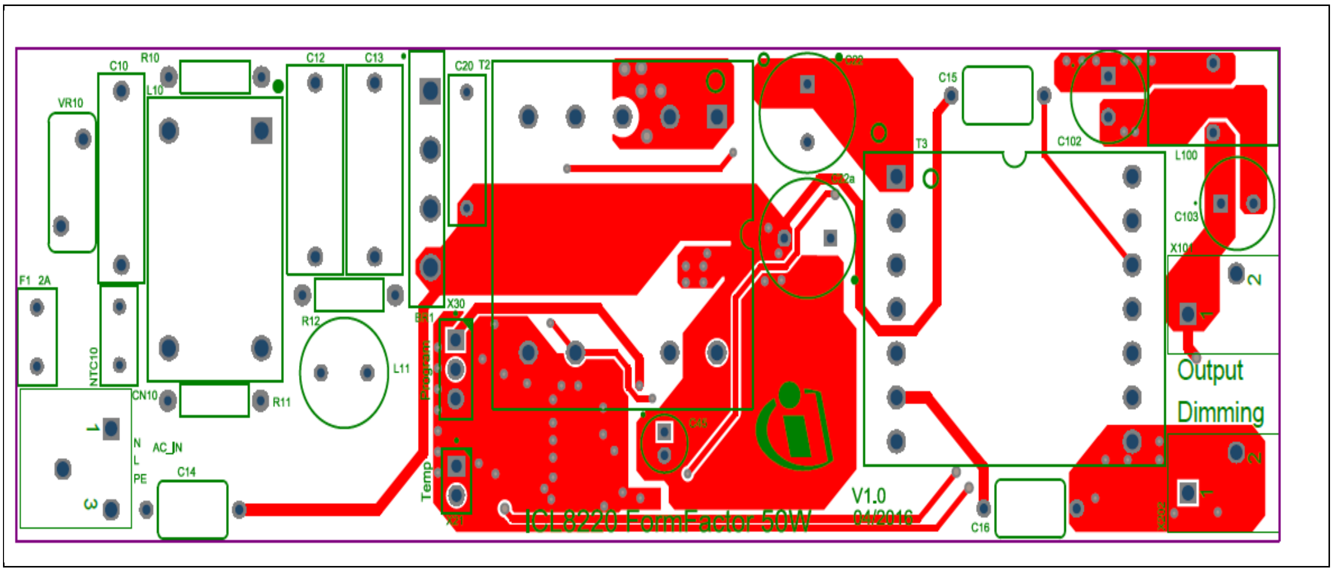


Figure 11 PCB Top

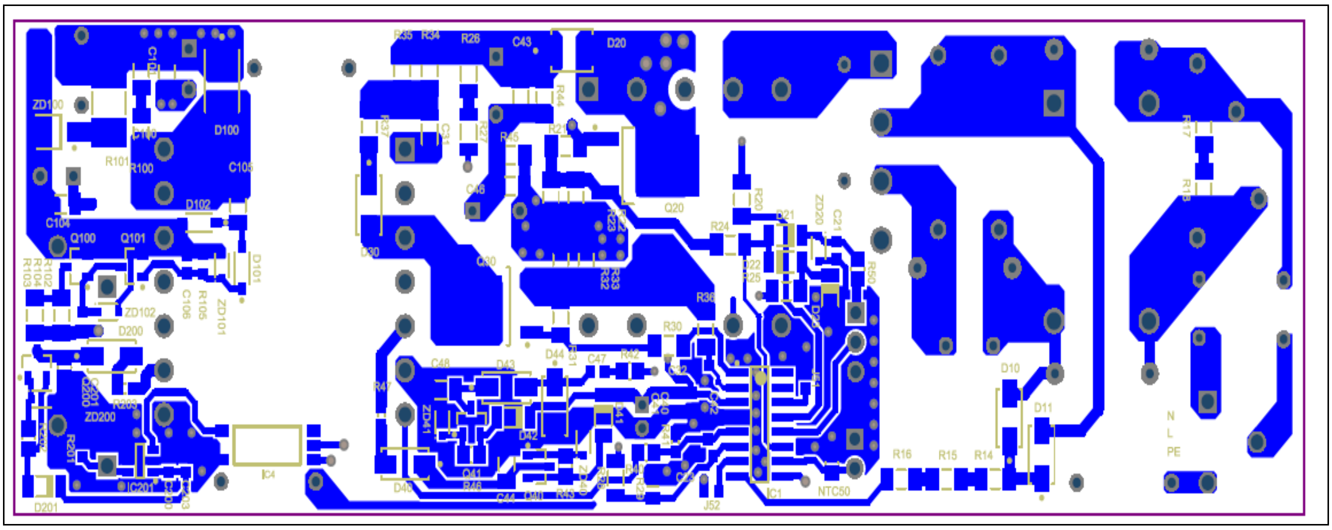


Figure 12 PCB Bottom

6 Performance

In this chapter, the measurement results of the 50W reference design with 6 LEDs (Table 2), 10 LEDs (Table 3) and 16 LEDs (Table 4) are listed for your easy reference. All measurements are done with the 50W parameters defined in the CSV configuration file (see [4]).

6.1 V_{OUT} = 16 V

Table 3 Measurement result with 6 LEDs

V_{IN} (V_{AC})	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	Power Factor	THD (%)	η (%)
100	34.67	18.6	1.51	98.88	14.70	81.57
120	34.26	18.61	1.51	99.36	9.96	82.56
140	33.85	18.61	1.51	99.16	11.05	83.55
200	33.44	18.61	1.51	98.74	8.76	84.60
220	33.36	18.61	1.51	98.43	8.37	84.78
230	33.35	18.61	1.52	98.25	8.11	84.80
240	33.34	18.60	1.52	98.04	8.00	84.85
265	33.31	18.60	1.52	97.39	7.83	84.94
277	33.26	18.6	1.52	96.99	8.21	86.99

6.2 V_{OUT} = 29 V

Table 4 Measurement result with 10 LEDs

V_{IN} (V_{AC})	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	Power Factor	THD (%)	η (%)
100	56.60	30.76	1.51	99.17	12.36	82.35
120	54.87	30.76	1.51	99.08	13.31	84.97
140	54.54	30.76	1.51	99.43	9.62	85.48
200	53.33	30.76	1.51	99.18	10.06	87.43
220	53.27	30.76	1.51	99.17	7.39	87.54
230	53.22	30.76	1.51	99.09	7.42	87.62
240	53.14	30.76	1.51	99.00	7.26	87.74
265	52.99	30.76	1.51	98.70	7.28	88.00
277	52.91	30.77	1.51	98.52	7.36	88.14

6.3 V_{OUT} = 48 V

Table 5 Measurement result with 16 LEDs

V_{IN} (V_{AC})	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	Power Factor	THD (%)	η (%)
100	52.45	47.45	0.94	99.15	12.19	85.19
120	52.01	47.45	0.94	99.43	8.80	85.38
140	51.66	47.45	0.94	99.35	9.54	87.16
200	50.96	47.45	0.94	99.21	7.94	88.30
220	50.80	47.44	0.94	99.10	7.31	88.45
230	50.71	47.44	0.94	99.01	7.67	88.60
240	50.53	47.42	0.94	98.90	7.34	88.65
265	50.32	47.41	0.94	98.56	7.09	88.75
277	50.25	47.40	0.94	98.37	7.36	88.89

Note: Due to the limited power mode, the current is limited so that the output power does not exceed the defined 50W.

6.4 0 – 10 V Dimming

This section provides measurement results for the 0 - 10 V dimming feature. A quadratic curve was configured for this measurement. Using the .dpVision GUI [3] the dimming curve can also be configured to a linear curve. The measurement was done for an input voltage of 230 V, 50 Hz and an output load of 16 LEDs (48 V at maximum current).

Table 6 Output current at different dimming voltages

Vdim (V)	**0.50**	**1.00**	**1.50**	**2.00**	**2.50**	**3.00**	**3.50**	**4.00**	**4.50**	**5.00**
Io (A)	**0.071**	**0.071**	**0.071**	**0.071**	**0.083**	**0.125**	**0.188**	**0.263**	**0.367**	**0.468**
Vdim (V)	5.50	6.00	6.50	7.00	7.50	8.00	8.50	9.00	9.50	10.00
Io (A)	**0.597**	**0.735**	**0.889**	**0.954**	**0.964**	**0.973**	**0.984**	**1.003**	**1.014**	**1.021**

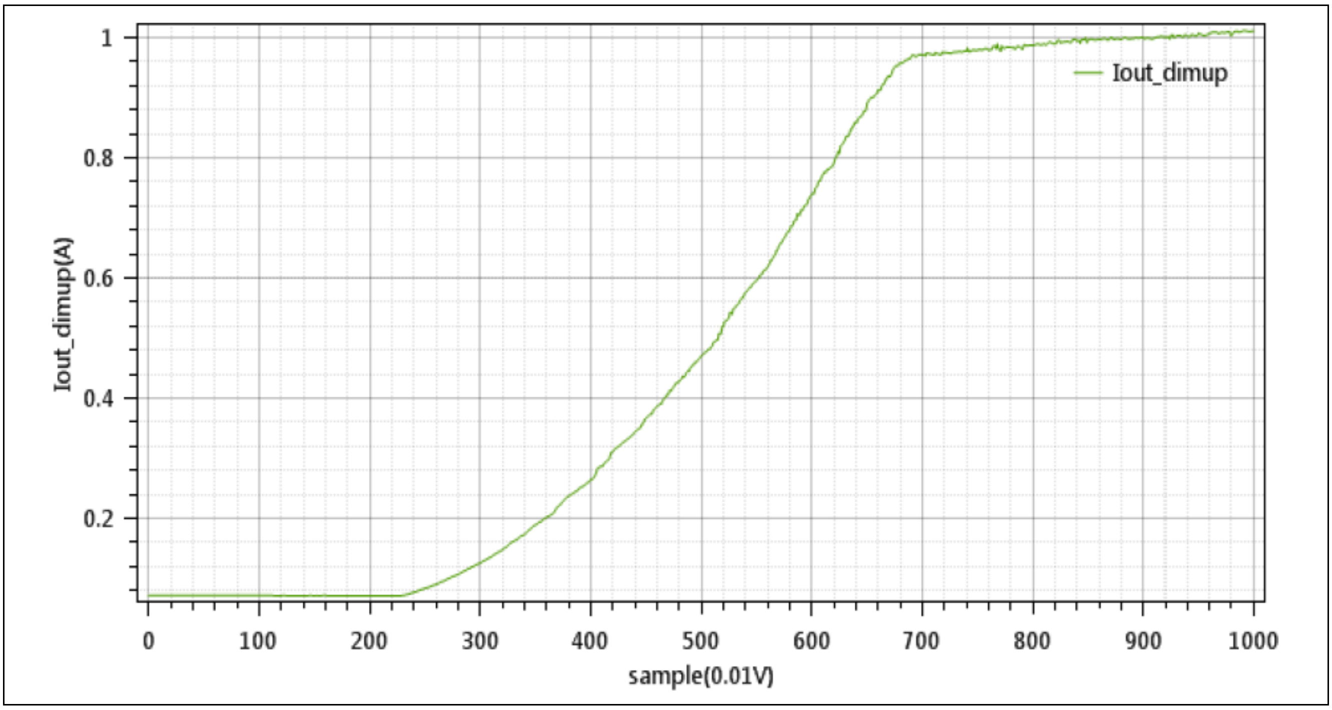


Figure 13 Dimming curve adapted to the sensitivity of the eye

6.5 PWM Dimming

This section provides measurement results for the PWM dimming feature. A quadratic curve was configured for this measurement. Using the .dpVision GUI [3], the dimming curve can also be configured to a linear curve. The measurement was done for an input voltage of 230 V, 50 Hz and an output load of 16 LEDs (48V at maximum current).

Table 7 Output current at different dimming duty cycles

Vdim (V)	5%	10%	15%	20%	35%	50%	75%	100%
Io (A)	0.074	0.074	0.074	0.077	0.206	0.436	0.931	0.943

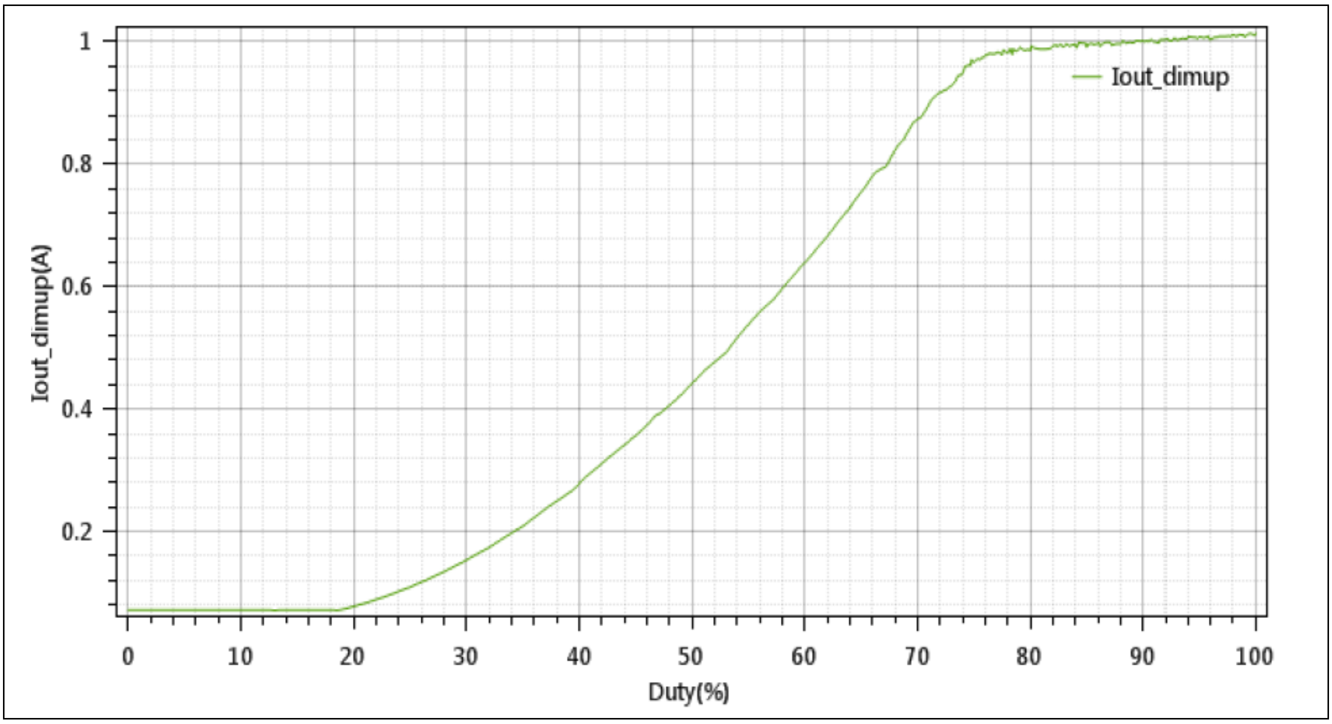


Figure 14 Dimming curve adapted to the sensitivity of the eye

7 Bill of Materials

Quantity	Designator	Value	Description	Manufacturer	ManufacturerPartNumber
1	BR1	GBU4K-E3/45	Bridge Rec 4 Amp, 800V, SIP4	Diodes	GBU4K-E3/45
2	C1, C3	470p	Cap-1206-470p/630V/5%/C0G	Murata	GRM31A5C2J471JW01D
1	C10	68n	EMI Cap 68n/305V/X2/10%	TDK	B32922C3683K
2	C12, C13	0.1u	EMI Cap 100n/305Vac, B32922	TDK	B32922C3104K
3	C14, C15, C16	2200p/Y-Cap	Y-Cap 2200pF/250V/pitch 10	Murata	DE1E3KX222MA5B
1	C20	10n	MKT, 10nF/630V/± 10%, 15mm, 4x12.5mm	Vishay	BFC237261103
1	C21	3.3n	Cap-0603-3.3n/50V/0.05/C0G	Kemet	C0603C332J5GACTU
2	C22, C22a	47u	Al-Cap-47u/250V/ 20%/pitch 5x10x25	Rubycon	250BXW47MEFR10X25
1	C23	1n	Cap-0603-1n/25V/0.1/X7R	AVX	06033C102K4Z2A
2	C24, C42	100p	Cap-0603-100p/50V/0.01/C0G	AVX	06035A101FAT2A
1	C25	1n	Cap-0603-1n/50V/0.01/C0G	Murata	GRM1885C1H102F
1	C31	2200p	Cap-1206-2200p/630V/10%/X7R	Murata	GRM31BR72J222KW01L
1	C32	330p	Cap-0603-330p/50V/0.05/C0G	Kemet	C0402C331J5GACTU
2	C40, C200	100n	Cap-0603-100n/50V/0.1/X7R	AVX	06035C104K4Z2A
1	C41	4.7u	Cap-0603-4.7u/25V/10%/X5R	Murata	GRM188R61E475KE11D
2	C43, C46	100n	Cap-1206-100n/250V/10%/X7R	Murata	GRM31CR72E104KW03L
2	C45, C203	4.7u	Al Cap 4.7uF/50V/pitch 2mm	Panasonic	EEUFC1H4R7
1	C47	47n	Cap-0603-47n/50V/0.1/X7R	Murata	GRM188R71H473KA61D
1	C48	2.2u	Cap-1206-2.2u/100V/0.1/X7R	Murata	GRM31CR72A225KA73L
1	C49	2.2u	Cap-1206-2.2u/50V/0.1/X7R	Kemet	C1206C225K5RAC
2	C101, C104	100n	Cap-1206-100n/100V/0.1/X7R	TDK	C3216X7R2A104K160AA
2	C102, C103	22u	Al-Cap 22uF/ 63V/pitch 3.5/DxH8,00x12.00mm	Wuerth Elektronik	870055874002
1	C105	1n	Cap-1206-1n/630V/0.5/NPO	TDK	CGA5F4C0G2J102J085AA
1	C106	470n	Cap-0603-470n/25V/0.2/X7R	Kemet	C0603C474M3RACTU
1	C201	220n	Cap-0603-220n/25V/0.2/X7R	Kemet	C0603C224K3RACTU
1	CN10	691412120003MB	7.92 mm Contact Pitch, Right Angle Header	Wuerth Electronics	691412120003MB
2	D10, D11	ES1J	UltraFast Diode 600V/1A/DO-214AC	Fairchild Semiconductor	ES1J
1	D20	STTH3R06U	Ultrafast Diode 600V/3A/DO-214AA	STMicroelectronics	STTH3R06U
4	D21, D22, D23, D42	LL4148	Diode 100V, 200mA, SOD80(Melf)	Fairchild Semiconductor	LL4148
1	D30	US1K-E3/61T	Ultrafast Diode 800V/1.0A/DO-214AC	Vishay General Semiconductor	US1K-E3/61T
4	D40, D43, D44, D200	1N4148W-7-F	Surface Mount Fast Switching Diode	Diodes Incorporated	1N4148W-7-F
1	D51	PESD12VS1UB	Unidirectional ESD Protection Diode / 12V	NXP Semiconductors	PESD12VS1UB
1	D100	STTH20L03CT	Dual Diode, TO220AB, 100V, CC	STMicroelectronics	STTH20L03CT
2	D101, D102	BAV19W	Diode 100V, 400mA, SOD123	Diodes Inc.	BAV19W
1	D202	PMEG3002EJ	Schottky Diode / 30V, 200mA, SOD323	NXP Semiconductors	PMEG3002EJ

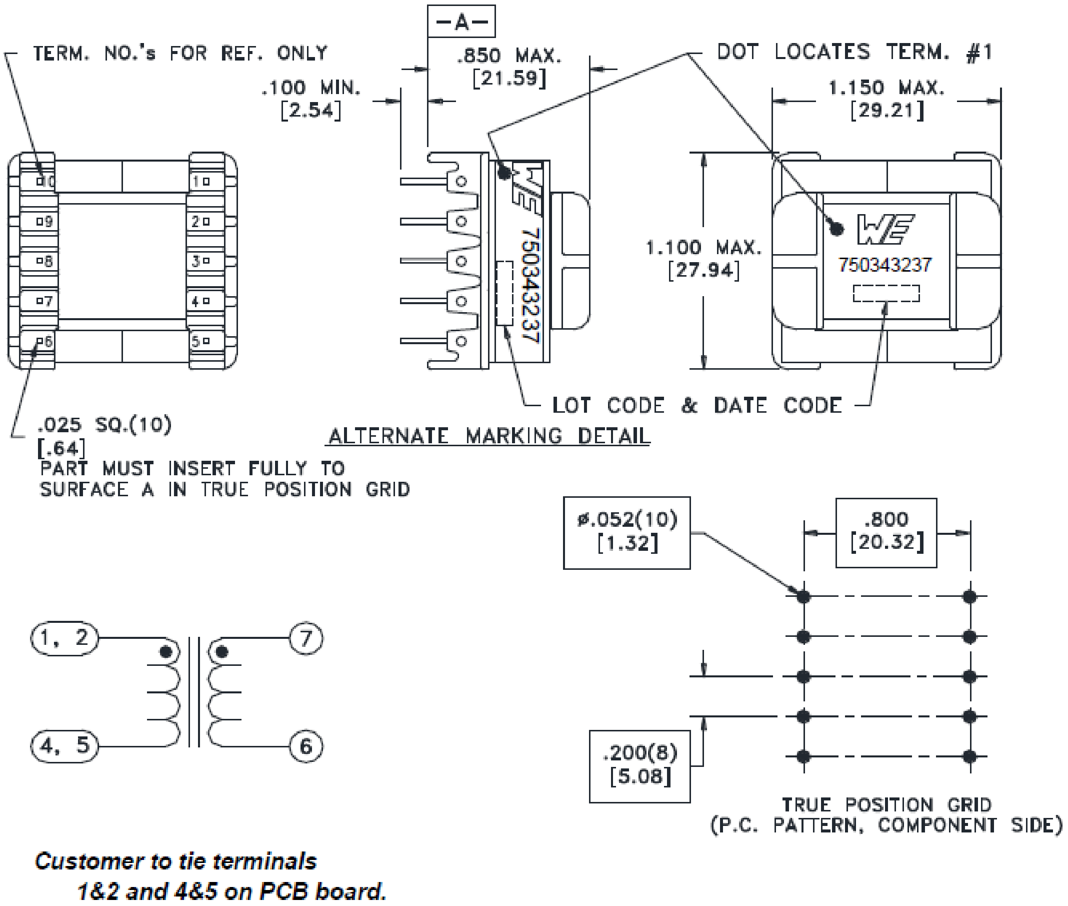
1	F1	2A	Radial Lead Fuse Rectangular - Slow Blow, 2A, 250V	Multicomp	MST 2A 250V
1	IC1	XDPL8220	LED Combo Control IC for PFC and FB Conversion	Infineon Technologies	XDPL8220
1	IC4	TCLT110	Optocoupler, Phototransistor Output, CTR 100% - 200% at 10mA, (Operating Temp -55°C - 100°C)	Vishay	TCLT1103
1	IC201	CDM10V	Dimming Interface IC SOT-23-6	Infineon Technologies	CDM10V
2	J51, J100	0R	0R/50V	Bourns	CR0603-J/-000ELF
1	L10	47mH/0.7A	Choke 47mH/0.7A/B82732F	Epcos	B82732F2701B001
2	L11, L11a	470uH	470uH, 1.15A, 0R47, pitch 5mm, 13 x 10 x 15mm	Wuerth	7447480471
1	L100	68uH	WE-FI Leaded Toroidal Line Choke	Wurth Elektronik	7447033
1	NTC10	5R	5R/265V/20%	Epcos	B57235S0509M000
1	NTC50	1n	Cap-0603-1n/25V/0.1/X7R	AVX	06033C102K4Z2A
1	Q20	IPD60R400CE	CoolMOS CE, 650V, 14.7A, DPAK	Infineon Technologies	IPD60R400CE
1	Q30	IPD80R450P7	CoolMOS™ P7, 800V, 11A, DPAK	Infineon Technologies	IPD80R450P7
1	Q41	BSS169	MOSFET N-Ch, 100V, 90mA, 12Ohm, SOT23	Infineon Technologies	BSS169
2	Q100, Q101	2N7002	OptiMOS Transistor 60V, 3Ohm, 300mA,SOT23	Infineon Technologies	2N7002
2	R12, R12a	68	68/200V/1%	TE CONNECTIVITY	352068RJT
5	R14, R15, R16, R21, R31	33k	33k/200V/1%	Yageo/Phycomp	RC1206FR-0733KL
3	R20, R30, R37	10R	10R/200V/1%	Yageo/Phycomp	RC1206FR-7W10RL
2	R22, R23	0R68	0.68/675mV/1%	Vishay	RCWE1206R680FKEA
2	R24, R25	18k	18k/200V/1%	Yageo/Phycomp	RC1206FR-0718KL
3	R26, R27, R28	3.32M	3.32M/200V/1%	Vishay	CRCW12063M32FKEA
1	R29	52.3k	52.3k/150V/1%	Panasonic	ERJP06F5232V
2	R32, R33	1R6	1.6/200V/1%	Bourns	CRM1206-FW-1R60 E LF
2	R34, R35	680k	680k/200V/1%	Yageo/Phycomp	RC1206FR-07680KL
1	R36	470R	470R/200V/1%	Yageo/Phycomp	RC1206FR-07470RL
1	R40	68k	68k/150V/1%	Yageo/Phycomp	RC0805FR-0768KL
1	R41	3k9	3.9k/50V/1%	Yageo/Phycomp	RC0603FR-073K9L
1	R42	4.7R	4.7R/150V/1%	Vishay	CRCW08054R70FKEA
2	R44, R45	2.2M	2.2M/200V/1%	Yageo/Phycomp	RC1206FR-072M2
1	R46	39k	39k/150V/1%	Yageo/Phycomp	RC0805FR-0739KL
2	R47, R203	1.0	1.0/150V/1%	Yageo/Phycomp	RC0805FR-071RL
1	R50	1M	1M/150V/1%	Yageo/Phycomp	RC0805FR-071ML
1	R62	300k	300k/75V/1%	Vishay	CRCW0603300KFKEA
1	R101	10k	10k/200V/5%/2512	Yageo	RC2512JK-0710KL
2	R102, R105	1M	1M/75V/1%	Yageo/Phycomp	RC0603FR-071ML
1	R204	10k	10k/75V/1%	Yageo/Phycomp	RC0603FR-0710KL
1	T2	1.06uH EE25	EE25 1060uH, 2A, N87, Gab 1.5mm	Wuerth Electronics	750343237, Rev01
1	T3	3.1mH EE25	EE25_14Pin, 3.1mH, 0.8A	Wuerth Electronics	750343127,Rev01
1	VR10	S10K385E2K1	S10K385E2K1/385V/10%	Epcos	B72210S0381K101
1	X30	HTSW-103-07-G-S	Through hole .025" SQ Post Header, 2.54mm pitch, 3 pin, vertical, single row	Samtec	HTSW-103-07-G-S

2	X101, X202	691412120002MB	Through-hole Shrouded Header, Top Entry, Vertical, 2.5mm Pitch, 2 Pins, Single Row, White	Wuerth Electronics	691412120002MB
1	ZD20	BZX384-C2V7	Zener Diode / 2.7V/SOD-323	NXP	BZX384-C2V7
1	ZD41	BZX384-C13	Zener Diode / 13V/SOD-323	NXP	BZX384-C13
1	ZD100	SS16HE3	Schottky Diode / 60V/1A/DO-214AC	Vishay General Semiconductor	SS16-E3/5AT
2	ZD101, ZD102	BZX384-C12	Zener Diode / 12V/SOD-323	NXP	BZX384-C12
0	C2	NA	GRM-Series General Purpose Monolithic Ceramic Capacitor	Murata	GRM31A5C2J471JW01D
0	C100, C107	NA	Cap-1206-1n/100V/0.1/X7R	AVX	12061C102KAT2A
0	J55, J56	NA	0R/50V	Bourns	CR0603-J/-000ELF
0	Q102, Q103	NA	OptiMOS Transistor 60V, 3Ohm, 300mA,SOT23	Infineon Technologies	2N7002
0	R10, R11	NA	510K/350V/5%	Welwyn Components Limited	MFP1-510KJI
0	R17, R18	NA	1M/200V/1%	Yageo/Phycomp	RC1206FR-071M0L
0	R100, R106	NA	47R/200V/1%	Yageo/Phycomp	RC1206FR-0747RL
0	R103, R104	NA	2k/200V/1%	Vishay	CRCW12062K00FKEA
0	R107, R108	NA	100k/150V/1%	Yageo/Phycomp	RC0805FR-07100KL
0	X21	NA	Through hole .025" SQ Post Header, 2.54mm pitch, 2 pin, vertical, single row	Samtec	TSW-102-07-L-S
0	ZD103	NA	Zener Diode / 24V/SOD-323	NXP	BZX384-C12

7.1 Transformer Specifications

This section provides the transformer design data. The necessary steps to design a transformer based on the design specification can be found in the XDPL8220 Design Guide [2]

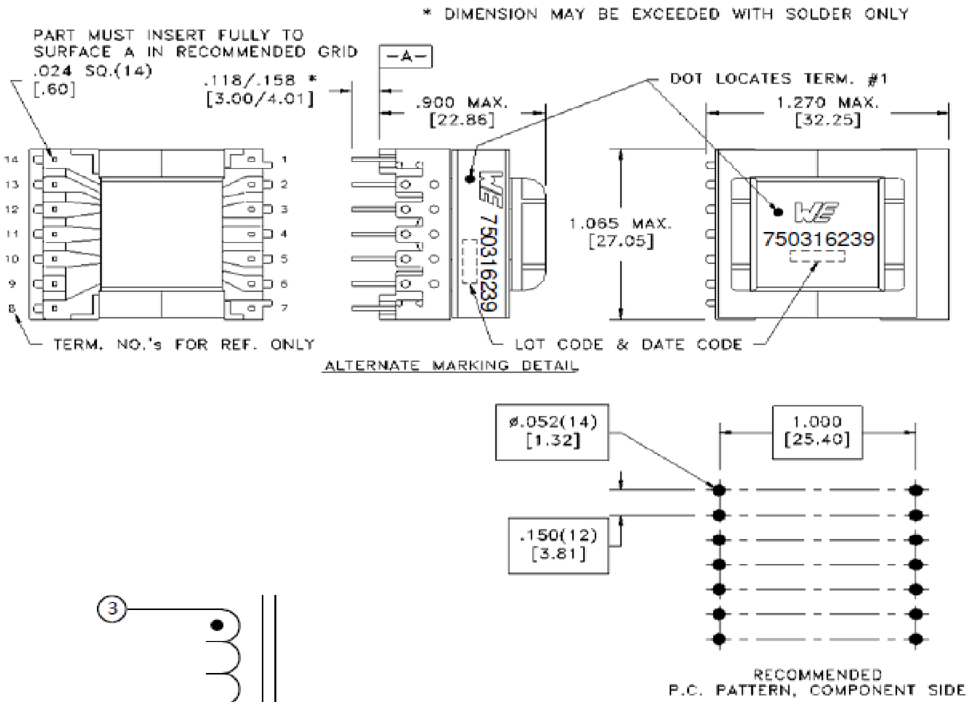
PFC choke

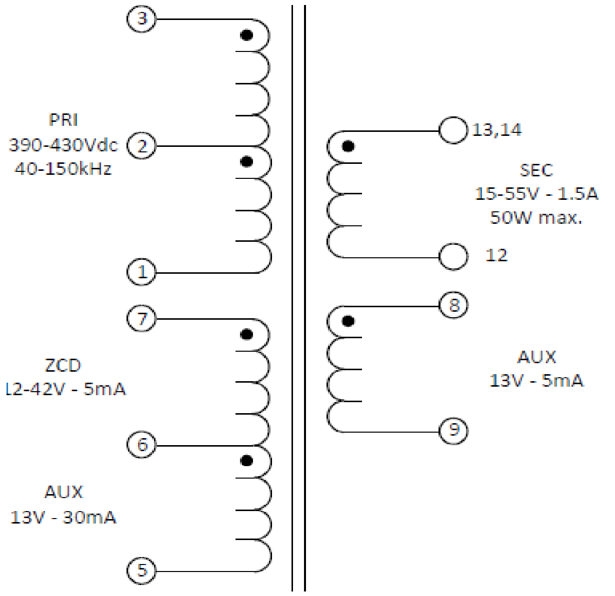


ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	2-4	tie(1+2, 4+5), @20°C	0.810 ohms max.
D.C. RESISTANCE	7-6	@20°C	0.050 ohms max.
INDUCTANCE	2-4	tie(1+2, 4+5),10kHz, 100mV, Ls	1060.00uH ±10%
SATURATION CURRENT	2-4	tie(1+2, 4+5), 20% rolloff from initial	2A
LEAKAGE INDUCTANCE	2-4	tie(1+2, 4+5,6+7),100kHz, 100mV, Ls	100µH max.
DIELECTRIC	5-6	tie(4+5), 1875VAC, 1 second	
TURNS RATIO		(2-4):(7-6), tie(1+2, 4+5)	9.69:1, ±2%

Flyback Transformer





ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	3-1	@20ºC	3.80 ohms ±10%
D.C. RESISTANCE	6-5	@20ºC	0.250 ohms ±10%
D.C. RESISTANCE	7-6	@20ºC	1.35 ohms ±10%
D.C. RESISTANCE	8-9	@20ºC	0.260 ohms ±10%
D.C. RESISTANCE	14-12	@20ºC	0.260 ohms ±10%
D.C. RESISTANCE	13-12	@20ºC	0.260 ohms ±10%
INDUCTANCE	3-1	10kHz, 100mV, Ls	2.00mH ±10%
SATURATION CURRENT	3-1	20% rolloff from initial	1.5A
LEAKAGE INDUCTANCE	3-1	tie(12+13+14),100kHz, 100mV, Ls	50µH typ., 100µH max.
DIELECTRIC	1-14	tie(3+5, 12+9), 3900VAC, 1 second	3900VAC, 1 minute
DIELECTRIC	1-7	tie(5+9, 3+12), 625VAC, 1 second	
TURNS RATIO		(3-2):(2-1)	1:1, ±1%
TURNS RATIO		(3-1):(6-5)	30:1, ±1%
TURNS RATIO		(3-1):(7-6)	5:1, ±1%
TURNS RATIO		(3-1):(8-9)	25:1, ±1%
TURNS RATIO		(3-1):(13-12)	3.95:1, ±1%
TURNS RATIO		(3-1):(14-12)	3.95:1, ±1%

8 Configuration setup and procedures

8.1 XDPL8220 Configuration

Tools needed for XDPL8220 parameters configuration are listed in **Table 8**.

Table 8 Tools needed for XDPL8220 parameters configuration

Tools type	Tools name	Description	Ordering / Download Link	Ordering / Download Content
Hardware	.dp Interface Gen2	Interface to control XDPL8220 from PC	IF-BOARD.DP-GEN2	.dp Interface Gen2 x 1 USB cable x 1
Software	.dp Vision	Graphic User interface (GUI) for parameters configuration	.dp Vision	.dp Vision installer (*.exe)
	XDPL8220 Parameters csv file	XDPL8220 parameters configuration file	XDPL8220 project addon installer *Note: please download the latest version*	XDPL8220 parameters configuration file (*.csv) XDPL8220 CSV file description XDPL8220 Documentations (datasheet, application note, design guide)

Figure 15 shows the hardware setup needed between the PC and the program connector of the reference design for XDPL8220 parameters configuration.

Note:Please ensure the reference design board is not supplied with any voltage before connecting the programmable cable to reference design program connector.

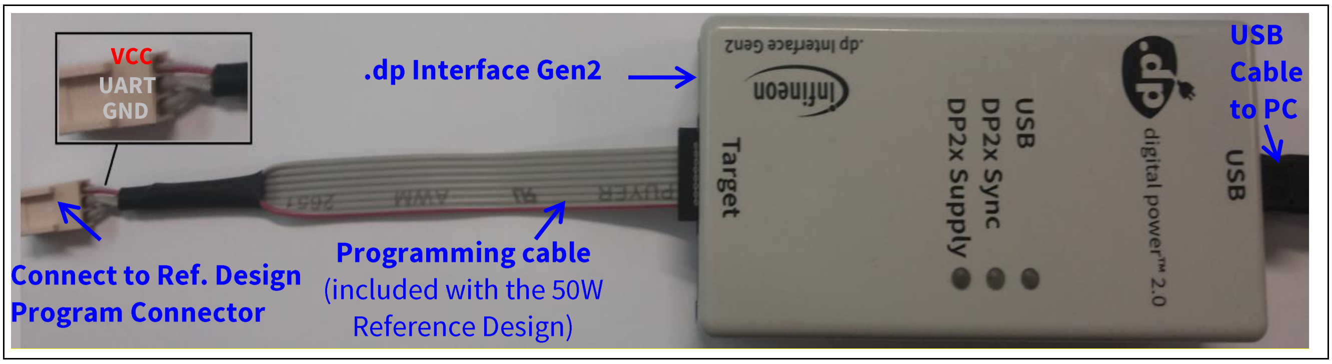


Figure 15 Hardware setup for XDPL8220 configuration

Please refer to the .dp Vision user manual for the detailed guide on the installation and how to use this graphic user interface (GUI) for parameters configuration. Alternatively, the following simple guide is also available for quick and easy reference.

After the tools installation (**Table 8**) and hardware connection for XDPL8220 configuration are done, please start the program by clicking the shortcut ".dp Vision" on the desktop.

Note: During the program startup, if the system shows there is a newer version of .dp Vision, please kindly follow the procedures and update it accordingly.

Then, please open the XDPL8220 parameters configuration file (*.csv) in the installation folder of the XDPL8220 project add-on. The default installation folder is at *C:\Users\Username\Infineon Technologies AG\.dp vision basic mode*

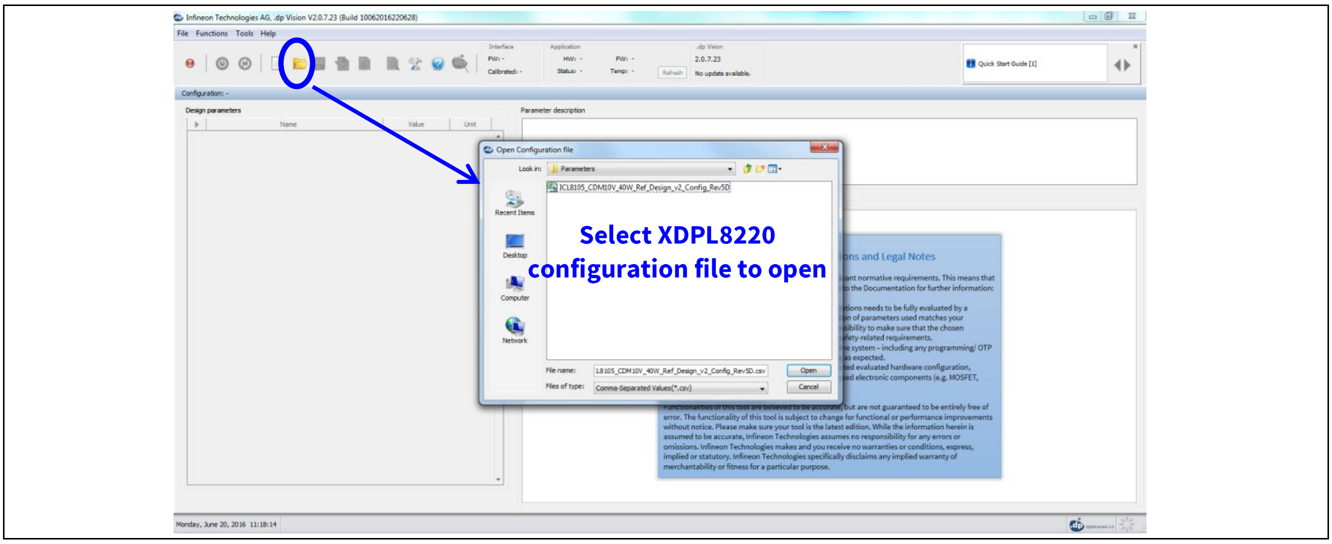


Figure 16 Opening XDPL8220 parameters configuration file (*.csv) in .dp Vision

After opening the parameter csv file, a list of XDPL8220 configurable parameters will then be shown (see the box on the left in **Figure 17**). If a parameter value is changed and there is no error detected, the changed value itself will turn blue, like the example of changing *I_out_full* parameter from 1500mA to 1000mA in **Figure 17**. Otherwise, if there is error detected (e.g. exceeded min/max value), the parameter value which causes the error will turn red and the message bar of .dp Vision (see the top right in **Figure 17**) will have an error message.

Note: User is not allowed to save, test or burn the configuration if there is an error detected.

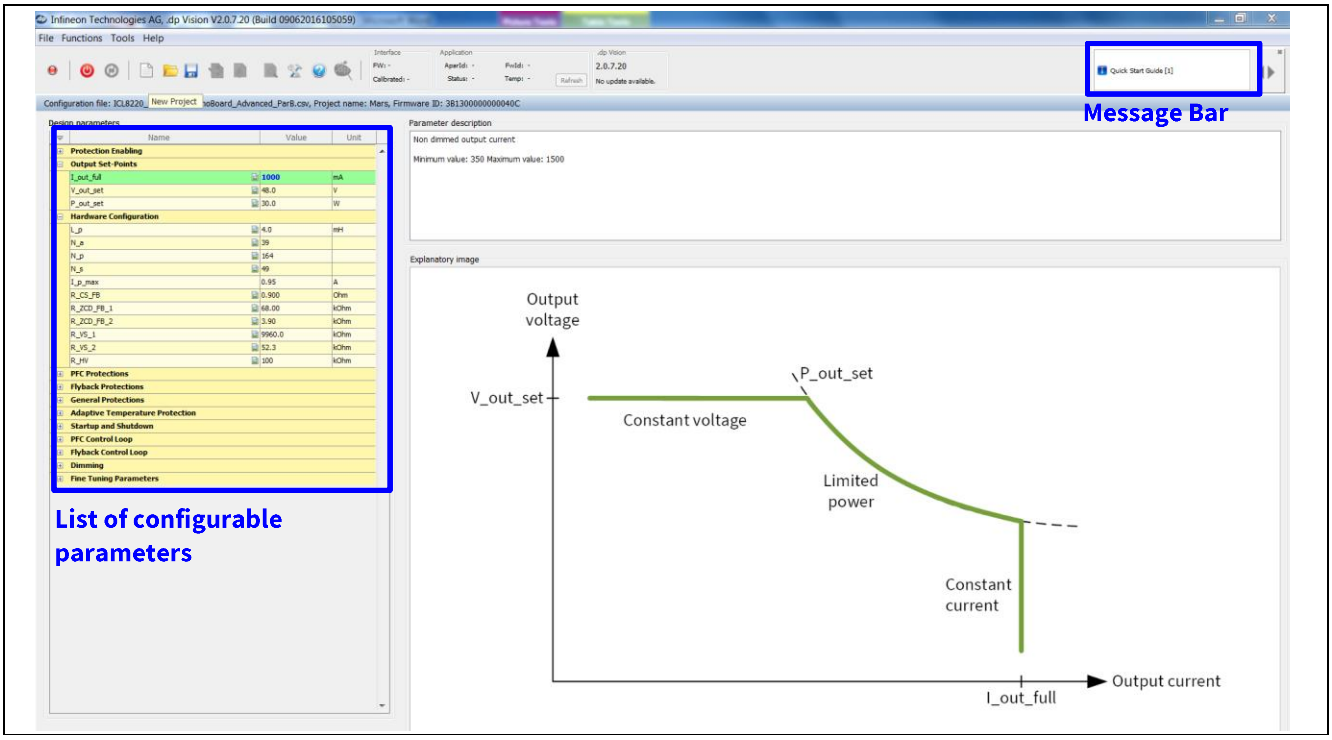


Figure 17 Changing parameter values of XDPL8220 configuration file in .dp Vision

There are 2 options available to configure the IC based on the parameter values in .dp Vision.

- Burn Configuration

  As the XDPL8220 chip on the 50W reference design PCB was already permanently burned with a first full set of parameters in its one time programmable (OTP) memory space, any parameter value change using this option is considered as parameter patching. The OTP memory space which is dedicated for patching or burning the parameter value change has a memory size of 274 words.

  Each time when the burn configuration function is executed, it will detect if there is parameter value difference between the saved configuration file and the target XDPL8220. If there is difference detected, each burn configuration will consume minimum 3 words depends on how many parameters need to be patched. However, the process will be aborted if it consumes more memory space than what is remaining in the target IC. As a result, the user will have to replace the target IC with a new XDPL8220 chip, in order to burn the configuration.

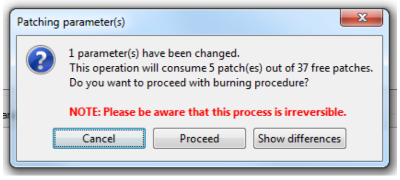
  Table 9 below shows the recommended procedures of using burn configuration function in .dp Vision to burn a first full set of new parameters or patch the parameter into the OTP memory.

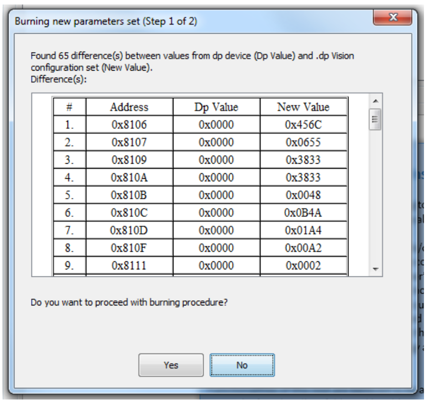
Table 9 Burn Configuration procedures

Step	Instruction
I	Open configuration file (see example in **Figure 16**)
II	If necessary, change any parameter value then press [File] >> [Save] or [File] >> [Save as], to

<table>
<tr><td></td><td>save the configuration file. Otherwise, proceed to step III</td></tr>
<tr><td>III</td><td>Ensure that the primary supply voltage (e.g. AC input) to the board is switched off or disconnected and the hardware connection for configuration is ok based on Figure 15</td></tr>
<tr><td>IV</td><td>Press to supply power and establish connection to the target XDPL8220. After this step, XDPL8220 will be in configuration mode and the device status should change to .</td></tr>
<tr><td>V</td><td>Press to burn configuration into target XDPL8220

After this step, you should see a pop-up window, which is similar to one of these below.



OR

</td></tr>
<tr><td>VI</td><td>Press “Proceed” or “Yes” to burn the configuration

After this step, a pop up window shows the burning was successful.</td></tr>
<tr><td>VII</td><td>Press “OK” on the pop up window then disconnect the programming cable from board connector Program and test the application, if needed.</td></tr>
</table>

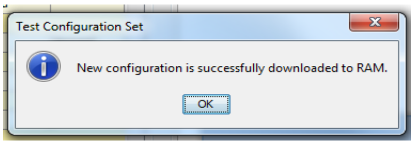
- Test Configuration

  This function will download the parameter values from the list in .dp Vision into the XDPL8220 RAM memory space and it will then be followed by an automatic IC startup for application testing with the new configuration.

  Unlike using the burn configuration, parameters configuration with this option is not permanent because the loaded RAM content will be lost once the IC supply voltage is turned off but the advantage of using this option is it does not consume OTP memory space, thus there is no limit on the amount of parameter value changes.

  Table 10 below shows the recommended procedures of using test configuration function in .dp Vision to load the new parameter values in the RAM and test the application with the new configuration.

Table 10 Test Configuration procedures

Step	Instruction
I	Open configuration file and change parameter value (see example in **Figure 16** and **Figure 17**)
II	Ensure that the primary supply voltage (e.g. AC input) to the board is switched off and the hardware connection for configuration is ok based on **Figure 15**
III	Press  to supply power and establish connection to the target XDPL8220. After this step, XDPL8220 will be in configuration mode and the device status  should change to .
IV	Ensure LED output is connected to the board and switch on AC input (e.g. 230Vac). After this step, the board does not startup because XDPL8220 is still in configuration mode.
V	Press  to test configuration with target XDPL8220 After this step, the IC will automatically start up with the new configuration and you should see a pop up window like below: 
VI	Press “OK” on the pop up window.
VII	Repeat the steps to test another configuration change. Otherwise, turn off the AC input and disconnect the programming cable from board connector Program.

Note: If there is any error encountered in between step I to VII, please kindly refer to the message bar of .dp Vision for the error message. For more details, please kindly refer to the .dp Vision user manual.

9 References

[1] XDPL8220 Datasheet

[2] XDPL8220 Design Guide

[3] .dp vision – Basic Mode User Manual

[4] XDPL8220 CSV File Description

[5] Power Management Selection guide:
http://www.infineon.com/powermanagement-selectionguide

Revision History

Major changes since the last revision

Page or Reference	Description of change
All	First release V1.0 2016-07-26
All	Update to V1.1 according to the board update V5.1. 2016-11-28

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