Brief Description

The ZSLS7031 is a primary-side controlled, peak-current-mode high-brightness LED flyback driver that supports both isolated and non-isolated designs with active power factor correction (PFC).

The device works at a constant frequency in discontinuous conduction mode to provide constant power to the output. It eliminates the need for an opto-coupler, TL431 shunt regulator, or any other type of secondary-side feedback device. It operates from a wide input voltage range of 85VAC to 265VAC.

The ZSLS7031 integrates over-current and over-voltage protection, as well as a thermal shutdown to halt the switching action in the event of abnormally high operating temperatures.

Benefits

- High efficiency
- Minimum bill of materials
- Small form-factor package
- No loop compensation required
- Isolated and non-isolated applications

Features

- Power factor PF > 0.95 depending on application
- Wide application input voltage range: 85V to 265VAC
- Internal over-temperature protection
- Output over-voltage protection (OVP)
- Output over-current protection (OCP) on primary side

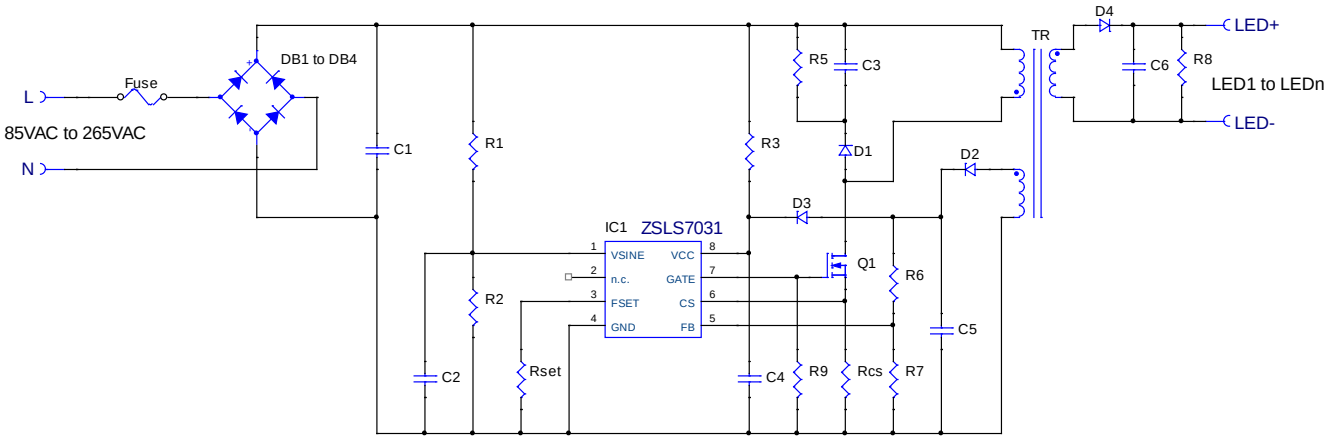
Available Support

- Evaluation Kit

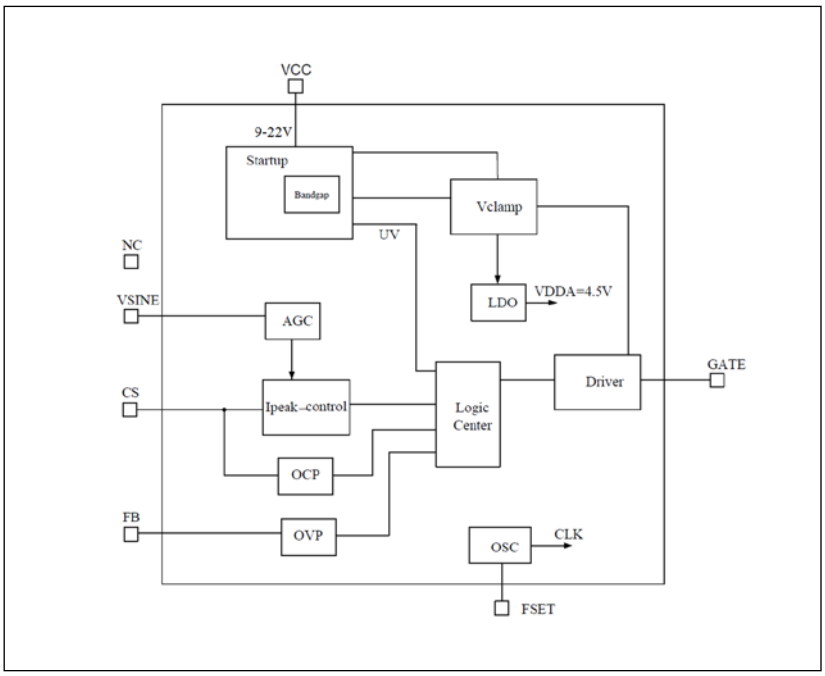
Physical Characteristics

- Operating temperature:-45°C to 105°C
- Maximum junction temperature: 150°C
- Package: MSOP-8, RoHS-compliant

ZSLS7031 Typical Isolated Application



Circuit Block Diagram



Typical Applications

- LED bulb lamps
- LED tube lamps
- General LED lighting

Ordering Information

Ordering Code	Description	Package
ZSLS7031ZI1R	ZSLS7031 Flyback LED Driver IC, MSOP-8	Tape on Reel
ZSLS7031KIT-D1	ZSLS7031PCB-D1 Evaluation Board, 5 ZSLS7031 ICs	Kit

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Contents

List of Figures

List of Tables

1 IC Characteristics

Stresses beyond those listed under “Absolute Maximum/Minimum Ratings” (section 1.1) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those recommended under “Operating Conditions” (section 1.2) is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

1.1 Absolute Maximum/Minimum Ratings

Table 1.1 Absolute Maximum Ratings

No.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.1.1	VCC to GND	V_{CC}		-0.3		24	V
1.1.2	VSINE, FSET, NC, CS, FB			-0.3		5.5	V
1.1.3	VCC input current	I_{CC}				10	mA
1.1.4	ESD performance		Human Body Model (HBM) based on MIL 883-H, Method 3015.8			±2	kV
1.1.5	Junction temperature	T_{jMAX}				150	°C
1.1.6	Storage temperature	T_{ST}		-65		150	°C

1.2 Operating Conditions

Table 1.2 Operating Conditions

No.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.2.1	Operating temperature	T_{AMB}		-45		105	°C
1.2.2	VCC voltage range	V_{CC}		9		22	V

1.3 Electrical Parameters

Except as noted, test conditions for the following specifications are VCC=16V, FB=0V, VSINE=2.5V, V_{CS}=0V, R_{SET}=300kΩ, and T_{AMB} = 25°C (typical).

Production testing of the chip is performed at 25°C unless otherwise stated. Functional operation of the chip and specified parameters at other temperatures are guaranteed by design, characterization, and process control.

Table 1.3 Electrical Parameters

No.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.3.1	VCC startup voltage threshold	V_{TH_S}	*VCC rising*	14.5	16	17.5	V
1.3.2	VCC under-voltage threshold	V_{TH_D}	*VCC falling*	7	8	9	V
1.3.3	GATE output voltage clamp value	$V_{GATEclp}$	*VCC rising to 22V*	15	17.5	19	V
1.3.4	Quiescent Supply Current	I_{CC}	Not switching		800		µA
1.3.5	Startup current	I_{ST}	VCC < Vth_s		60	80	µA
1.3.6	Primary peak current control threshold voltage	V_{CS}		0.49	0.5	0.51	V
1.3.7	Blanking time	t_{BLANK}			500	800	ns
1.3.8	Rise time	t_{RISE}	0V to 7V, 1nF capacitor from GATE to GND		100	120	ns
1.3.9	Fall time	t_{FALL}	V_{CC} = 16V, 1nF capacitor from GATE to GND		50	80	ns
1.3.10	OVP rising voltage threshold of FB	V_{OVP_H}		1.2	1.25	1.3	V
1.3.11	OVP falling voltage threshold of FB	V_{OVP_L}		0.95	1.0	1.05	V
1.3.12	Operating frequency	f	R_{SET} = 300kΩ	49	50	51	kHz
1.3.13	CS over-current protection delay	t_{OCP}	f = 50 kHz	500	600	750	µs
1.3.14	CS over-current protection threshold	V_{OCP_TH}	f = 50 kHz	0.65	0.70	0.75	V

1.4 Typical Performance Characteristics Graphs

Figure 1.1 V_{IN} vs. PF (Output: V_{OUT}=40V, I_{OUT}=0.45A)

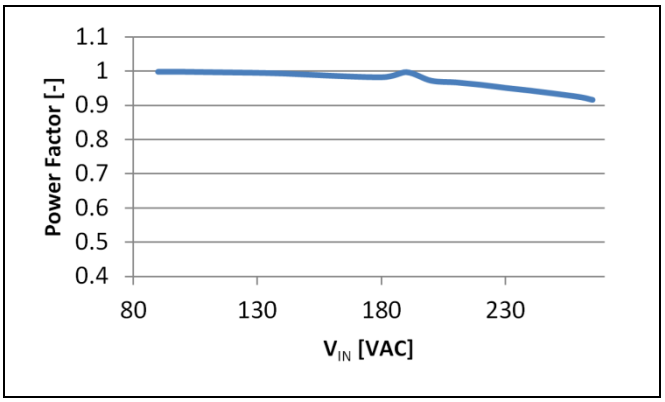


Figure 1.2 V_{IN} vs. I_{OUT} (Output: target I_{OUT}=0.45A, V_{OUT}=40V, without line compensation circuit)

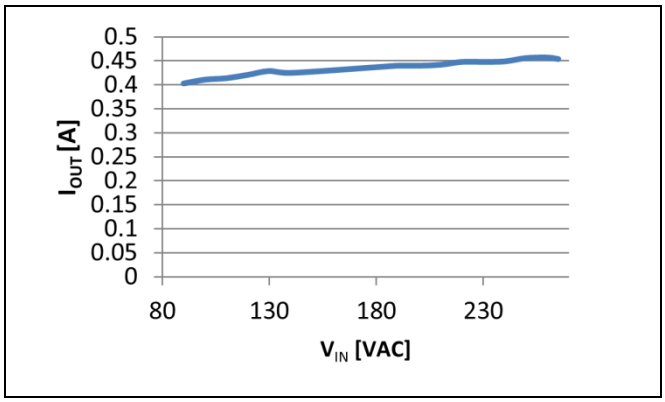


Figure 1.3 V_{IN} vs. Efficiency (Output: V_{OUT}=40V, I_{OUT}=0.45A)

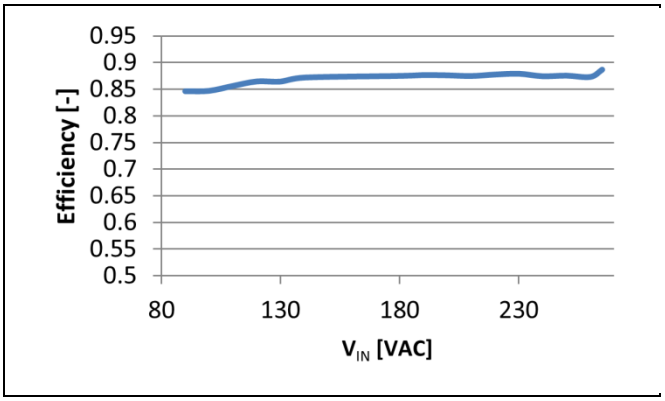


Figure 1.4 V_{IN} vs. I_{OUT} (Output: target I_{OUT}=0.45A, V_{OUT}=40V, with line compensation circuit)

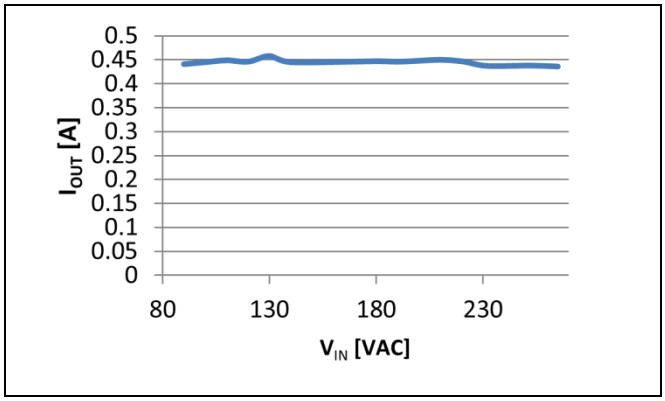


Figure 1.5 THD of V_{IN}=110V (Output: V_{OUT}=40V, I_{OUT}=0.45A)

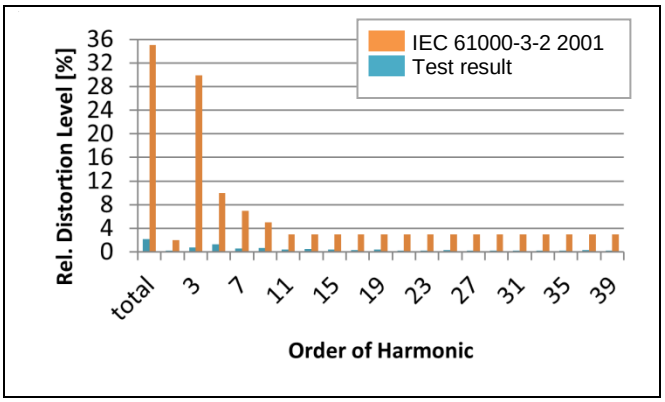
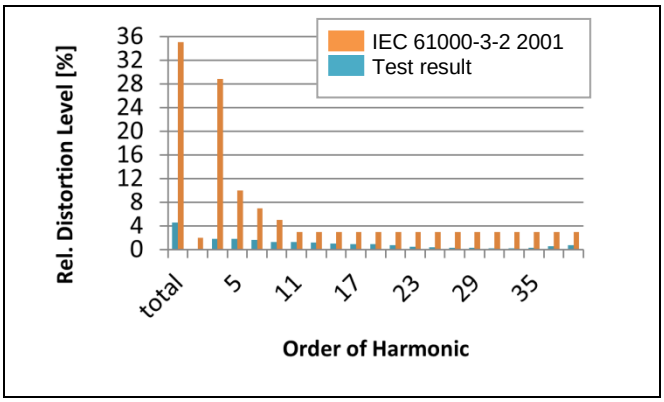


Figure 1.6 THD of V_{IN}=230V (Output: V_{OUT}=40V, I_{OUT}=0.45A)



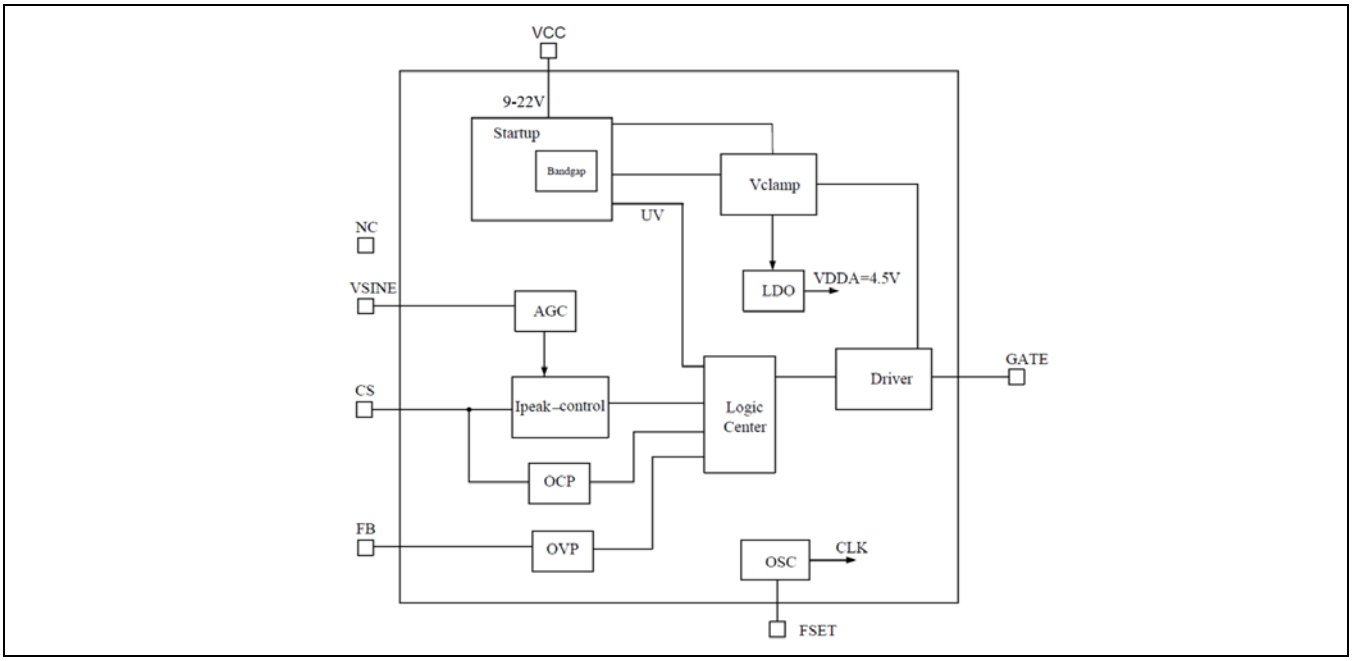
2 Circuit Description

Refer to the basic application circuit shown on page 2 for the external components referenced in the following sections.

2.1 ZSLS7031 Overview

The ZSLS7031 consists of the basic functional blocks shown in Figure 2.1.

Figure 2.1 ZSLS7031 Block Diagram



2.2 Startup Voltage

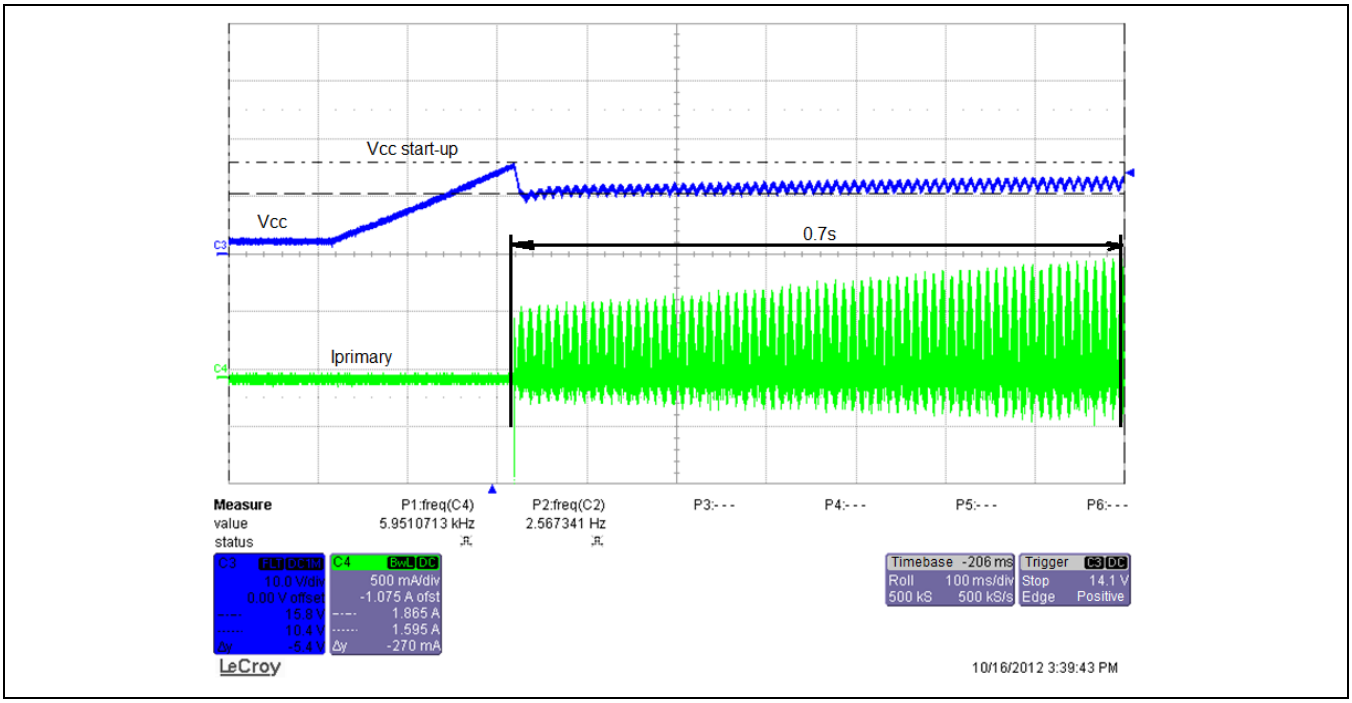
After power is applied to the circuit, R3 provides a trickle current to allow C4 to begin charging. The ZSLS7031 starts functioning when the voltage across C4 reaches the startup threshold V_{TH_S}, which is approximately 16.5V (see specification 1.3.1).

The value of R3 and C4 can be determined by the input voltage. Choosing a larger value of R3 increases the startup time but reduces the losses after the circuit is running. A low ESR capacitor of 2.2µF rated for 25V is recommended for C4.

2.3 Soft Start Control

When the ZSLS7031 is initially powered up, the internal automatic gain control (AGC) output is at the minimum value, so the peak CS threshold is initially much less than 0.5V. The AGC steps up cycle-by-cycle until the CS threshold at the peak of the input sine wave is equal to 0.5V. With this technique, it will take several cycles of the AC waveform for the final value of current to be attained, as shown in Figure 2.2.

Figure 2.2 ZSLS7031 Soft Start



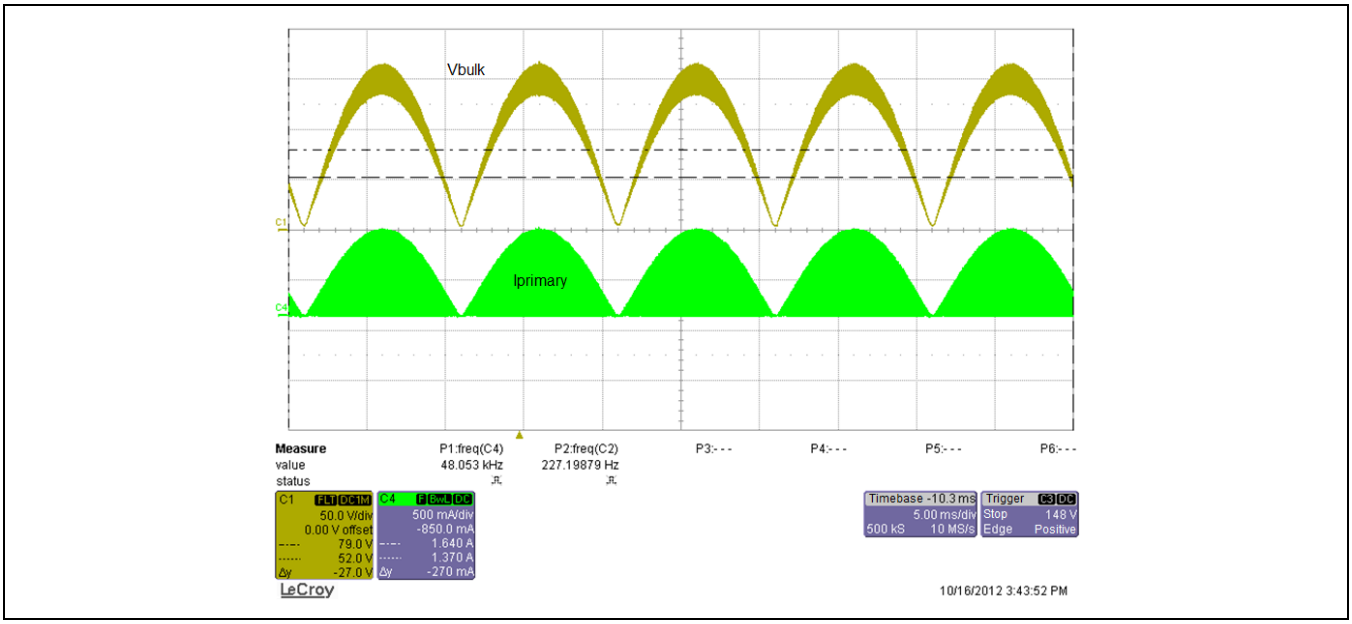
2.4 Gate Output Voltage Clamp

ZSLS7031 provides the voltage clamp for the GATE output. When the voltage at VCC is smaller than the $V_{GATEclp}$ threshold (see specification 1.3.3), the output high voltage of the GATE output is approximately VCC. When the voltage of VCC is greater than the $V_{GATEclp}$ threshold, the output high voltage of GATE is limited to the $V_{GATEclp}$ threshold.

2.5 V_{SINE} Detection Network and Active PFC

The voltage V_{SINE} at the VSINE pin is used to control the waveform of the input current to ensure that it follows the input voltage waveform, V_{BULK}, to achieve a high power factor (PF) and low total harmonic distortion (THD) performance, as demonstrated in Figure 2.3.

Figure 2.3 Active PFC



V_{SINE} is used to detect the input voltage that controls the peak current waveform in the primary inductor. An integrated AGC ensures that the peak current of the inductor remains constant with changing input voltage. This allows the ZSLS7031 to actively correct the power factor while maintaining a constant power output during operation. The resistor network connected to VSINE should be computed so that the peak input voltage condition corresponds to ~2.4VDC. For example, for 265VAC, the peak voltage is 374.7V. At 374.7V input, the output of the network should be 2.4V; therefore values of R1=1.86M and R2 = 12k are appropriate. Precision resistors of 1% tolerance or better must be used. A small capacitor, C2, is used to filter high frequency noise that may couple to the VSINE pin.

2.6 Operating Frequency

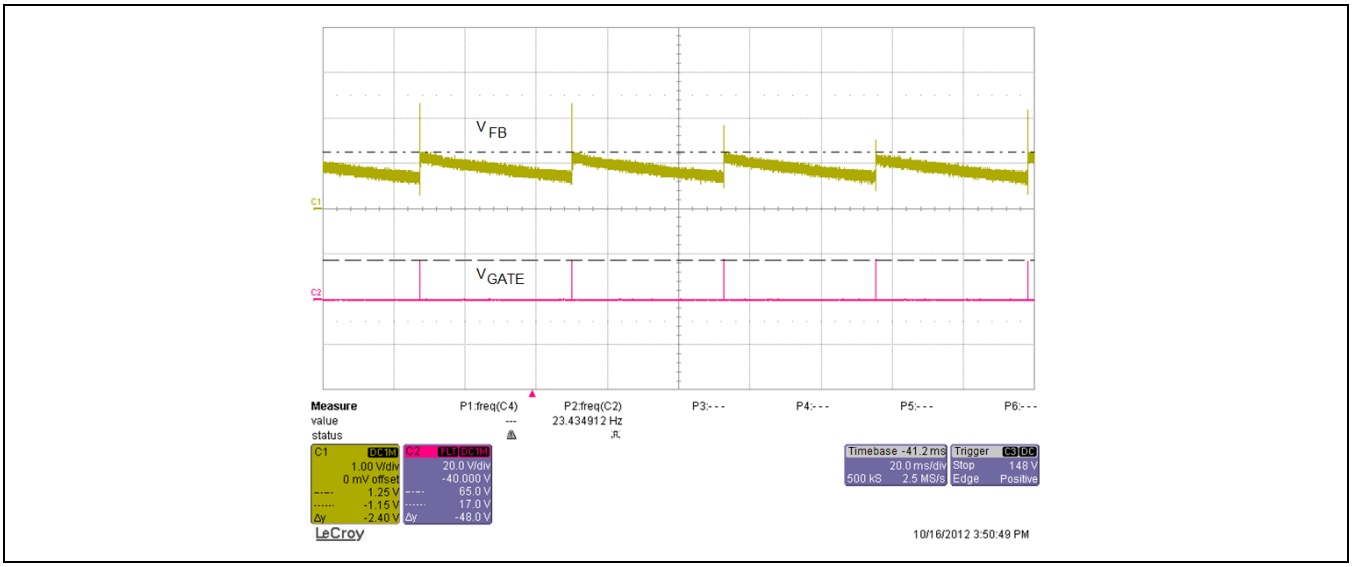
The operating frequency is set by connecting a resistor between the FSET pin and ground. The relationship between the frequency and resistance is given in equation (1).

$$f[kHz] = \frac{15 \times 10^3}{R_{SET}[k\Omega]} \quad (1)$$

2.7 Output Over-Voltage Protection

Over-voltage protection of the output (OVP) is achieved by connecting a resistor network from the auxiliary winding to the FB pin. By sensing the voltage of the auxiliary winding, which is proportional to the output voltage, the ZSLS7031 detects when there is an open circuit condition on the secondary side and consequently reduces the switching action to a minimum burst mode. The threshold voltage for the FB pin is typically 1.25V. Care must be taken that the high ripple current bursts do not lead to an overshoot of the output capacitor's rated voltage. This can be accomplished by a Zener diode in parallel, rated slightly lower than the output capacitor's nominal voltage or a reasonable discharge resistor. The ZSLS7031 will recover to normal operation when the open-circuit condition has been corrected.

Figure 2.4 Output Over-Voltage Protection



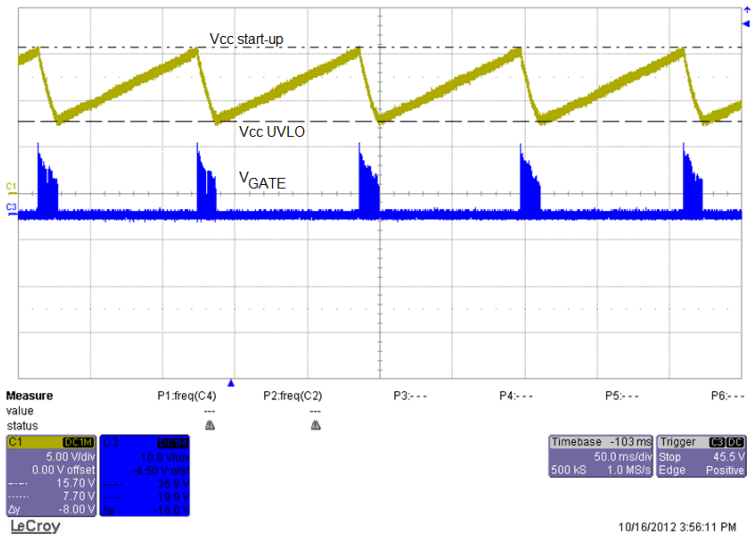
2.8 Output Over-Current Protection (OCP)

If the output of the circuit is suddenly shorted, the resulting over-current condition is detected on the primary side and the converter will shut off for 30 cycles when the over-current comparator has switched after time t_{blank} (see specification 1.3.7) has elapsed.

2.9 Under-Voltage Lock Out (UVLO)

If the input voltage on the VCC pin falls below the under-voltage threshold V_{TH_D} (see specification 1.3.2), the under voltage lock out (UVLO) will be triggered. In this event, the device will stop operating until the VCC voltage rises above the startup threshold V_{TH_S} (see specification 1.3.1), at which point the device will start again.

Figure 2.5 Under-Voltage Lock Out



3 Application Circuit Design

3.1 Typical Applications

The typical application circuits shown on the following pages are designed for a wide input voltage range 85VAC to 265VAC.

3.2 Line Regulation Compensation Design

The output power of the ZSLS7031 varies slightly with input voltage due to the small delay associated with the current-sense control loop. At high input voltages, the slope of the input current is quite steep, and therefore it will overshoot the target value by more than it would at low input voltage conditions. Therefore, under wide input voltage conditions, and without additional compensation, the output power varies over the full input voltage range, 85VAC to 265VAC, by about +/-5%. To further improve the line regulation, a simple compensation circuit can be added as shown in Figure 3.1 and Figure 3.2 with components R4, R12, R13, R14, R15, and C9.

3.3 Transformer Design

The transformer design is described in a separate application note *ZSLS7031_AN_TransformerDesign.pdf* supported by a calculation spreadsheet.

Figure 3.1 Typical Isolated Application Circuit

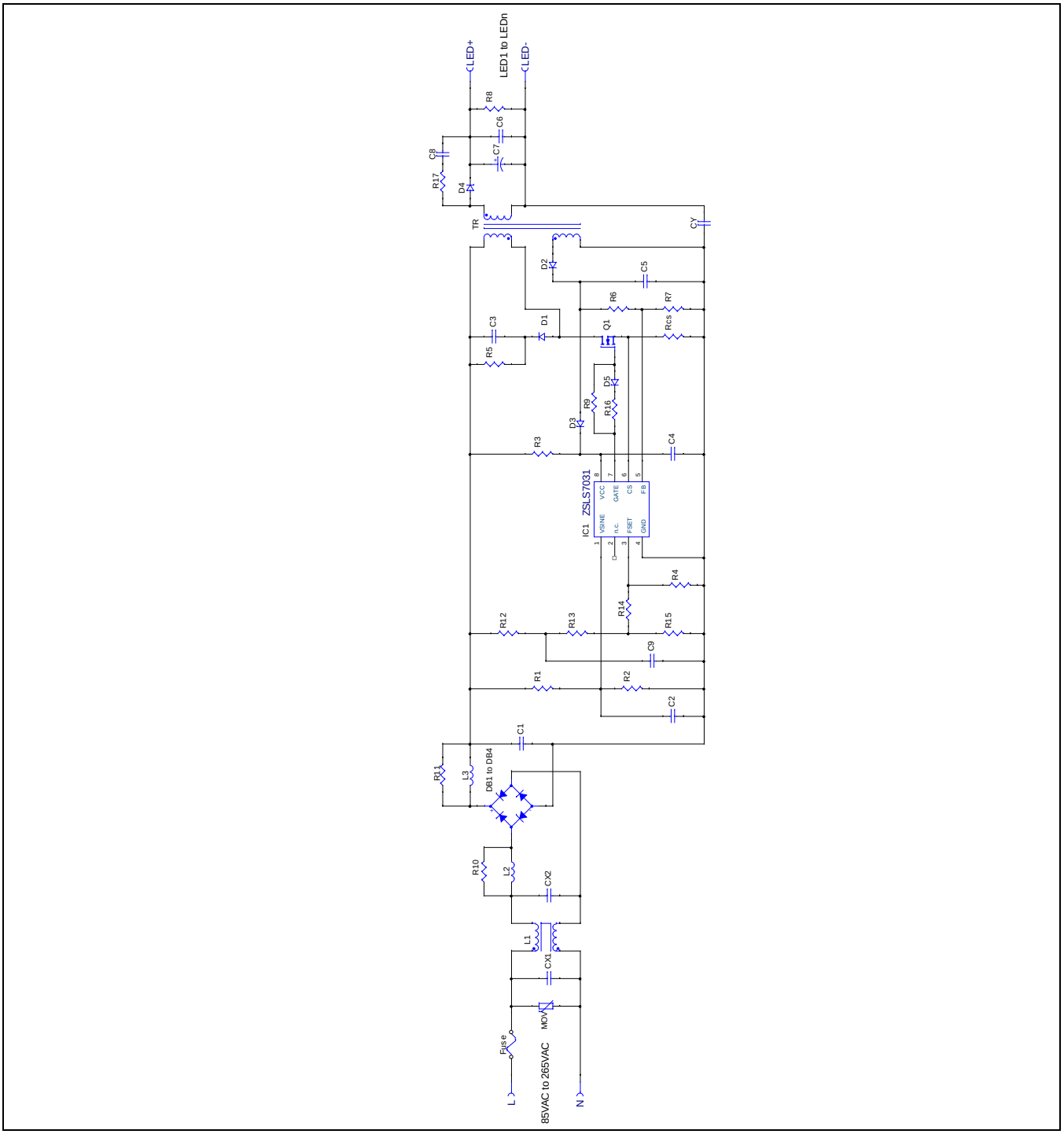
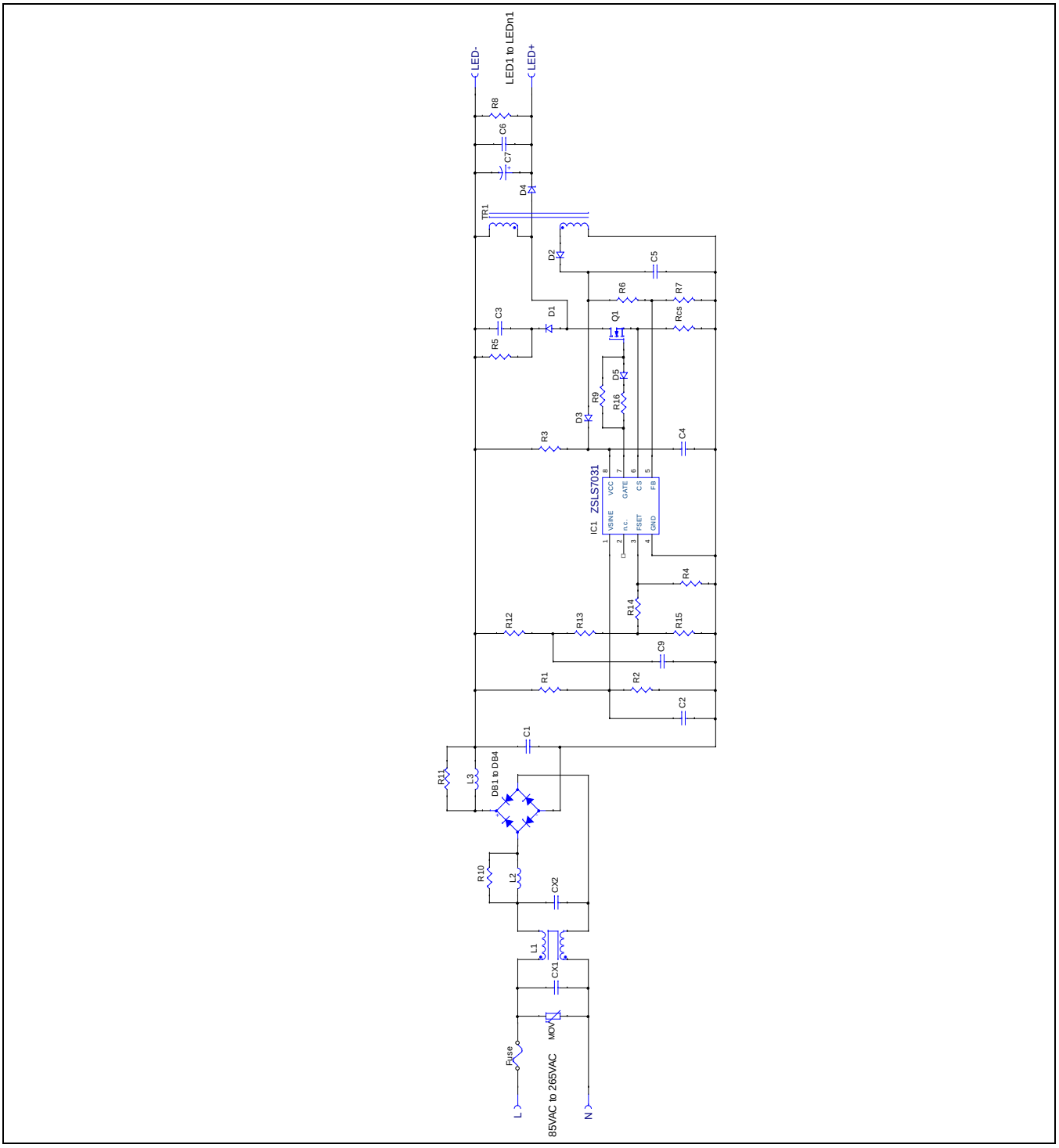


Figure 3.2 Typical Non-Isolated Application Circuit



3.4 Printed Circuit Board (PCB) Design Considerations

The guidelines in this section are strongly recommended when laying out application circuits. As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If the layout is not well-designed, the regulator could show instability as well as EMI problems. For additional information, refer to the IDT application note *PCB Layout Design Guidelines for LED Driver Circuits* available at *www.IDT.com*.

Components such as R4, R_{CS}, R6, R7, R2, C2, C5, etc., that are connected to the ZSLS7031 as well as the bypass capacitors should be mounted as close to the ZSLS7031 as possible.

Switching signal traces should be kept as short as possible and not be routed in parallel to one another so as to prevent coupling. Power ground and signal ground should be separated, and the traces of power ground should be kept as short as possible.

Figure 3.3 shows, as an example, the layout of the ZSLS7031 Demonstration Board comprising a 20W isolated flyback design on a 28mm x 71mm PCB area. Note: This board's component labels are different from those in previous schematics and equations. Figure 3.4 shows the corresponding circuit diagram.

Figure 3.3 ZSLS7031PCB-D1v1 Demonstration Board Layout

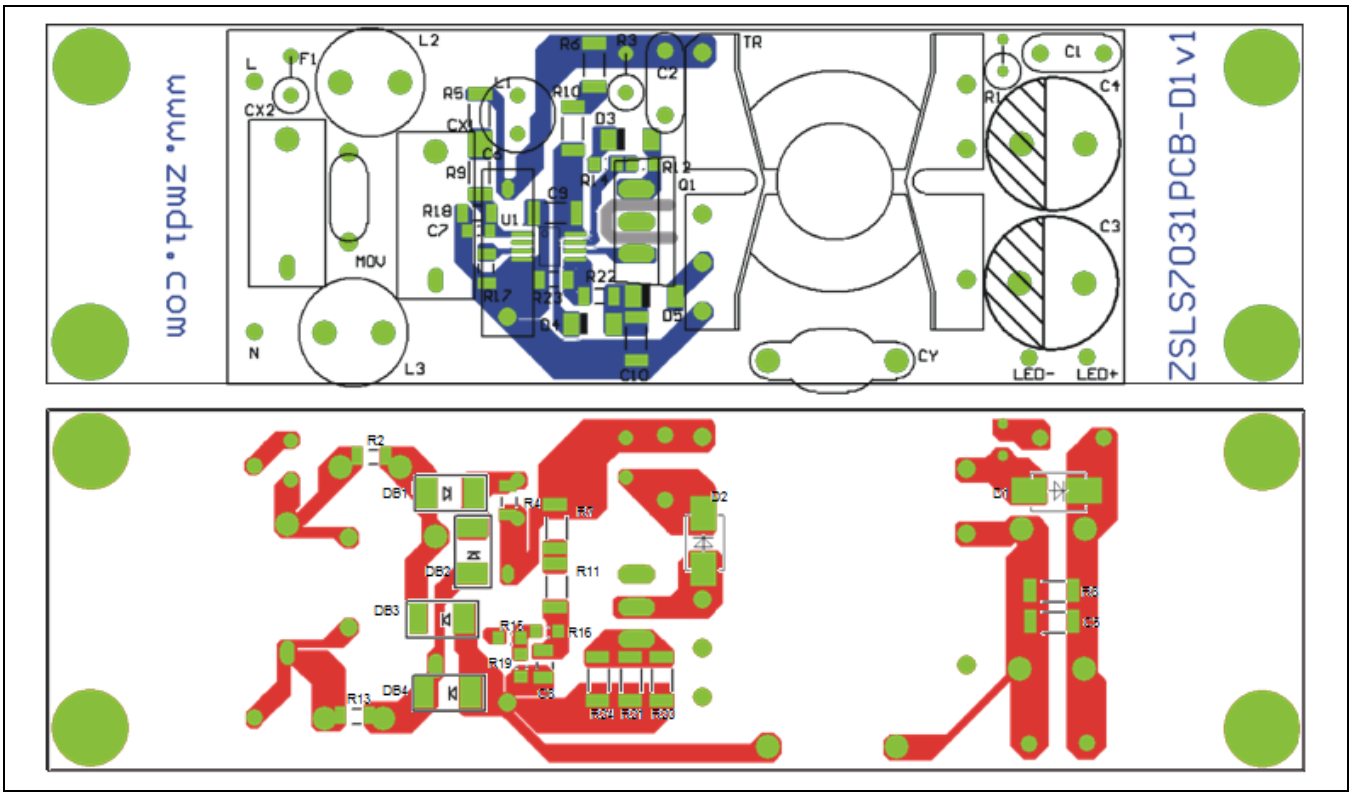
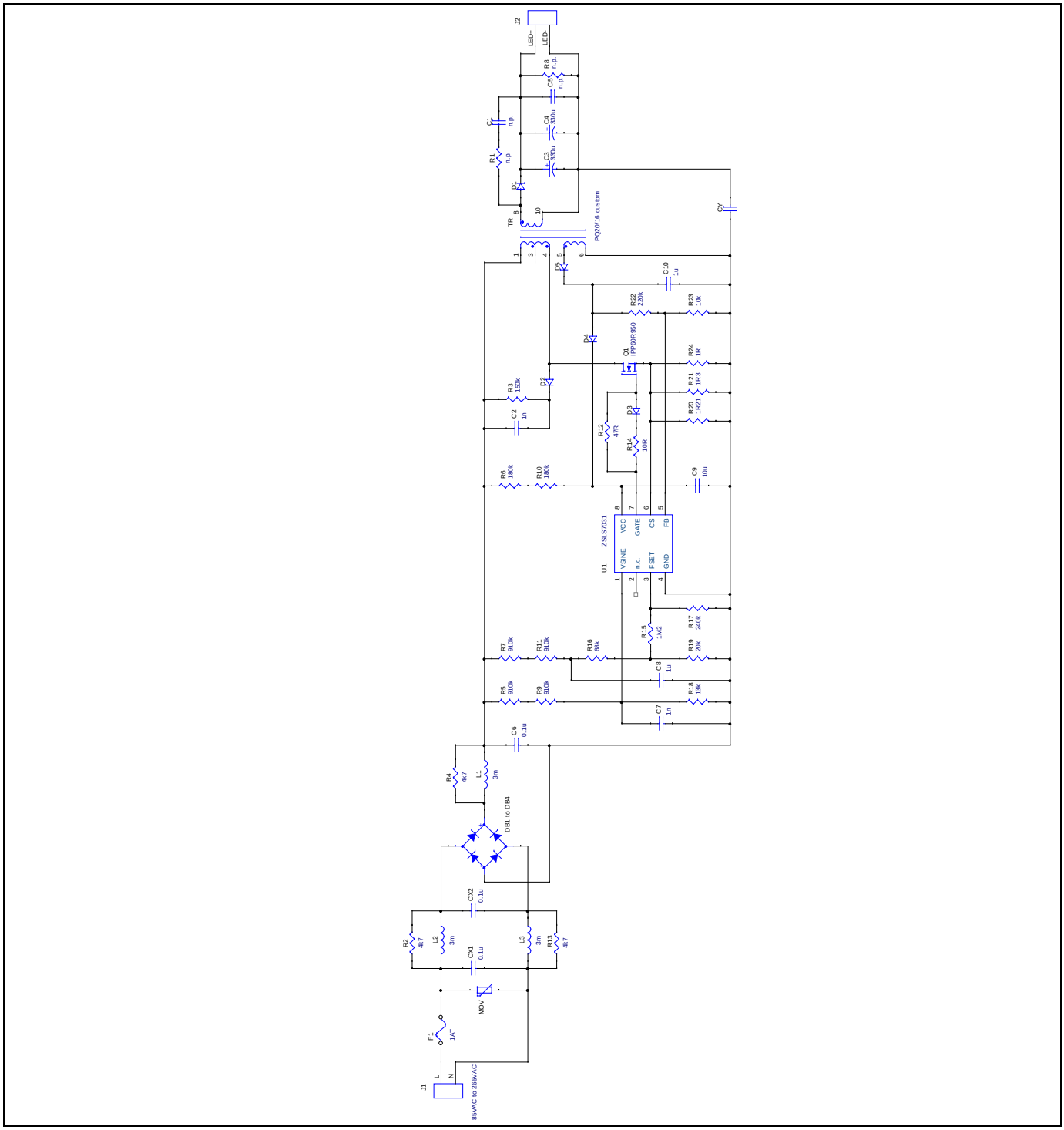


Figure 3.4 ZSLS7031PCB-D1v1 Demonstration Board Circuit



4 ESD Protection

All pins have an ESD protection of ≥ ±2000V according to the Human Body Model (HBM). The ESD test follows the Human Body Model based on MIL 883-H, Method 3015.8.

5 Pin Configuration and Package

Figure 5.1 ZSLS7031 Pin Assignments Top View

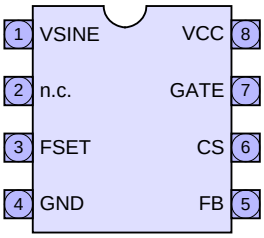
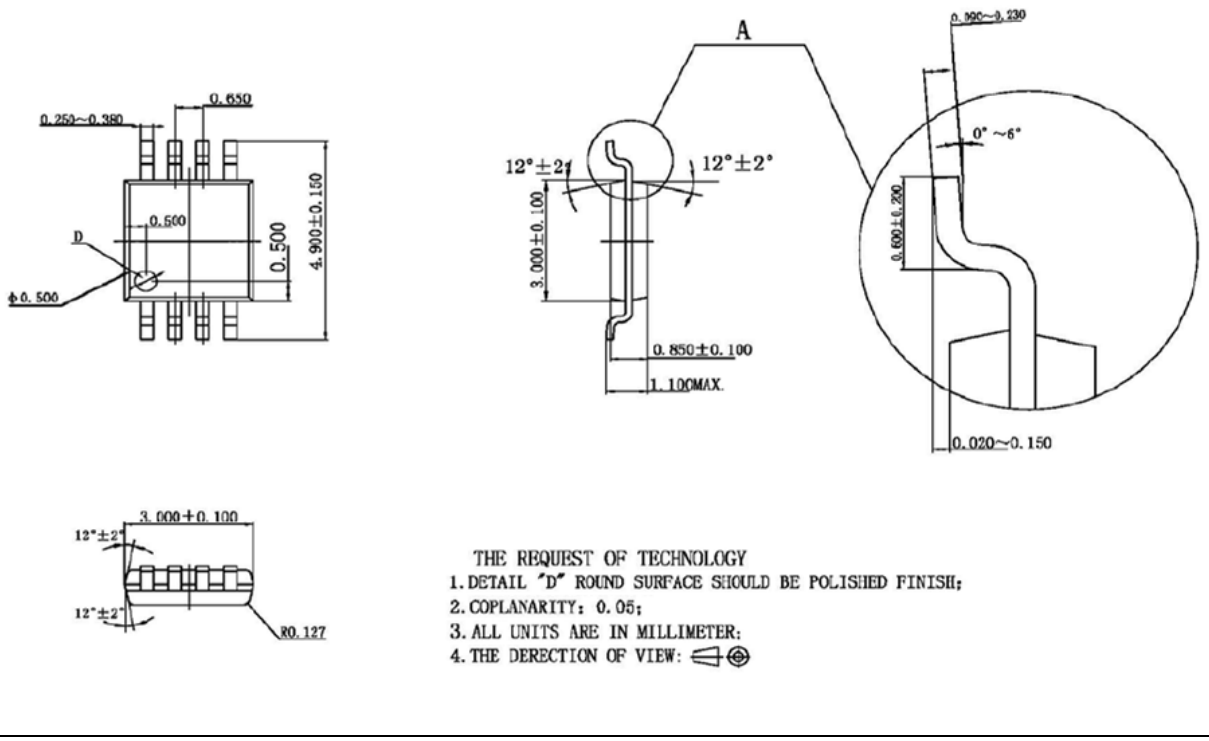


Table 5.1 Pin Description MSOP-8

Pin Name	NO.	Description
VSINE	**1**	Line voltage sense input required for PFC.
NC	**2**	Not connected. Leave floating in the application.
FSET	**3**	Connect a resistor from this pin to GND to set the operating frequency.
GND	**4**	Ground. Common potential to all internal circuitry.
FB	**5**	Auxiliary winding voltage sensing pin for OVP.
CS	**6**	Primary winding peak current sensing input.
GATE	**7**	External power NMOS gate driving output.
VCC	**8**	Internal circuit power supply input.

Figure 5.2 MSOP-8 Package Dimensions



6 Glossary

Term	Description
AGC	Automatic Gain Control
LDO	Low Dropout (Regulator)
OCP	Over-Current Protection
OVP	Over-Voltage Protection
PF	Power Factor
PFC	Power Factor Correction
THD	Total Harmonic Distortion
UVLO	Under-Voltage Lock Out

7 Ordering Information

Ordering Code	Description	Package
ZSLS7031ZI1R	ZSLS7031 Flyback LED Driver IC, MSOP-8	Tape on Reel
ZSLS7031KIT-D1	ZSLS7031PCB-D1 Evaluation Board, 5 ZSLS7031 ICs	Kit

8 Document Revision History

Revision	Date	Description
1.00	May 7, 2013	First release.
	January 26, 2016	Changed to IDT branding.

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