Design Example Report

Title	***2.5 W, Universal Input, Non-Isolated Flyback Converter Using LinkSwitch™-XT2 LNK3604D***
Specification	85 VAC – 265 VAC Input, 5.0 V, 500 mA Output
Application	Embedded Power Supply
Author	Applications Engineering Department
Document Number	DER-578
Date	December 7, 2016
Revision	1.0

Summary and Features

- Lowest component count for a non-isolated flyback solution
- Output voltage regulation, ±5%
- Programmable current limit for clampless design
- Reduced dissipation during output short circuit fault
- <10 mW no-load input power at 230 VAC
- >75% Efficiency at full load condition
- >6 dB conducted EMI margin

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a non-isolated flyback converter designed to provide a nominal output voltage of 5 V at 500 mA load from a wide input voltage range of 85 VAC to 265 VAC. This adapter utilizes the LNK3604D from the LinkSwitch™-XT2 family of devices.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

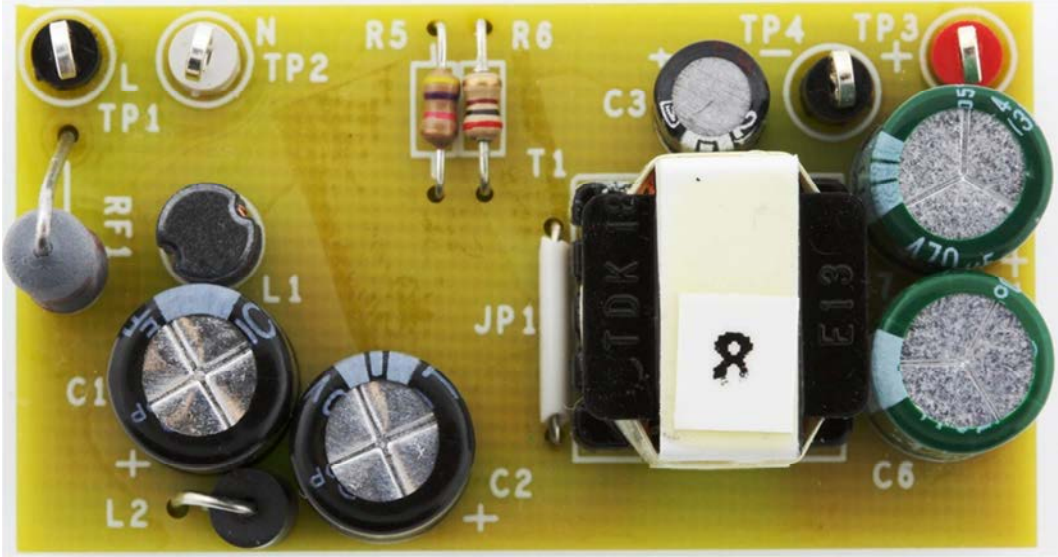

Figure 1 – Populated Circuit Board, Upper View.

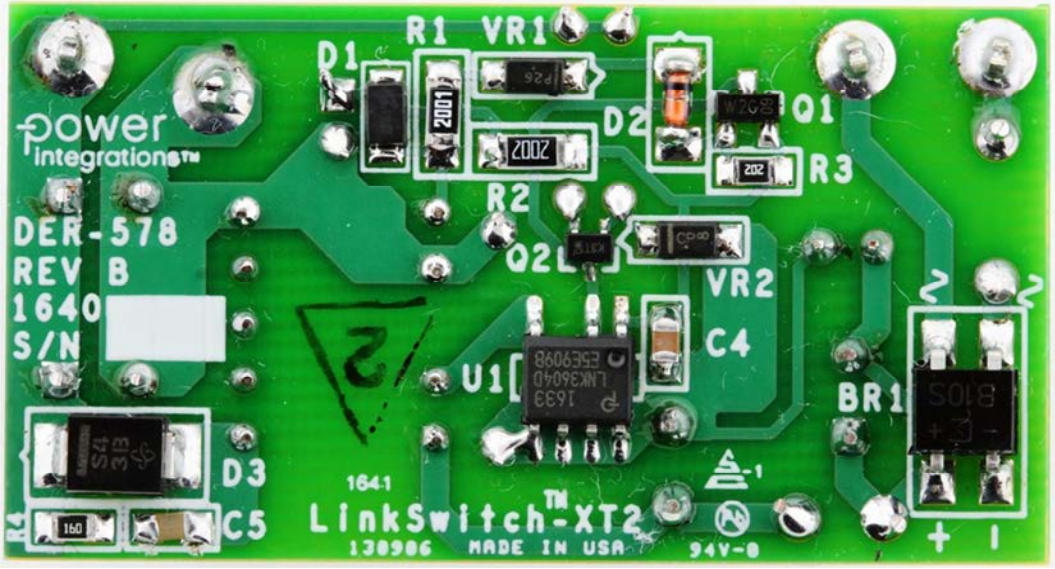

Figure 2 – Populated Circuit Board, Lower View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				10	mW	Measured at 230 VAC Line.
Output						
Output Voltage	V_{OUT}	4.75	5	5.25	V	
Output Ripple Voltage	V_{RIPPLE}			200	mV	Output Ripple Voltage Measured at the Board Output Terminals.
Rated Output Power	P_{OUT}		2.5		W	
Efficiency						
Full Load			75		%	Measured at Output Terminal.
Environmental						
Conducted EMI			CISPR22B / EN55022B Load floating			With 6 dB Margin using Resistive Load
Line Surge Differential mode (L/N)				1	kV	Differential: 2 Ω
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure.

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3 Schematic

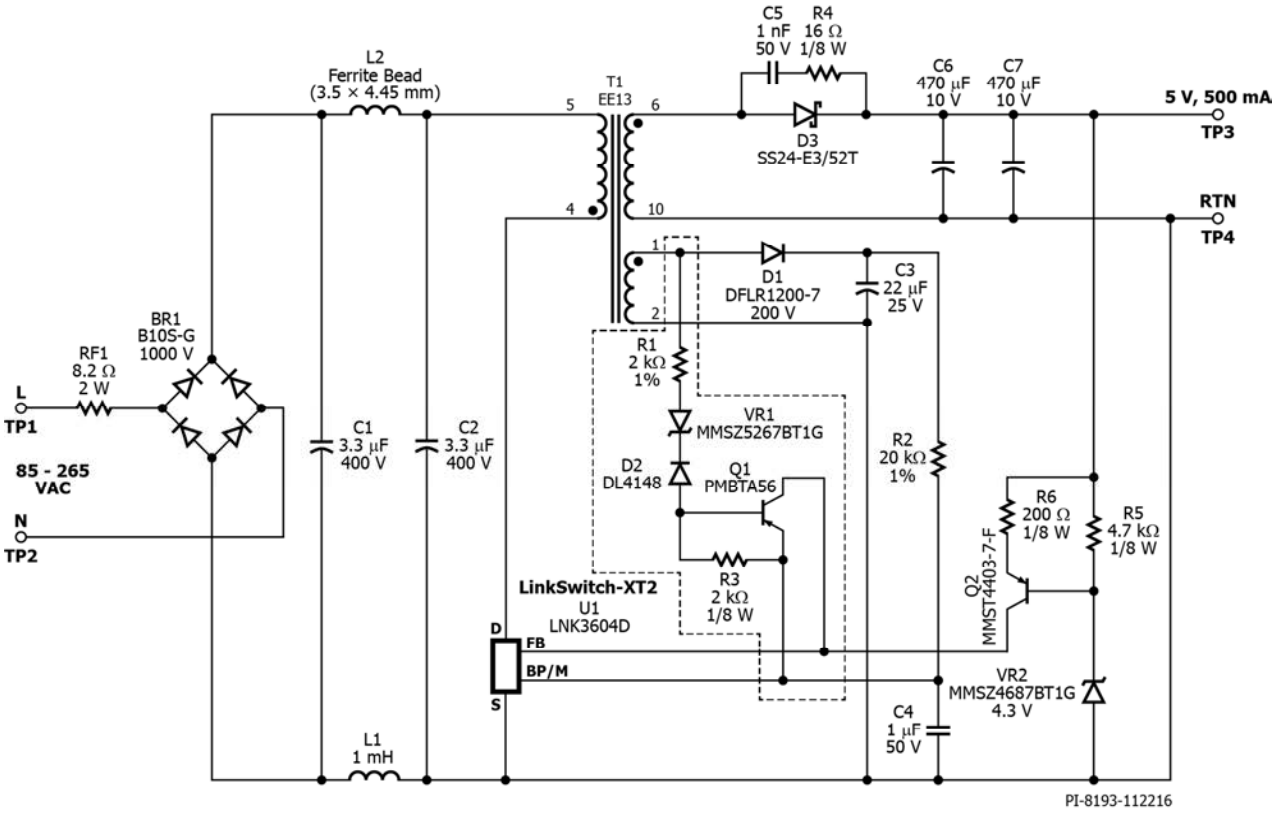

Figure 3 – Schematic.

NOTE:

Populate when line overvoltage protection is needed.

4 Circuit Description

4.1 *Input Rectifier and Filter*

Fusible resistor RF1 provides protection against catastrophic failure of components on the primary side. Bridge rectifier BR1 rectifies the input supply and charges the bulk storage capacitor. Capacitor C1 and C2 provide filtering of the rectified AC input and together with L1 and L2 form a π (pi) filter to attenuate differential mode EMI.

4.2 *LinkSwitch-XT2 Primary Side Circuit Operation*

The LNK3604D device integrates the oscillator, controller, start-up and other protection circuitry as well as the high-voltage power MOSFET on a single monolithic IC. Suffix D indicates the SO-8 package.

The LNK3604D IC operates at a fixed current limit (I_{LIMIT}). Every enabled switching cycle the primary current ramps to this current limit level. Output regulation is maintained by skipping switching cycles (ON/OFF control). The internal controller determines if the next switching cycle should be enabled or disabled (skipped) based on the current flowing into the FEEDBACK (FB) pin. If a current less than 49 µA flows into the FB pin when the oscillator's (internal) clock signal occurs, power MOSFET switching is enabled for that particular switching cycle and the power MOSFET turns on. If the current is greater than 49 µA then the power MOSFET is disabled for the current switching cycle.

The switching cycle terminates when the current through the power MOSFET reaches I_{LIMIT}, or the on-time of the power MOSFET reaches the maximum duty cycle (DC_{MAX}) limit.

At full load, few switching cycles will be skipped (disabled), resulting in a high effective switching frequency. As the load reduces, more switching cycles are skipped, which reduces the effective switching frequency. At no-load, most switching cycles are skipped, which is what makes the no-load power consumption of supplies designed around the LinkSwitch-XT2 family so low, since switching losses are the dominant loss mechanism at light loading. Additionally, since the amount of energy per switching cycle is fixed by I_{LIMIT}, the skipping of switching cycles gives the supply a flat efficiency characteristic over the load range.

No primary clamp is required as the low value and tight tolerance of the LNK3604D internal current limit allows the primary winding capacitance of the transformer and drain-source capacitance of the power MOSFET in the LNK3604D to provide adequate clamping of the leakage inductance drain voltage spike.

4.3 *Primary Bias Circuit*

LinkSwitch-XT2 devices do not require an external bias supply for operation and can be configured to be self-powered. However providing the operating current for the device

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into the BYPASS (BP) pin externally dramatically reduces no load input power. In this design the bias winding (pins 1 and 2 on the transformer) output is rectified and filtered by D1 and C3. The value of C3 was selected to give an acceptable minimum voltage during no-load when the supply is operating at low switching frequencies. Resistor R2 is selected such that approximately 250 μA flows into the BP pin.

4.4 *Output Rectification*

Diode D3 rectifies the output from transformer T1. This rectifier is a low drop Schottky diode. Output filtering was provided by capacitor C6 and C7 which is a super low ESR type to reduce output ripple and remove the need for a LC second stage switching noise filter.

4.5 *Output Feedback*

The output voltage (CV portion) is regulated by the transistor Q2 and Zener diode VR2. The combined voltage drop across VR2, emitter to base voltage drop of transistor Q2 ($V_{EB(Q2)}$) and R8 determines the output voltage. When the output voltage exceeds this level, current will flow through transistor Q2. As the current increases, the current fed into the FB pin of U1 increases until the turnoff threshold current (~49 μA) is reached, disabling further switching cycles of U1. Just before the start of each cycle, the LinkSwitch-XT2 controller checks this FB pin current, to determine if the next switching cycle is enabled or disabled.

Resistor R5 provides ≈150 μA through VR2 to bias the Zener diode to its test current. The Zener diode used here is a low test current Zener diode which needs only 50 μA to conduct. 5% tolerance Zener diode is used here as its test current (50 μA) is much lower than the 1%-2% tolerance Zener diode (1 mA). This will provide <10 mW no-load input power. Resistor R8 is used to limit the current into FB pin to less than 1.2 mA for protection.

If <10 mW no-load input power is not required, higher accuracy Zener diode can be used here. Moreover, the resistor divided feedback can also be used here. Please refer the data sheet design example for the resistor divided feedback.

5 PCB Layout

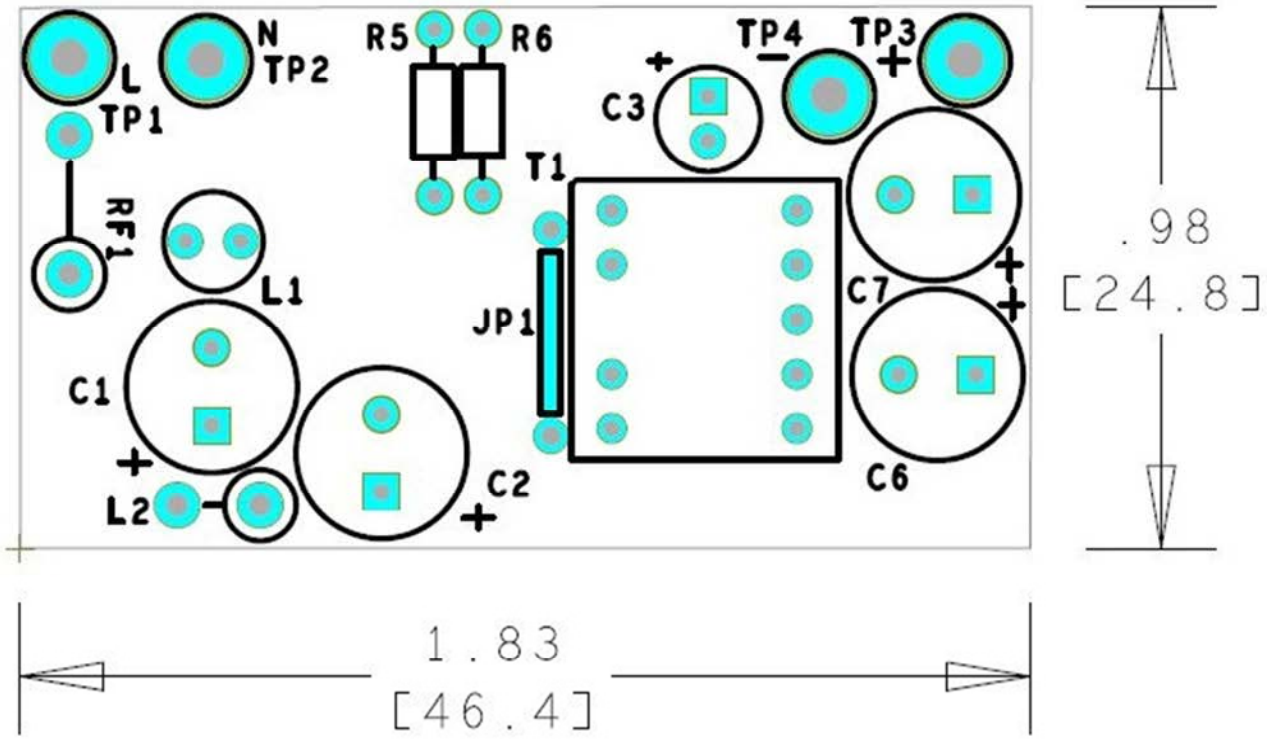

Figure 4 – PCB Upper Side.

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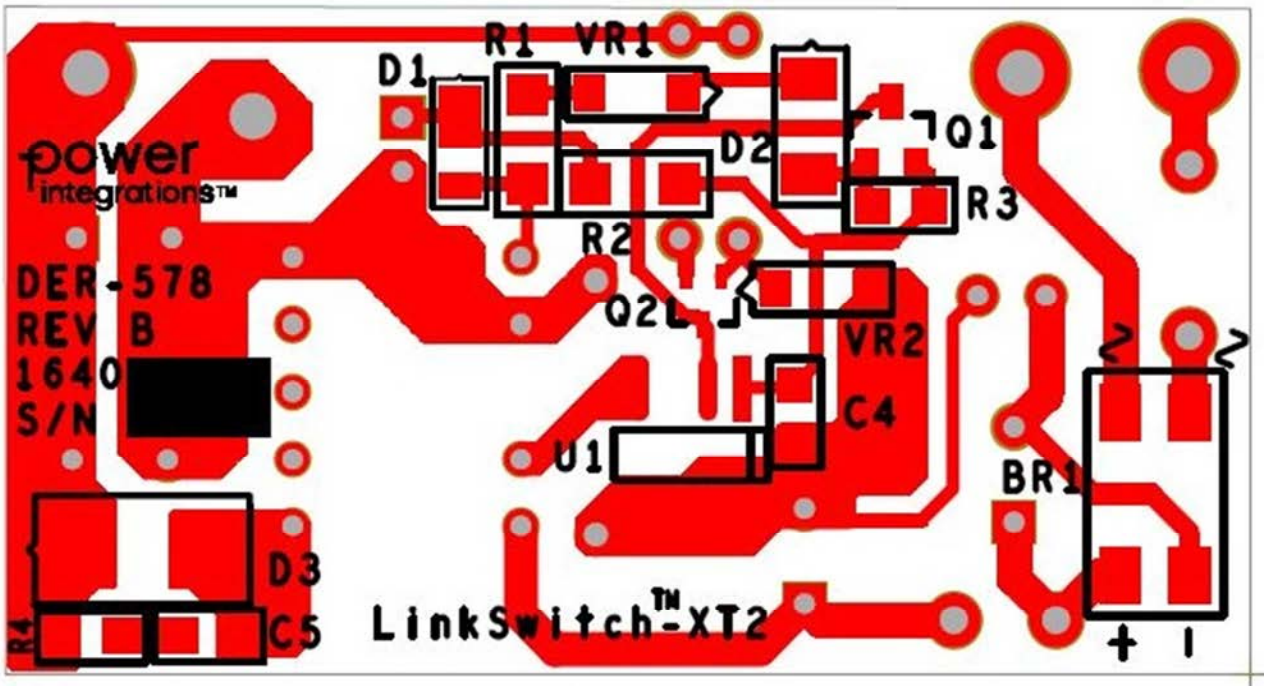

Figure 5 – PCB Lower Side.

6 Bill of Materials

Item	Qty	Ref	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	2	C1 C2	3.3 µF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G3R3MK0811MLL3	Taicon
3	1	C3	22 µF, 25 V, Electrolytic, 20 %, Gen. Purpose, (5 x 7 mm)	EEA-GA1E220	Panasonic
4	1	C4	1 µF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
5	1	C5	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX
6	2	C6 C7	470 µF, 10 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE100ELL471MHB5D	Nippon Chemi-Con
7	1	D1	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
8	1	D2	75 V, 0.15 A, Fast Switching, 4 ns, MELF, SOD80C	DL4148-TP	Micro Commercial
9	1	D3	40 V, 2 A, Schottky, SMD, DO-214AA	SS24-E3/52T	Vishay
10	1	JP1	Wire Jumper, Insulated, TFE, #22 AWG, 0.5 in	C2004-12-02	Alpha
11	1	L1	1 mH, 0.15 A, Ferrite Core	SBCP-47HY102B	Tokin
12	1	L2	3.5 mm x 4.45 mm, 56 Ω at 100 MHz, #22 AWG hole, Ferrite Bead	2761001112	Fair-Rite
13	1	Q1	PNP, Small Signal BJT, 80 V, 0.5 A, SOT-23	PMBTA56 T/R	Philips
14	1	Q2	PNP, Small Signal BJT, 40 V, 0.6 A, SC70-3, SOT-323	MMST4403-7-F	Diodes, Inc.
15	1	R1	RES, 2 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2001V	Panasonic
16	1	R2	RES, 20.0 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2002V	Panasonic
17	1	R3	RES, 2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ202V	Panasonic
18	1	R4	RES, 16 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ160V	Panasonic
19	1	R5	RES, 4.7 kΩ, 5%, 1/8 W, Carbon Film	CF18JT4K70	Stackpole
20	1	R6	RES, 200 Ω, 5%, 1/8 W, Carbon Film	CF18JT200R	Stackpole
21	1	RF1	RES, 8.2 Ω, 2 W, Fusible/Flame Proof Wire Wound	CRF253-4 5T 8R2	Vitrohm
22	1	T1	Bobbin, EE13, Vertical, 10 pins	P-1302-2	Pin Shine
23	1	TP1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
24	2	TP2 TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
25	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
26	1	U1	LinkSwitch-XT2 , SO-8C	LNK3604D	Power Integrations
27	1	VR1	Diode, Zener, 75 V, 500 MW, SOD123	MMSZ5267BT1G	ON Semi
28	1	VR2	4.3 V, 5%, 500 mW, SOD-123, -55 C ~ +150 C	MMSZ4687T1G	ON Semi

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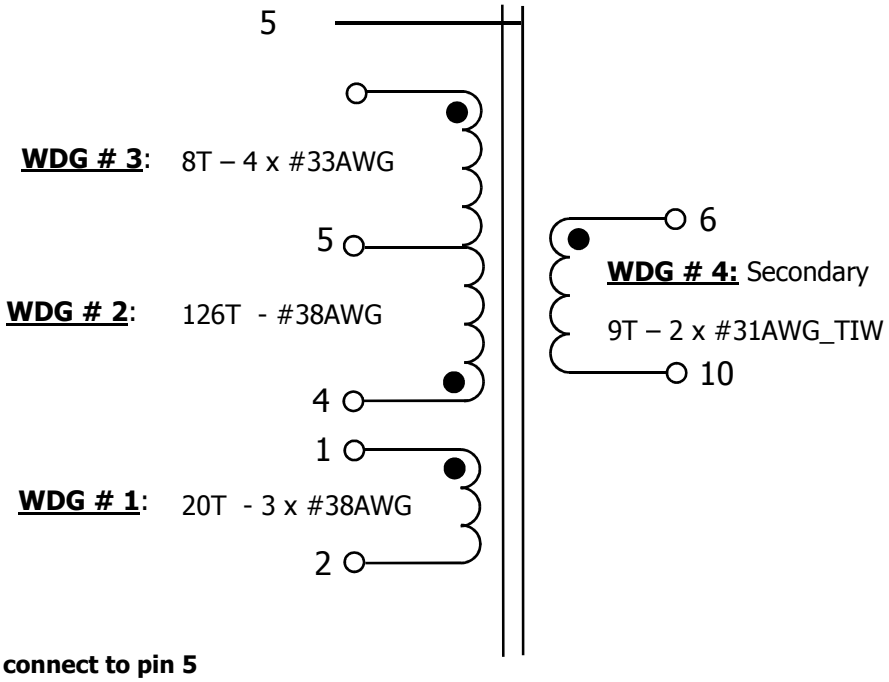
7 Transformer Specification

7.1 *Electrical Diagram*



Note: Flux band connect to pin 5

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Electrical Strength	60 seconds, 60 Hz, from pins 1-4 to pins 7-8.	3000 VAC
Primary Inductance	Pins 4-5, all other windings open.	1625 µH, ±7%
Resonant Frequency	Pins 4-5, all other windings open.	750 kHz (Min.)
Primary Leakage Inductance	Pins 4-5, all other windings short	15 µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EE13 Gapped for 46vnH/T^2.
[2]	Bobbin: EE13, Vertical, part NO. 25-01023-00.
[3]	Magnet Wire: #38 AWG, Double Coated.
[4]	Triple insulated: #31 AWG.
[5]	Magnet Wire: #32 AWG, Double Coated.
[6]	Tape: 3M 1298 Polyester Film, 2 mils Thick, 7.5 mm Wide.
[7]	Copper Tape 2 mil Thick.
[8]	Varnish.

7.4 *Transformer Build Diagram*

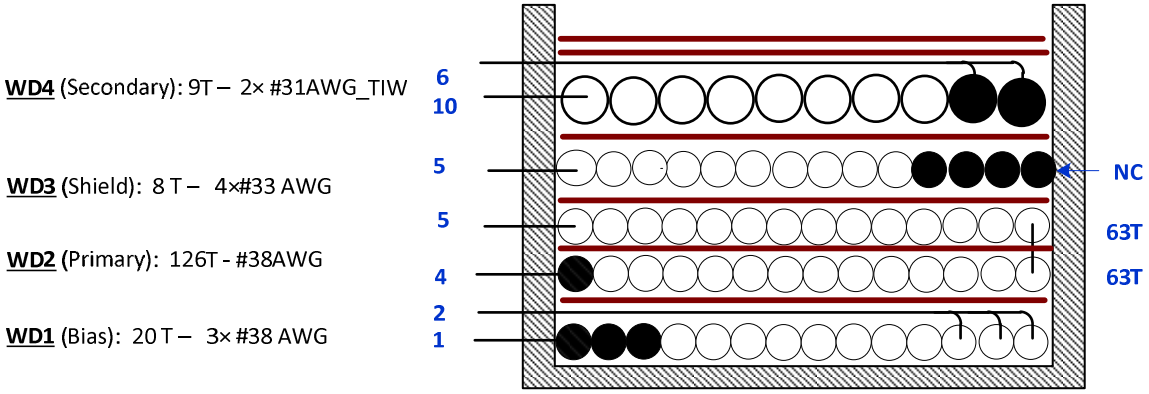


Figure 7 – Transformer Build Diagram.

7.5 *Transformer Instructions*

Winding Preparation	Place the bobbin [2] with pin side is on the left hand side. Winding direction is clockwise direction.
Winding 1: Bias	Start at pin 1, wind 20 tri-filar turns of wire item [3] from left to right. Wind with tight tension across entire bobbin evenly in a single uniform layer. At the last turn bring the wires back to the left and finish at pin 2.
Insulation	1 layer of tape item [6] for insulation.
Winding 2: Primary	Start at pin 4, wind 63 turns of item [3] from left to right uniformly, 1 layer of tape item [6], continue wind another 63 turns uniformly from right to left and finish at pin 5.
Insulation	1 layer of tape item [6] for insulation.
Winding 3: shield	Use 4 wires item [4], start from the right side of the bobbin, wind 8 turns from right to left with tight tension and finish at pin 5. Now cut short the wires floating on the right become to No-Connect.
Insulation	1 layer of tape, item [6] for insulation.
Winding 4: Secondary	Use 4 wires item [5], leave ~½" floating on the right side of the bobbin, wind 9 turns from right to left with tight tension and finish at pin 10. Now bring the wires floating on the right side back to the left and terminate at pin 6.
Insulation	3 layers of tape item [6] for insulation.
Flux Band	Gap core halves to get 1625 µH. Construct a flux band by wrapping a single shorted turn of item [7] around the outside of windings and core halves. Make an electrical connection to pin 5 using wire item [4].
Finish	Wrap around the flux band 1 layer of tape item [6]. Dip varnish in item [8] – do not vacuum impregnate due to higher capacitance.

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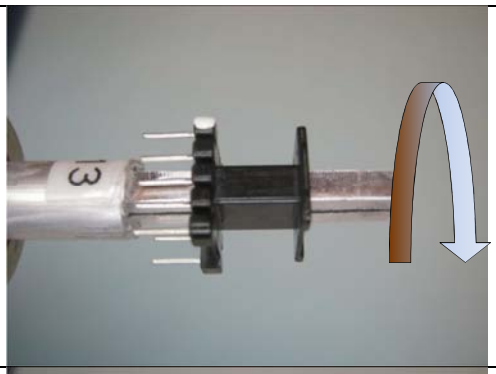
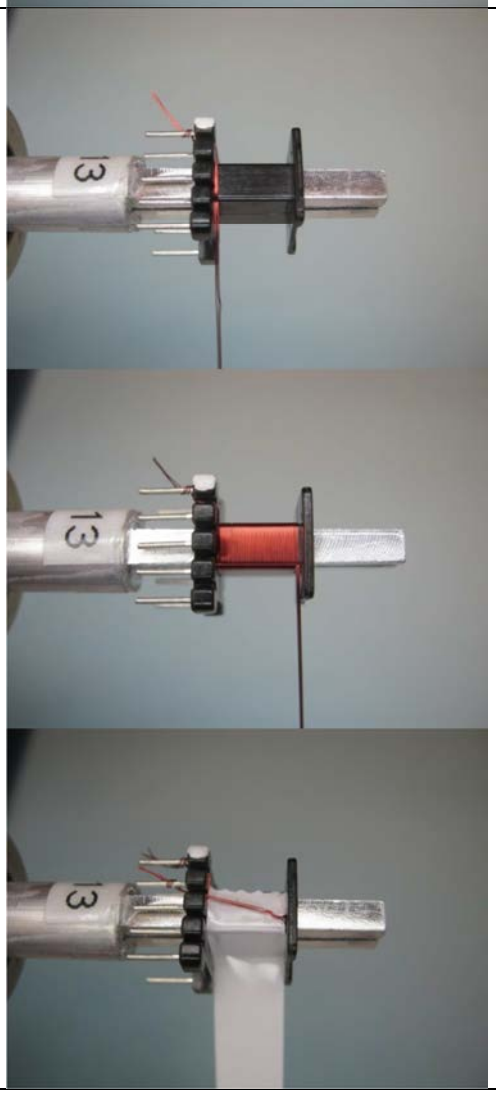
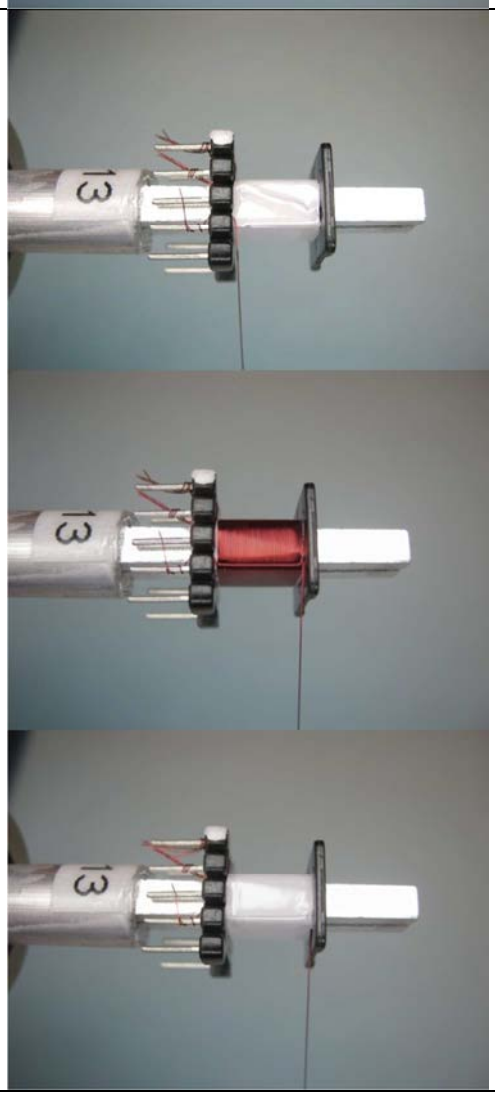
7.6 *Transformer Winding Illustrations*

Winding Preparation		Place the bobbin [2] with pin side is on the left hand side. Winding direction is clockwise direction.
Winding 1: Bias		Start at pin 1, wind 20 tri-filar turns of wire item [3] from left to right. Wind with tight tension across entire bobbin evenly in a single uniform layer. At the last turn bring the wires back to the left and finish at pin 2.

Insulation		1 layer of tape, item [6] for insulation
Winding 2: Primary		Start at pin 4, wind 63 turns of item [3] from left to right uniformly, 1 layer of tape item [6], continue wind another 63 turns uniformly from right to left and finish at pin 5.

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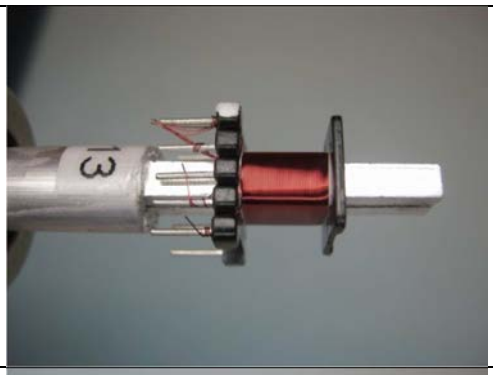
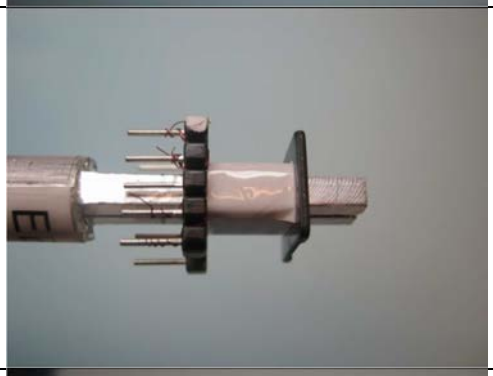
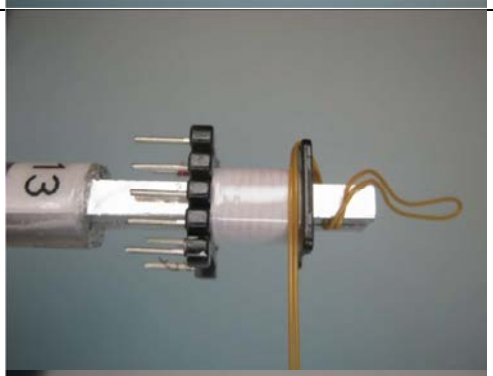
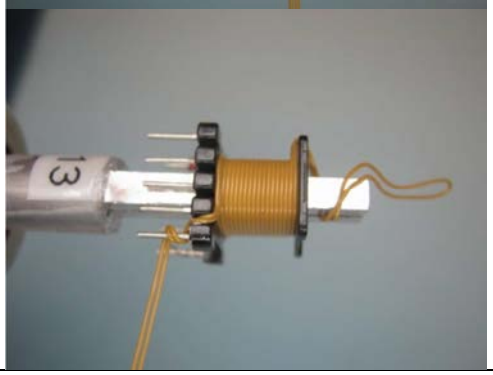
		
Insulation		1 layer of tape, item [6] for insulation.
Winding 3: Shield	 	Use 4 wires item [4], start from the right side of the bobbin, wind 8 turns from right to left with tight tension and finish at pin 5. Now cut short the wires floating on the right become to no-connect.

		
Insulation		1 layer of tape, item [6] for insulation.
Winding 4: Secondary	 	Use 4 wires item [5], leave ~½" floating on the right side of the bobbin, wind 9 turns from right to left with tight tension and finish at pin 10. Now bring the wires floating on the right side back to the left and terminate at pin 6.

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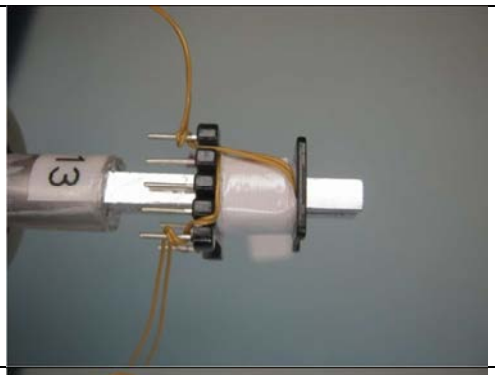
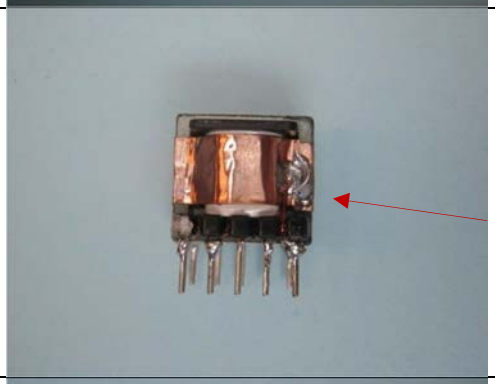
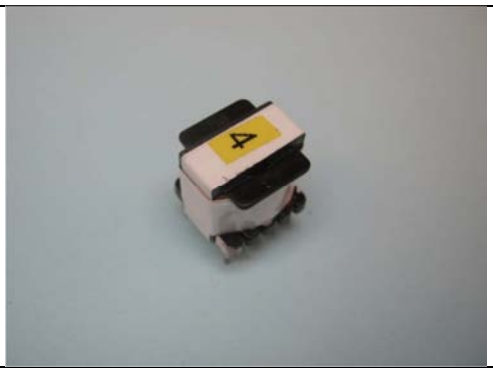
		
Insulation		3 layers of tape item [6] for insulation and secure the windings.
Flux band		Gap core halves to get 1625 μH. Construct a flux band by wrapping a single shorted turn of item [7] around the outside of windings and core halves. Make an electrical connection to pin 5 using wire item [4].
Finish		Wrap around the flux band 1 layer of tape item [6]. Dip varnish in item [8] – do not vacuum impregnate due to higher capacitance.

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8 Transformer Design Spreadsheet

ACDC_LinkSwitch-XT2_102516; Rev.0.1; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-XT2 Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.00			Volts	Output Voltage (main) (For CC designs enter upper CV tolerance limit)
IO	0.50			Amps	Power Supply Output Current (For CC designs enter upper CC tolerance limit)
CC Threshold Voltage	0.00			Volts	Voltage drop across sense resistor.
Output Cable Resistance	0.00		0.00	Ohms	Enter the resistance of the output cable (if used)
PO			2.50	Watts	Output Power (VO x IO + CC dissipation)
Feedback Type	OPTO		Opto		Choose 'BIAS' for Bias winding feedback and 'OPTO' for Optocoupler feedback from the 'Feedback Type' drop down box at the top of this spreadsheet
Add Bias Winding	Yes		Yes		Choose 'YES' in the 'Bias Winding' drop down box at the top of this spreadsheet to add a Bias winding. Choose 'NO' to continue design without a Bias winding. Addition of Bias winding can lower no load consumption
Clampless design	Yes		External clamp		!!! Warning. Clampless designs are supported only with the LNK362 device. Select NO from the Clampless drop down box at the top of this spreadsheet and continue
n			0.70		Efficiency Estimate at output terminals.
Z	0.50		0.50		Loss Allocation Factor (suggest 0.5 for CC=0 V, 0.75 for CC=1 V)
tC	2.90			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	6.60			uFarads	Input Capacitance
Input Rectification Type	F		***F***		Choose H for Half Wave Rectifier and F for Full Wave Rectification from the 'Rectification' drop down box at the top of this spreadsheet
ENTER LinkSwitch-XT2 VARIABLES					
LinkSwitch-XT2	**LNK3604**		**LNK3604**		User selection for LinkSwitch-XT2. Ordering info - Suffix P/G indicates DIP 8 package; suffix D indicates SO8 package; second suffix N indicates lead free RoHS compliance
Chosen Device		*LNK3604*			
ILIMIT MODE	**RED**		RED		Chose from STD or RED current limit
ILIMITMIN			0.180	Amps	Minimum Current Limit
ILIMITMAX			0.230	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I^2fmin			4017.6	A^2Hz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	77.00		77.00	Volts	Reflected Output Voltage
VDS			10.00	Volts	LinkSwitch-XT2 on-state Drain to Source Voltage
VD			0.50	Volts	Output Winding Diode Forward Voltage Drop
KP			1.06		Ripple to Peak Current Ratio (0.6 < KP < 6.0). For Clampless Designs use KP > 1.1
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EE13**		**EE13**		User-Selected transformer core
Core		*EE13*		*P/N:*	PC40EE13-Z
Bobbin		*EE13_BOBBIN*		*P/N:*	EE13_BOBBIN

AE			0.17	cm^2	Core Effective Cross Sectional Area
LE			3.02	cm	Core Effective Path Length
AL			1130.00	nH/T^2	Ungapped Core Effective Inductance
BW			7.90	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2.00		Number of Primary Layers
NS	9		9		Number of Secondary Turns
NB	20		20		Number of Bias winding turns
VB			12.22	Volts	Bias Winding voltage
PIVB			96	Volts	Bias Diode Maximum Peak Inverse Voltage
DC INPUT VOLTAGE PARAMETERS					
VMIN			82.26	Volts	Minimum DC Input Voltage
VMAX			374.77	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.50		Maximum Duty Cycle
IAVG			0.05	Amps	Average Primary Current
IP			0.18	Amps	Minimum Peak Primary Current
IR			0.18	Amps	Primary Ripple Current
IRMS			0.07	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1625	uHenries	Typical Primary Inductance. +/- 7%
LP_TOLERANCE	7		7	%	Primary inductance tolerance
NP			126		Primary Winding Number of Turns
ALG			102	nH/T^2	Gapped Core Effective Inductance
BM		***Info***	1735	Gauss	!!! Info. Flux densities above ~ 1500 Gauss may produce audible noise. Verify with dip varnished sample transformers. Increase NS to greater than or equal to 11 turns or increase VOR
BAC			867	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1588		Relative Permeability of Ungapped Core
LG			0.19	mm	Gap Length (Lg > 0.1 mm)
BWE			15.8	mm	Effective Bobbin Width
OD	0.14		0.14	mm	Maximum Primary Wire Diameter including insulation
INS			0.03	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.11	mm	Bare conductor diameter
AWG			38	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			16	Cmils	Bare conductor effective area in circular mils
CMA			222	Cmils/Amp	Primary Winding Current Capacity (150 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			2.52	Amps	Peak Secondary Current
ISRMS			0.98	Amps	Secondary RMS Current
IRIPPLE			0.84	Amps	Output Capacitor RMS Ripple Current
CMS			196	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			27	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.36	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.88	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.26	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			556	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)

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PIVS			32	Volts	Output Rectifier Maximum Peak Inverse Voltage
FEEDBACK COMPONENTS					
Recommended Bias Diode			1N4003 - 1N4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI. See LinkSwitch-XT2 Design Guide
R1			500 - 1000	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-XT2 Design Guide
R2			200 - 820	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-XT2 Design Guide
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			5.00	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			0.50	Amps	Output DC Current
PO1			2.50	Watts	Output Power
VD1			0.50	Volts	Output Diode Forward Voltage Drop
NS1			9.00		Output Winding Number of Turns
ISRMS1			0.98	Amps	Output Winding RMS Current
IRIPPLE1			0.84	Amps	Output Capacitor RMS Ripple Current
PIVS1			31.77	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			SB140, 1N5819		Recommended Diodes for this output
Pre-Load Resistor			2	k-Ohms	Recommended value of pre-load resistor
CMS1			195.78	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			27.00	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.36	mm	Minimum Bare Conductor Diameter
ODS1			0.88	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current
PO2			0.00	Watts	Output Power
VD2			0.70	Volts	Output Diode Forward Voltage Drop
NS2			1.15		Output Winding Number of Turns
ISRMS2			0.00	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			3.41	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS2			0.00	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current
PO3			0.00	Watts	Output Power
VD3			0.70	Volts	Output Diode Forward Voltage Drop
NS3			1.15		Output Winding Number of Turns
ISRMS3			0.00	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			3.41	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output

CMS3			0.00	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			2.50	Watts	Total Output Power
Negative Output	N/A		N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

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9 Performance Data

9.1 *Full Load Efficiency vs. Input Line Voltage*

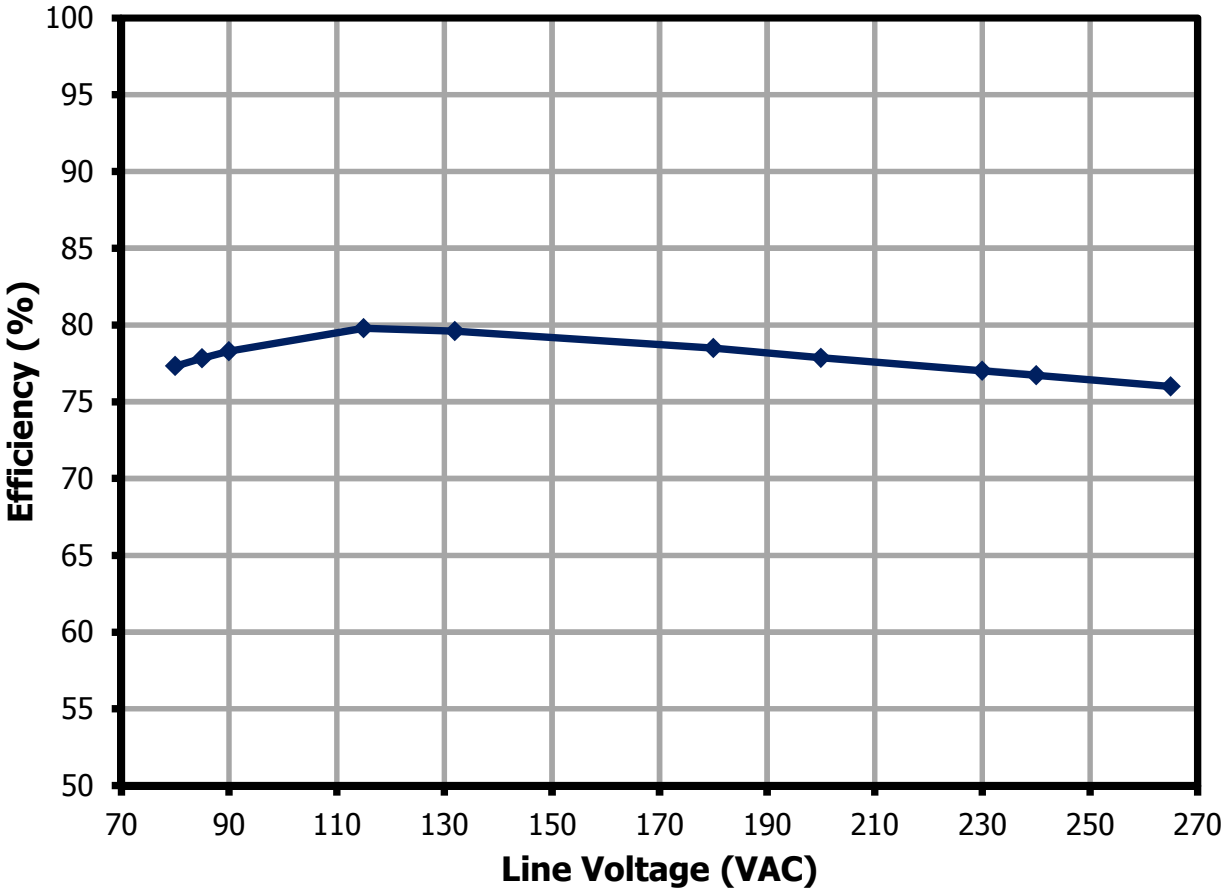

Figure 8 – Efficiency vs. Line Voltage, Room Temperature.

9.2 *Efficiency vs. Load*

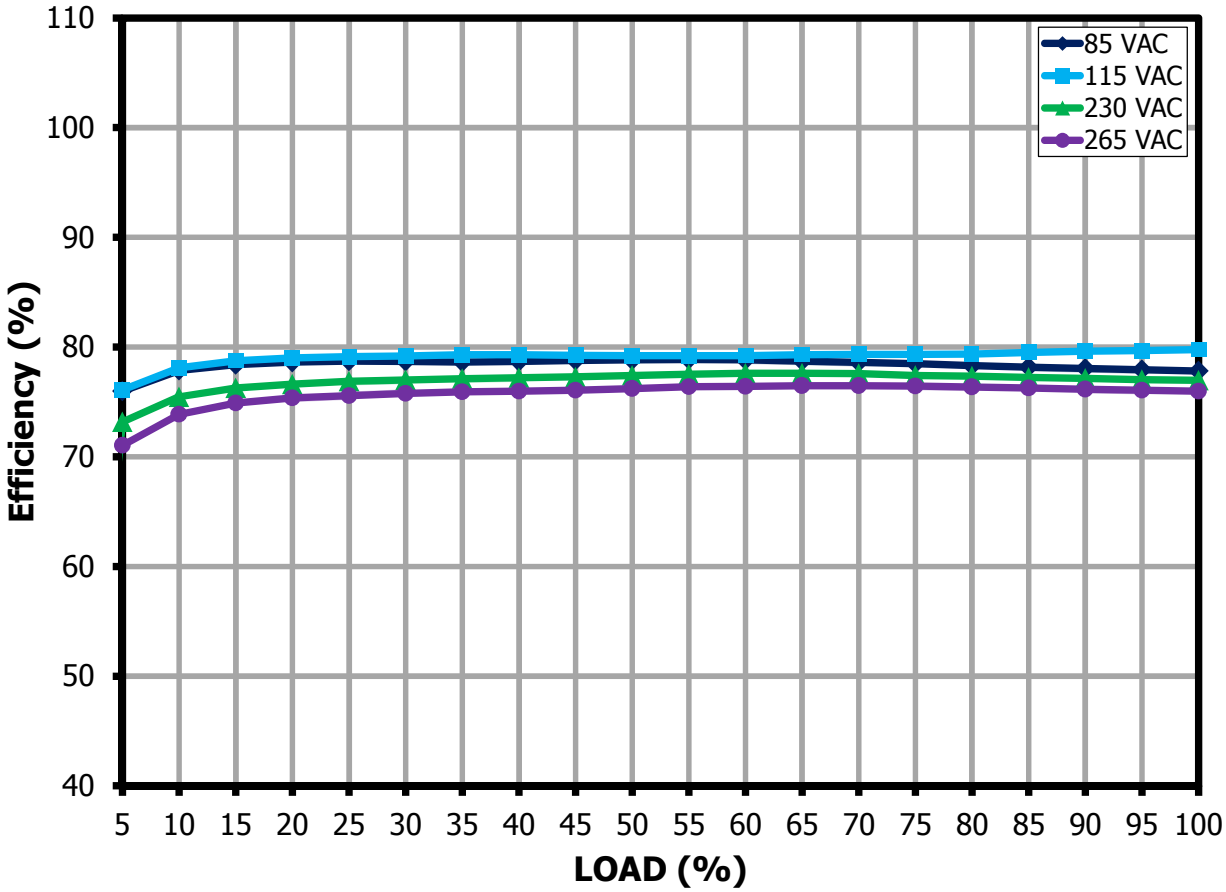

Figure 9 – Efficiency vs. Load, Room Temperature (Measured at the Output Terminal).

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9.3 *No-Load Input Power*

No-load input power soak time: 20 mins.

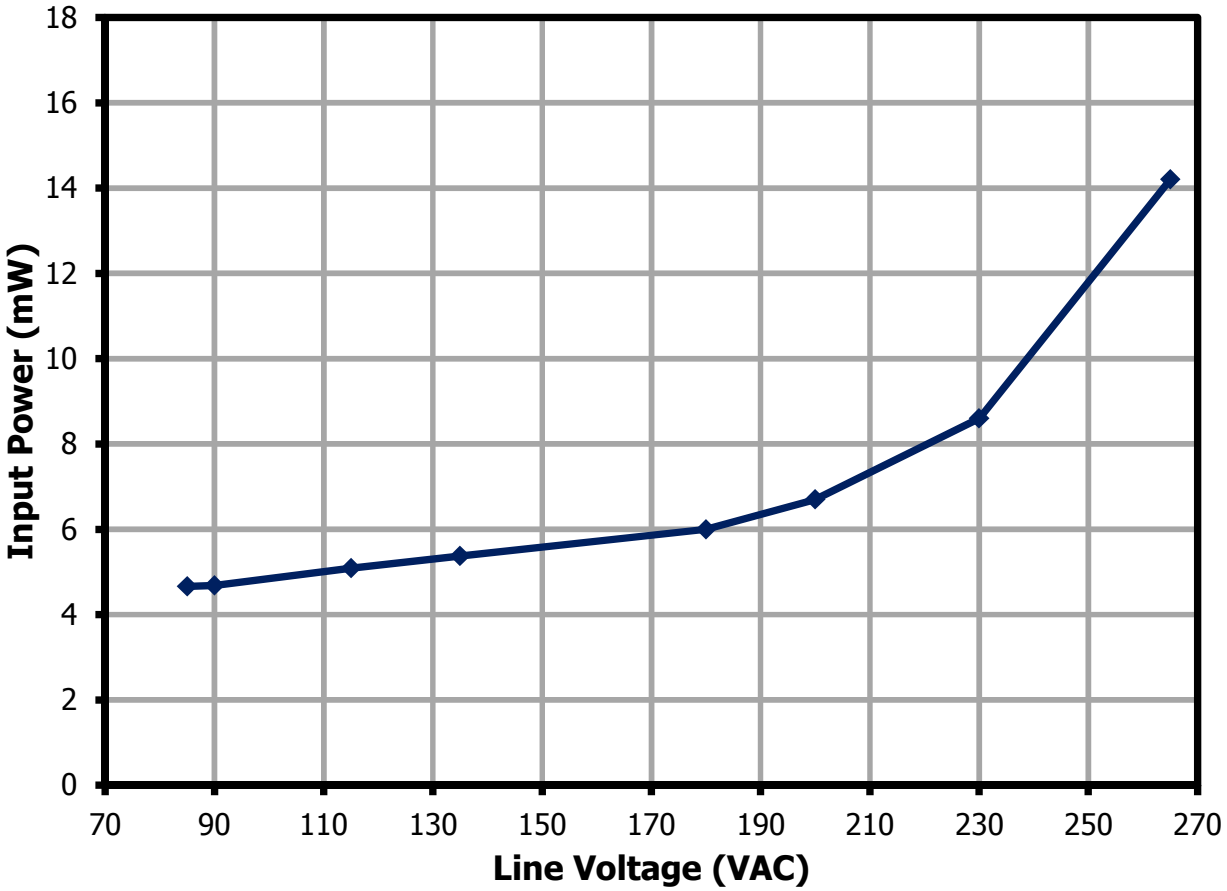

Figure 10 – Input Power vs. Input Line Voltage at No-Load, Room Temperature.

9.4 *Line and Load Regulation*

9.4.1 Line Regulation

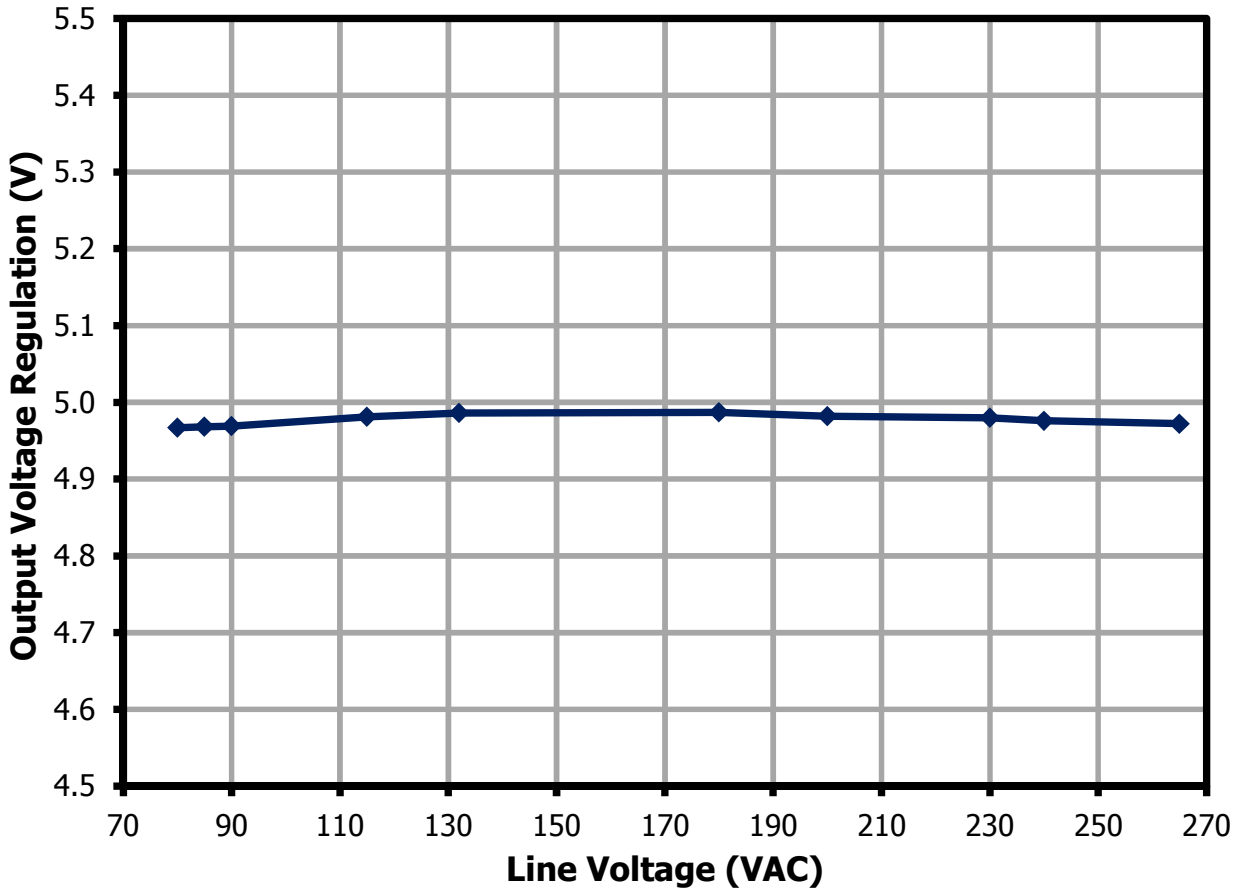

Figure 11 – Measured at the Board Output Terminals at Room Temperature.

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9.4.2 Load Regulation

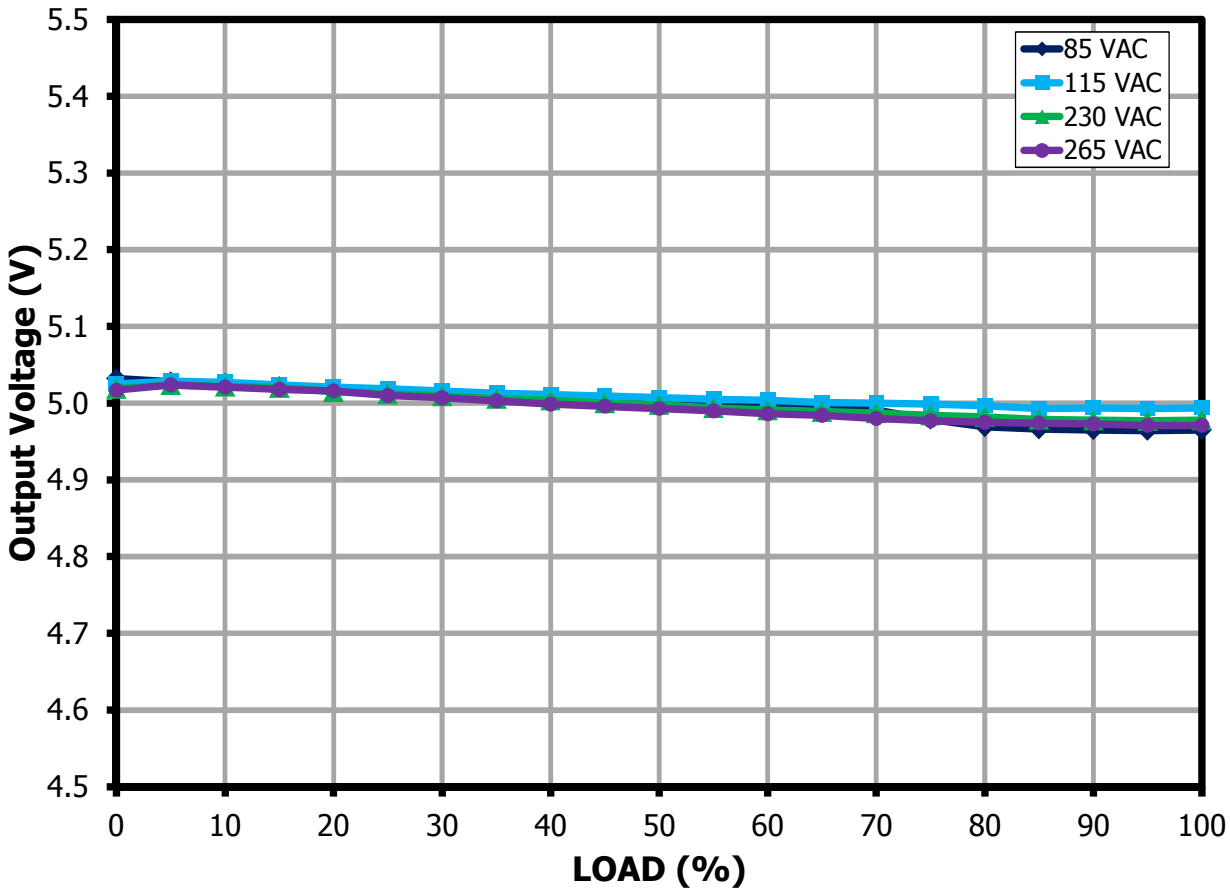

Figure 12 – Measured at the Board Output Terminals at Room Temperature.

10 Waveforms

10.1 *Output Voltage Ripple*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 1 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

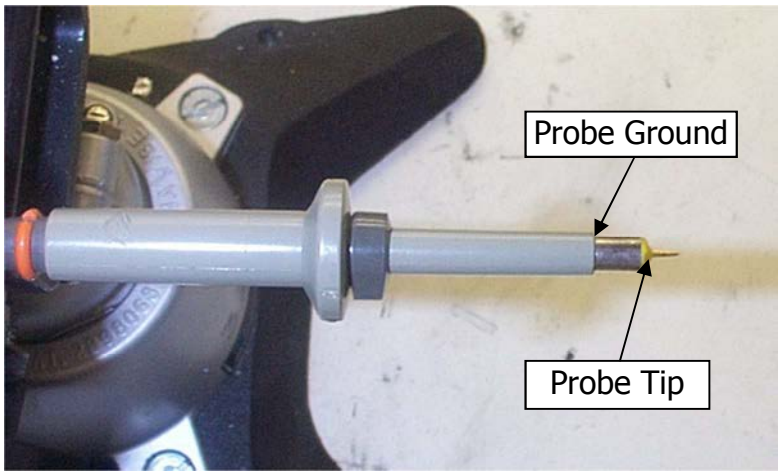

Figure 13 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

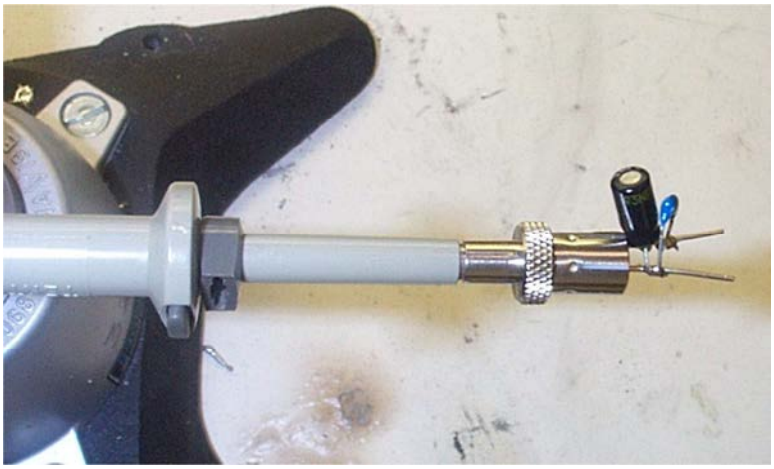

Figure 14 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

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10.2 *Measurement Results*

10.2.1 Output Ripple Voltage Graph from 0% - 100%

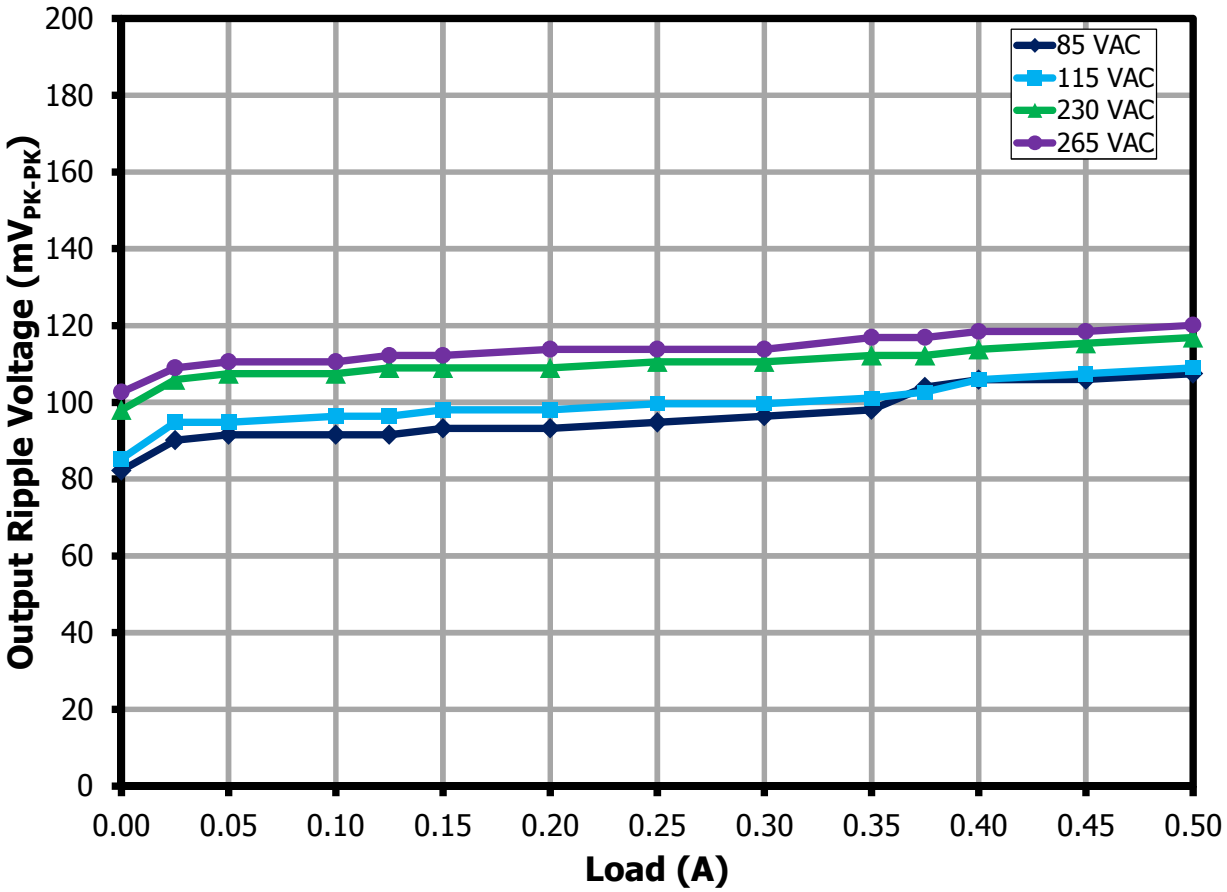

Figure 15 – Measured at the Board Output Terminals at Room Temperature.

85 V RIPPLE (mV_{PK-PK})	115 V RIPPLE (mV_{PK-PK})	230 V RIPPLE (mV_{PK-PK})	265 V RIPPLE (mV_{PK-PK})
107.51	109.09	117	120.16

10.2.2 Output Ripple Voltage Waveforms for 5 V Output

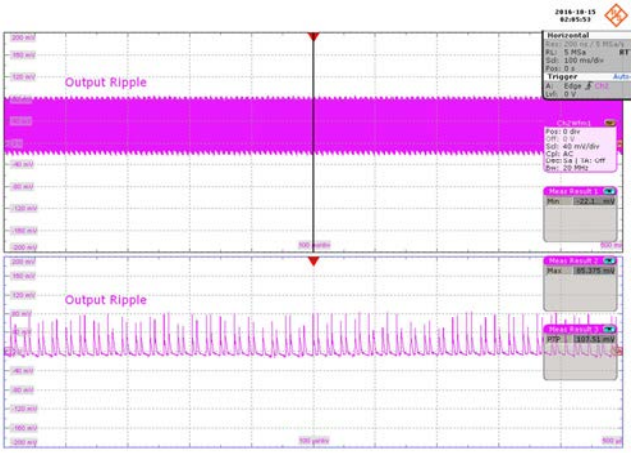

Figure 16 – 85 VAC Input.
Condition: 5 V – 500 mA.
V_{RIPPLE}, 40 mV / div., 100 ms / div.
Zoom, 100 µs / div.
$V_{RIPPLE(PK-PK)}$: 107.51 mV.

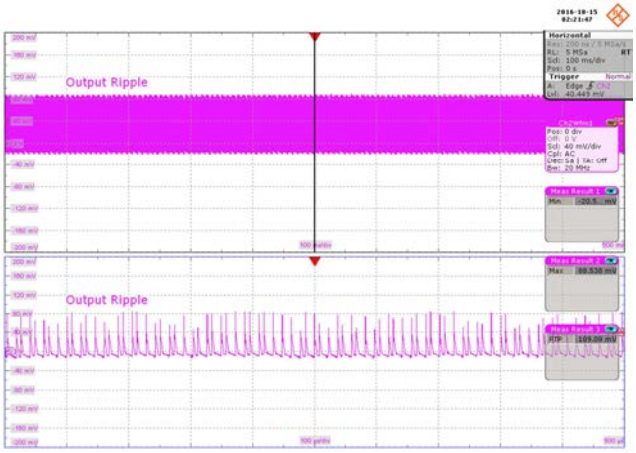

Figure 17 – 115 VAC Input.
Condition: 5 V – 500 mA.
V_{RIPPLE}, 40 mV / div., 100 ms / div.
Zoom, 100 µs / div.
$V_{RIPPLE(PK-PK)}$: 109.09 mV

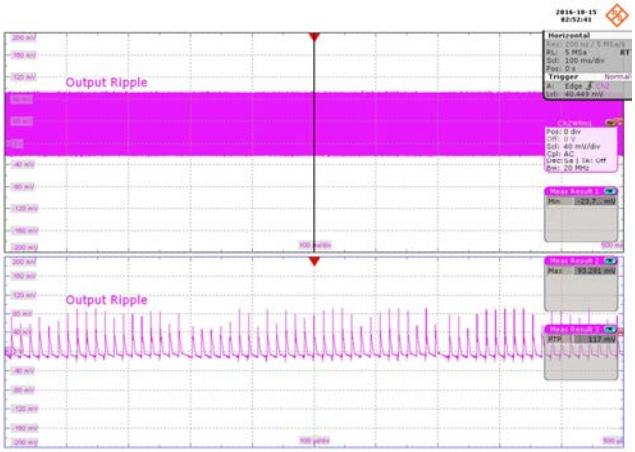

Figure 18 – 230 VAC Input.
Condition: 5 V – 500 mA.
V_{RIPPLE}, 40 mV / div., 100 ms / div.
Zoom, 100 µs / div.
$V_{RIPPLE(PK-PK)}$: 117 mV.

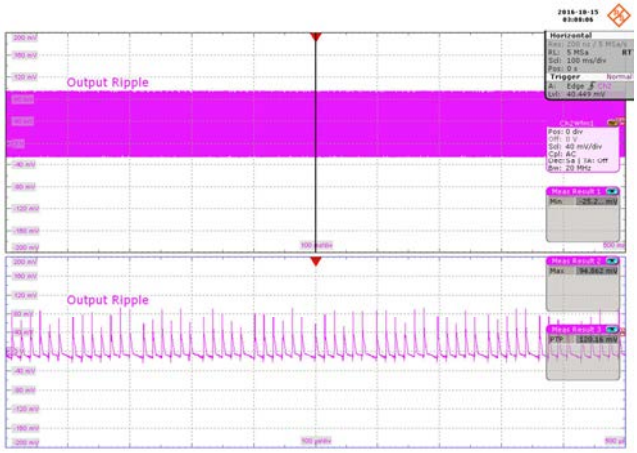

Figure 19 – 265 VAC Input.
Condition: 5 V – 500 mA.
V_{RIPPLE}, 40 mV / div., 100 ms / div.
Zoom, 100 µs / div.
$V_{RIPPLE(PK-PK)}$: 120.16 mV.

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10.3 *Start-up Performance*

Measured at the board output terminals with 10 Ω as resistive load.

10.3.1 Start-up Operation V_{IN}, V_{OUT} and I_{OUT}

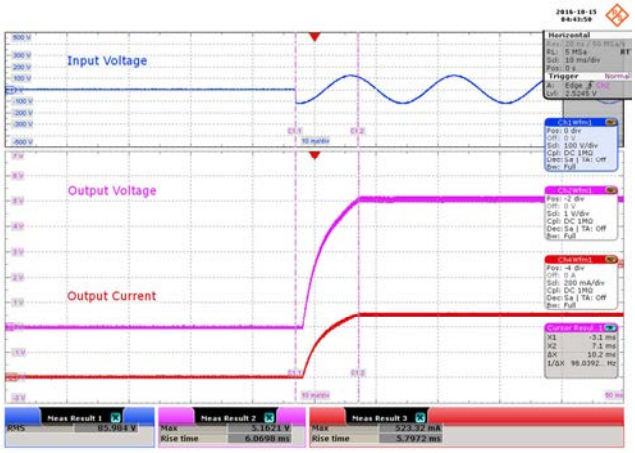

Figure 20 – 85 VAC Input.
Upper: V_{IN}, 100 V / div.
Middle: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 200 mA / div., 10 ms / div.

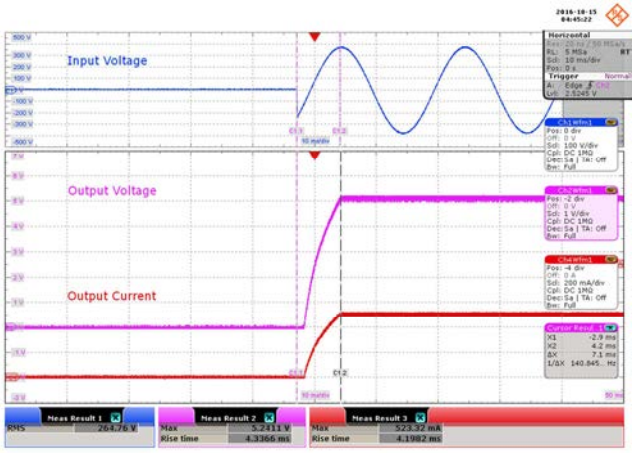

Figure 21 – 265 VAC Input.
Upper: V_{IN}, 100 V / div.
Middle: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 200 mA / div., 10 ms / div.

10.3.2 Start-up Operation V_{DS} and I_{DS}

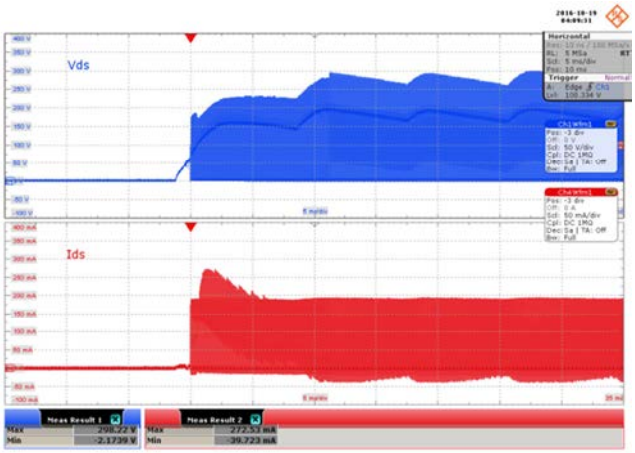

Figure 22 – 85 VAC Input.
Upper: V_{DS}, 50 V / div.
Lower: I_{DS}, 50 mA / div., 5 ms / div.
V_{DSMAX}: 298.22 V.
I_{DSMAX}: 272.53 mA.

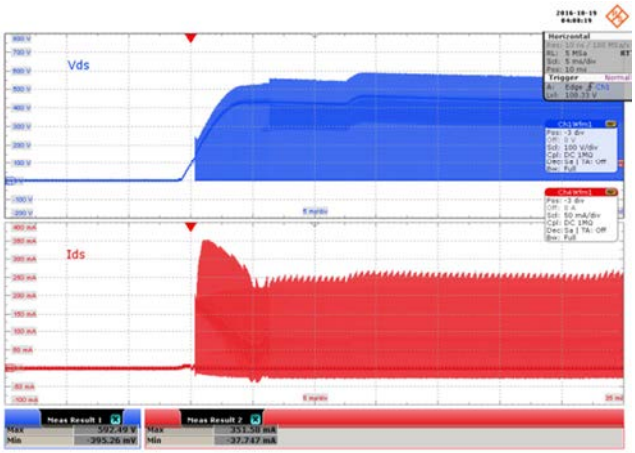

Figure 23 – 265 VAC Input.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 50 mA / div., 5 ms / div.
V_{DSMAX}: 592.49 V.
I_{DSMAX}: 351.58 mA.

10.3.3 Output Load Transient

10.3.3.1 Dynamic Loading from 0% - 100%

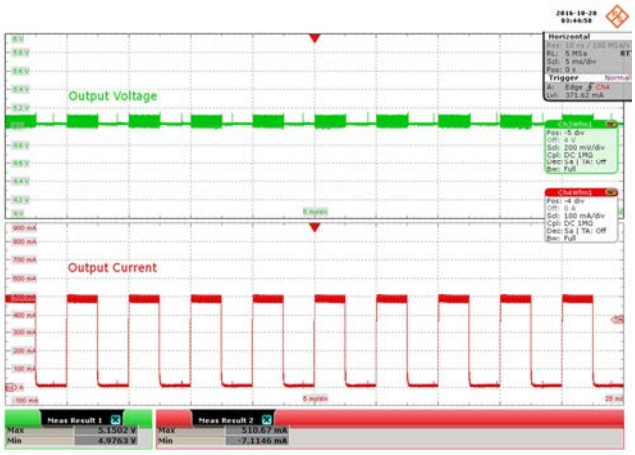

Figure 24 – 85 VAC Input.
V_{OUT}, 200 mV / div.
I_{OUT}, 100 mA / div., 5 ms / div.
V_{MAX}: 5.1502 V.
V_{MIN}: 4.9763 V.

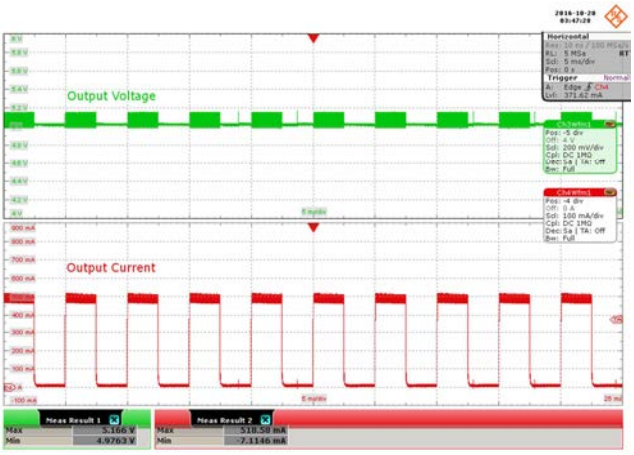

Figure 25 – 265 VAC Input.
V_{OUT}, 200 mV / div.
I_{OUT}, 100 mA / div., 5 ms / div.
V_{MAX}: 5.166 V.
V_{MIN}: 4.9763 V.

10.3.3.2 Dynamic Loading from 50% - 100%

Figure 26 – 85 VAC Input.
V_{OUT}, 200 mV / div.
I_{OUT}, 100 mA / div., 5 ms / div.
V_{MAX}: 5.1502 V.
V_{MIN}: 4.9684 V.

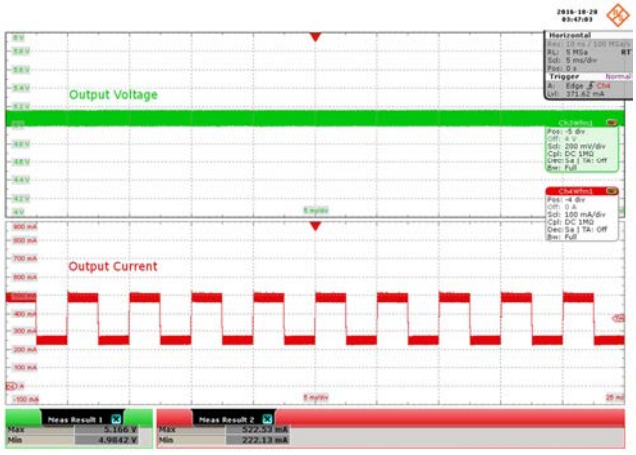

Figure 27 – 265 VAC Input.
V_{OUT}, 200 mV / div.
I_{OUT}, 100 mA / div., 5 ms / div.
V_{MAX}: 5.166 V.
V_{MIN}: 4.9842 V.

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10.4 *Drain Waveforms*

10.4.1 Normal Operation V_{DS} and I_{DS}

10.4.1.1 100% Load

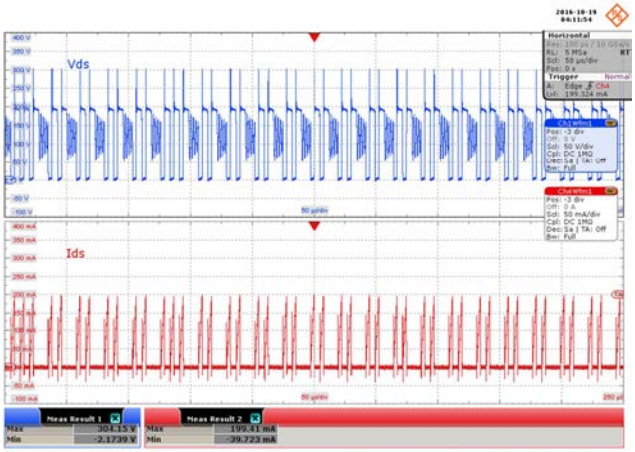

Figure 28 – 85 VAC Input.
Upper: V_{DS}, 50 V / div.
Lower: I_{DS}, 50 mA / div., 50 µs / div.

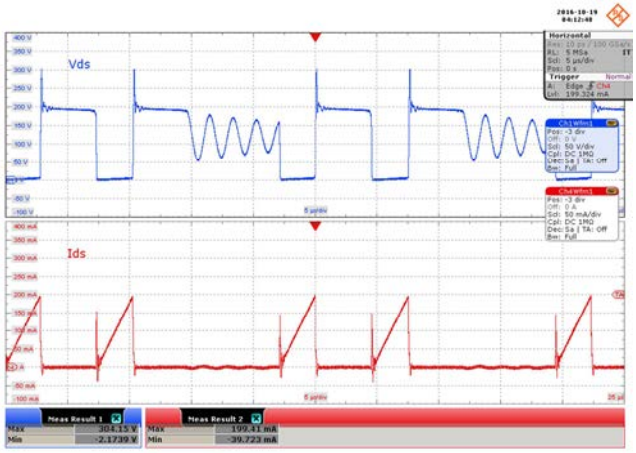

Figure 29 – 85 VAC Input.
Upper: V_{DS}, 50 V / div.
Lower: I_{DS}, 50 mA / div., 5 µs / div.
V_{DSMAX}: 304.15 V.
I_{DSMAX}: 199.41 mA.

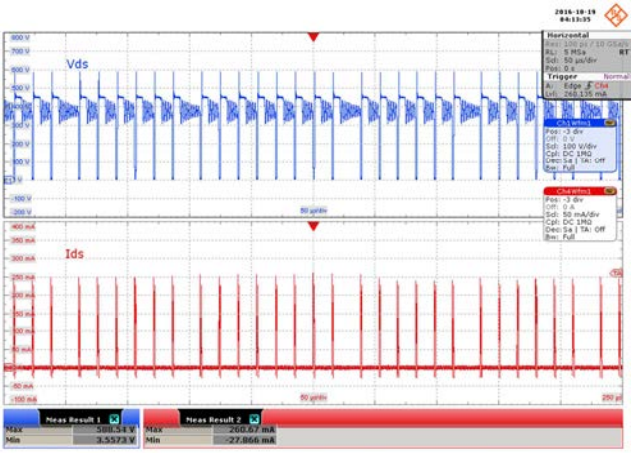

Figure 30 – 265 VAC Input.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 50 mA / div., 50 µs / div.

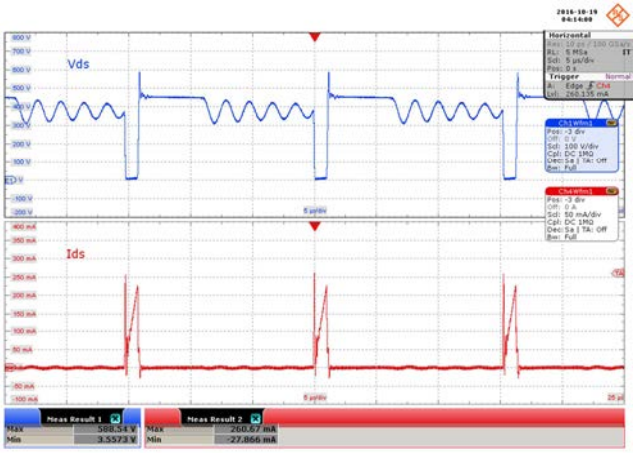

Figure 31 – 265 VAC Input.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 50 mA / div., 5 µs / div.
V_{DSMAX}: 588.54 V.
I_{DSMAX}: 260.67 mA.

10.5 *Output Short Waveforms*

Short the main output (5 V) and monitor I_{DS}, output voltage and output current. The first time a fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ first off period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ subsequent periods).

10.5.1 Fault During Start-up

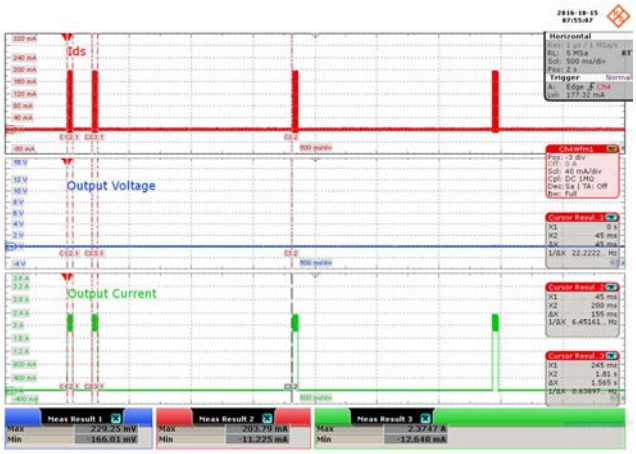

Figure 32 – 85 VAC Input.
Condition: 5 V – Shorted.
Upper: I_{DS}, 40 mA / div
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 400 mA / div., 500 ms / div.

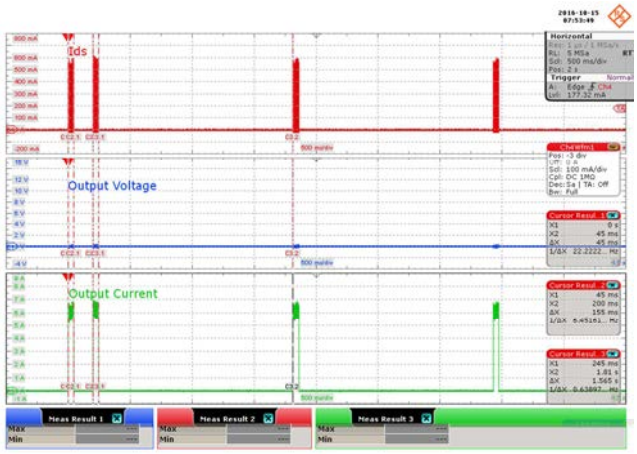

Figure 33 – 265 VAC Input.
Condition: 5 V – Shorted.
Upper: I_{DS}, 100 mA / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 400 mA / div., 500 ms / div.

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10.5.2 Fault During Normal Operation

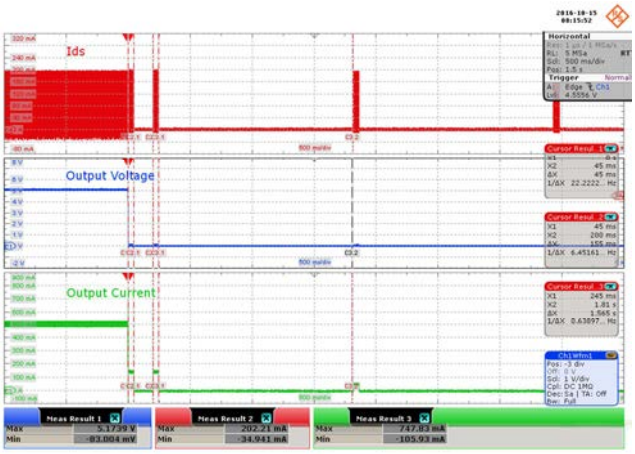

Figure 34 – 85 VAC Input.
Condition: 5 V – Shorted.
Upper: I_{DS}, 40 mA / div.
Middle: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 100 mA / div., 500 ms / div.

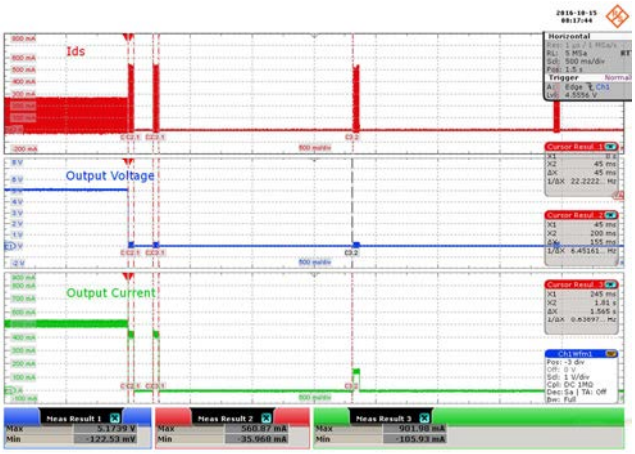

Figure 35 – 265 VAC Input.
Condition: 5 V – Shorted.
Upper: I_{DS}, 100 mA / div.
Middle: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 100 mA / div., 500 ms / div.

10.6 *Thermal Performance at Room Temperature*

This was done inside an acrylic box under room temperature condition. The board was mounted horizontal. The output set to 100% load. Soak the power supply for 2 hours.

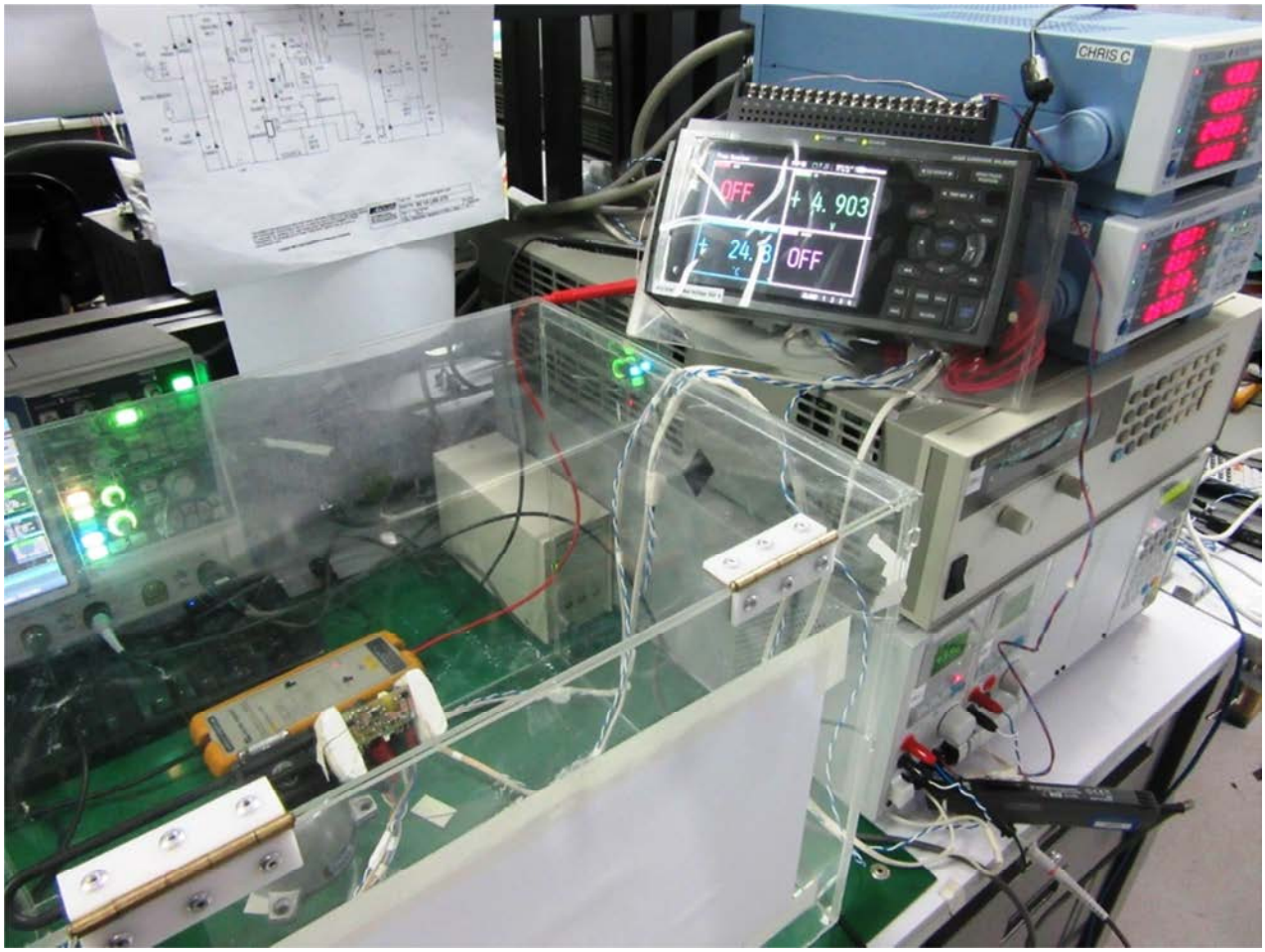

Figure 36 – Thermal Performance Set-up Using Acrylic Box.

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10.6.1 Thermal Performance at 85 VAC

Ambient temperature is 28.5 ºC

Figure 37 – LinkSwitch-XT2 (U1).
Spot: 49.9 ºC.

Figure 38 – Secondary Snubber Diode (D3).
Spot: 50.7 ºC.

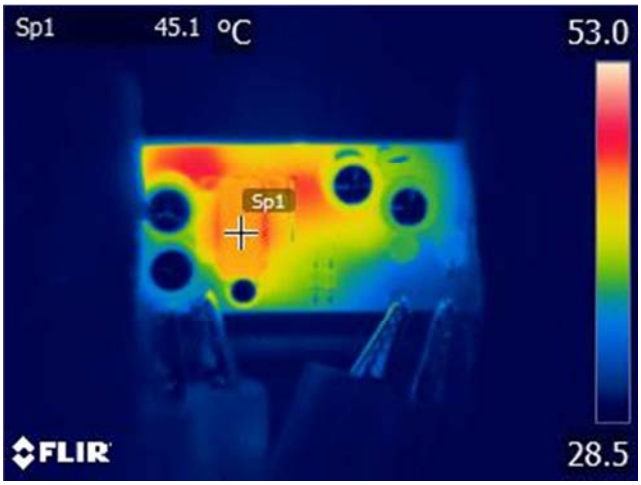

Figure 39 – Transformer core (T1).
Spot: 45.1 ºC.

Figure 40 – Transformer winding (T1).
Spot: 46.7 ºC.

10.6.2 Thermal Performance at 265 VAC

Ambient temperature is 28.5 ºC

Figure 41 – LNK-XT2 (U1).
Spot: 58.0 ºC.

Figure 42 – Secondary Snubber Diode (D3).
Spot: 53.9 ºC.

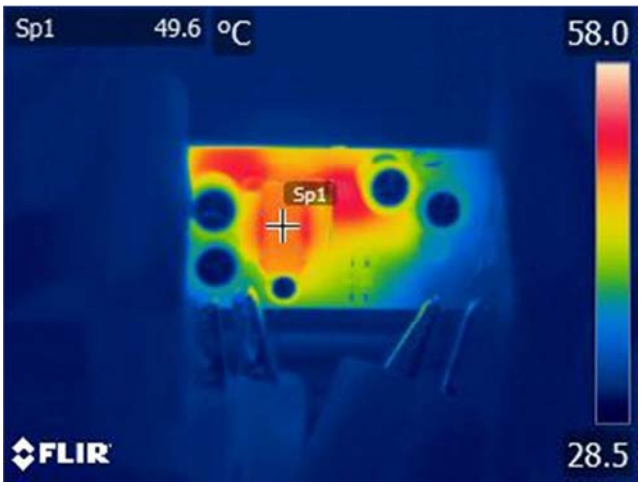

Figure 43 – Transformer Core (T1).
Spot: 49.6 ºC.

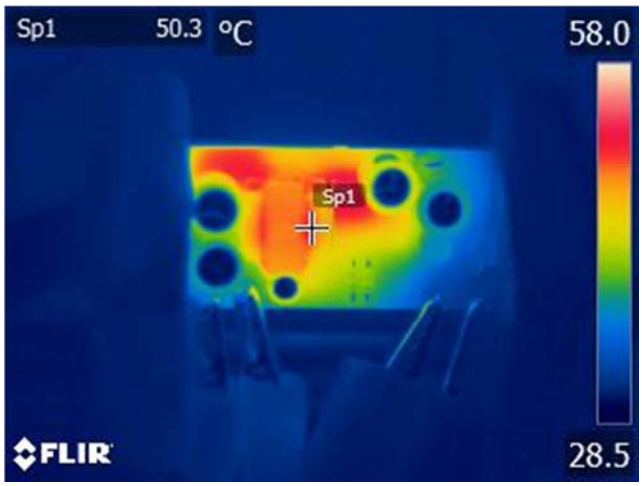

Figure 44 – Transformer Winding (T1).
Spot: 50.3 ºC.

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11 Conducted EMI

11.1 *Test Set-up Equipment*

11.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power Hi-tester.
4. Chroma measurement test fixture.
5. 10 Ω resistor load.
6. Input voltage set at 115 VAC and 230 VAC.

11.2 *Test Set-up*

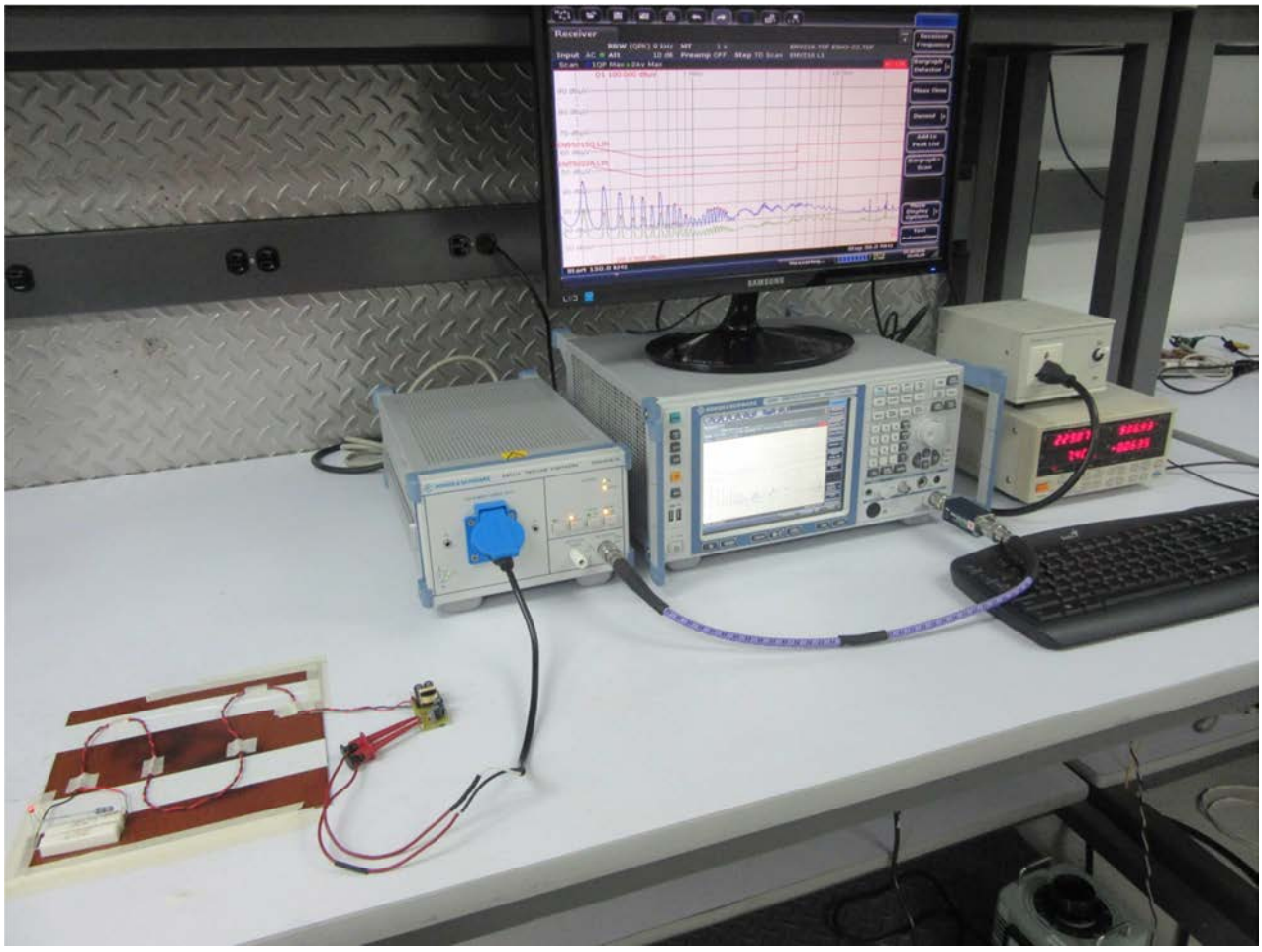

Figure 45 – EMI Test Set-up.

11.3 *Floating Output (QP / AV)*

11.3.1 115 VAC

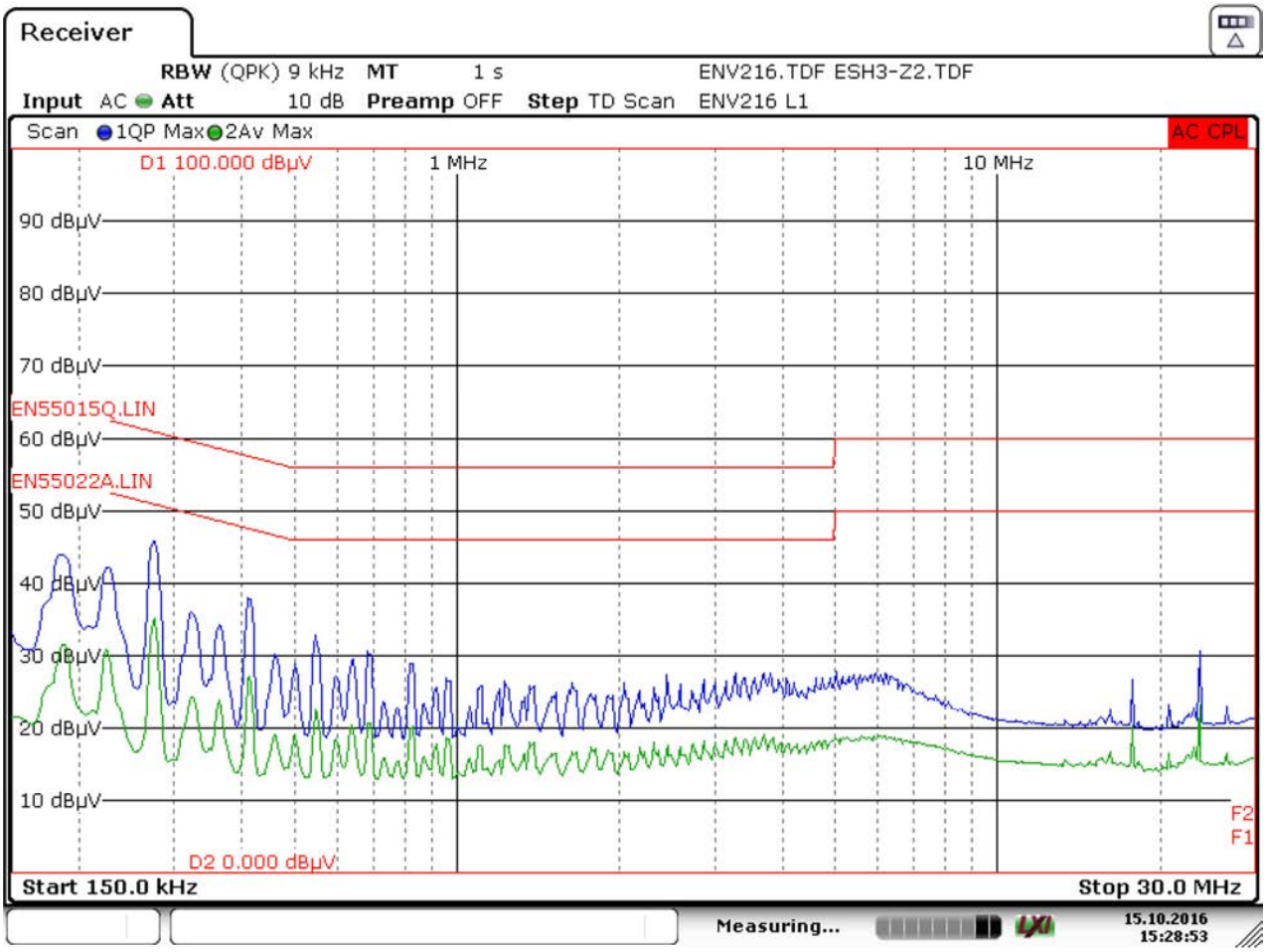

Figure 46 – Floating Negative Output at 115 VAC, LINE.

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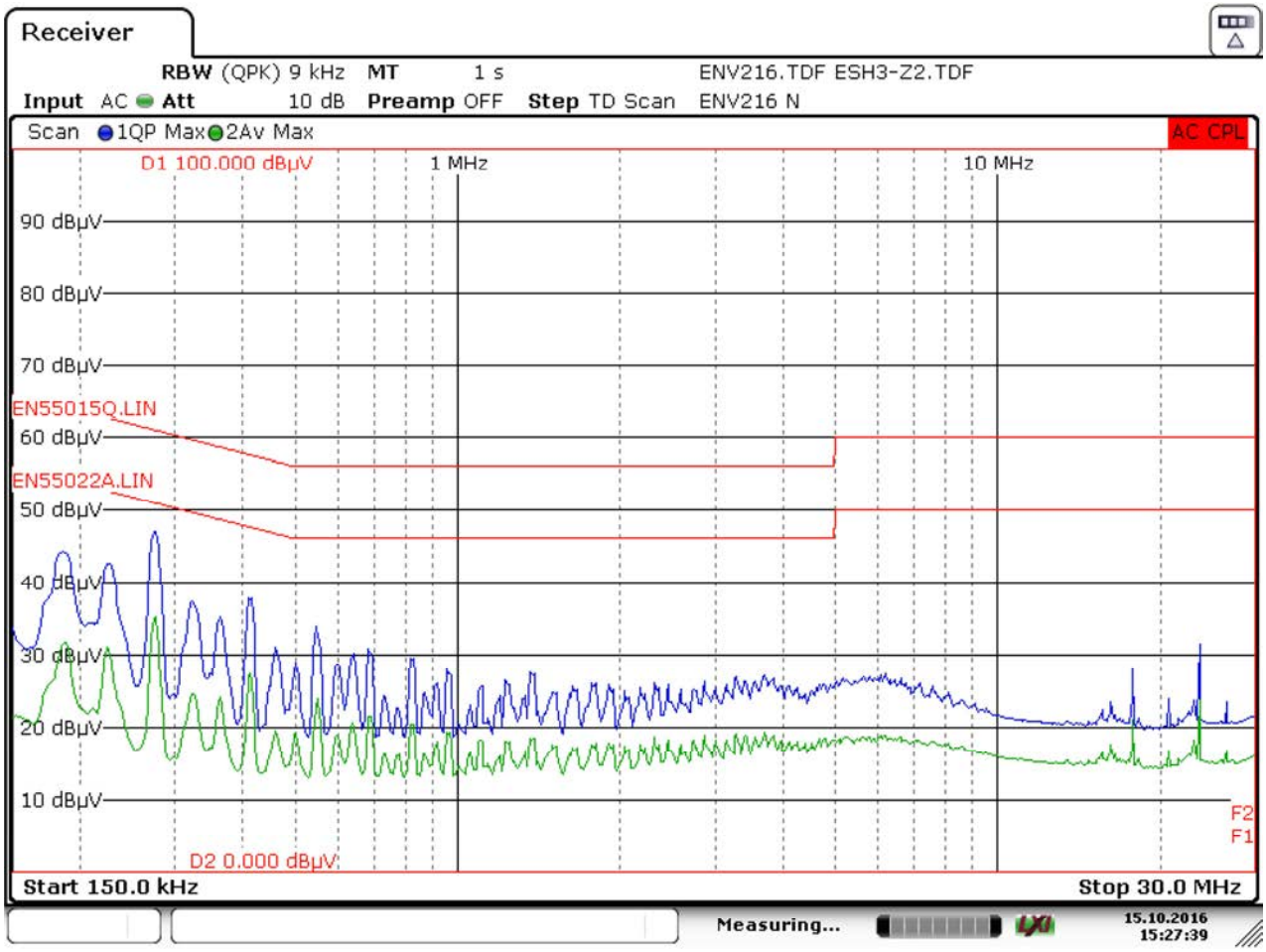

Figure 47 – Floating Negative Output at 115 VAC, NEUTRAL.

11.3.2 230 VAC

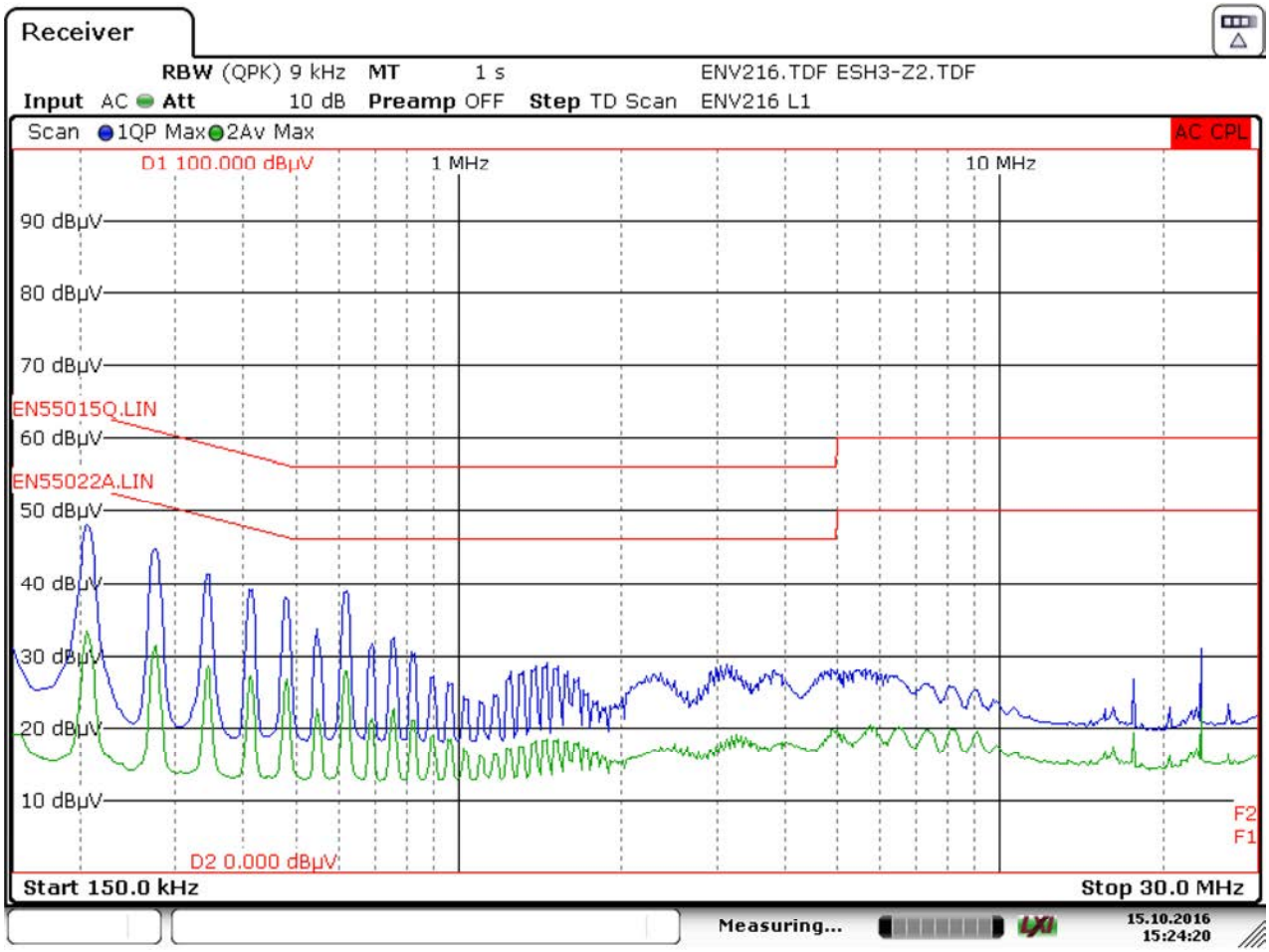

Figure 48 – Floating Negative Output at 230 VAC, LINE.

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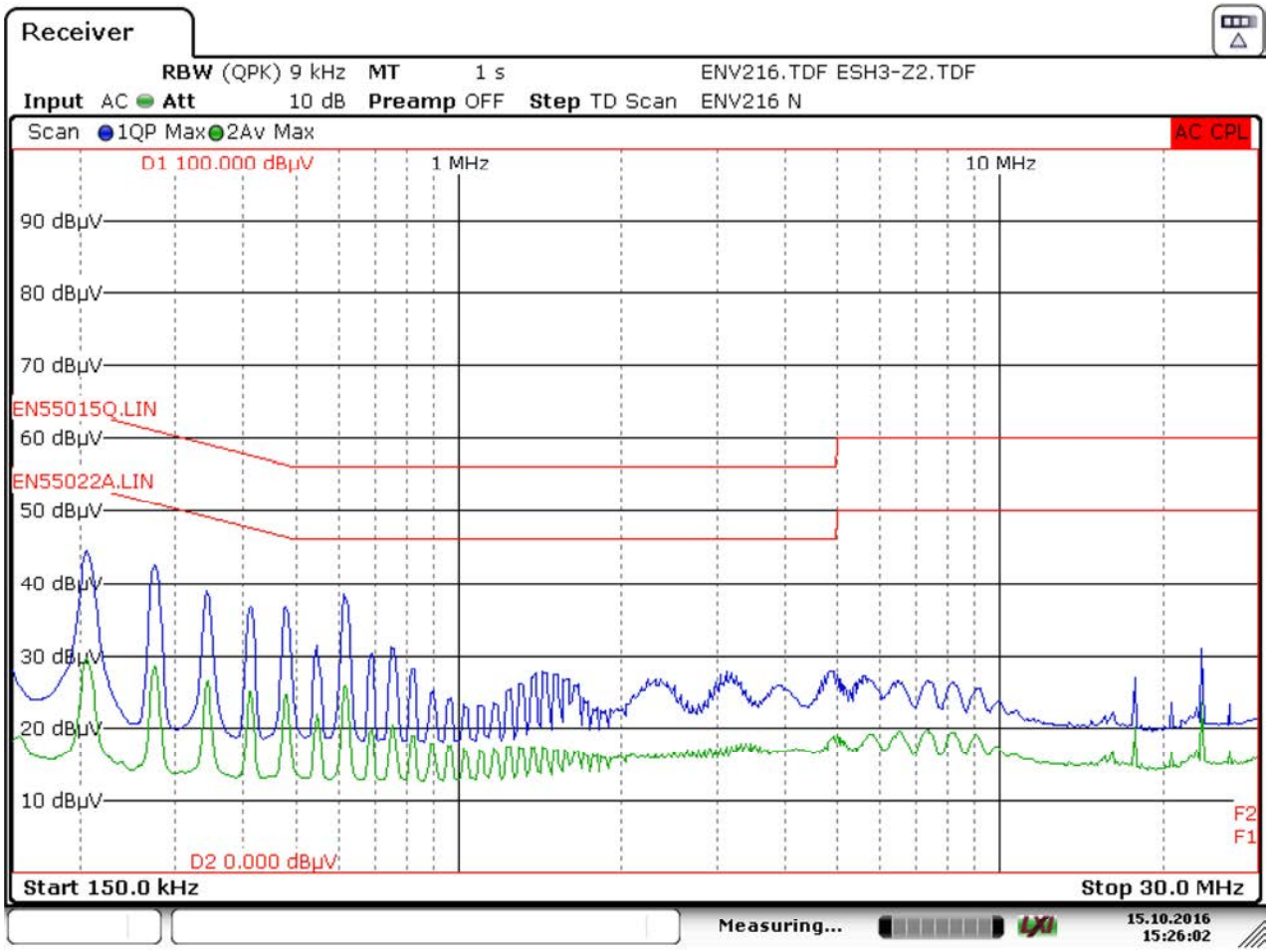

Figure 49 – Floating Negative Output at 230 VAC, NEUTRAL.

12 Line Surge

The unit was subjected to ±1000 V, differential surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (º)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

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Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

13 Revision History

Date	Author	Revision	Description and Changes	Reviewed
07-Dec-16	CC & JW	1.0	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

Patent Information

The products and applications illustrated herein (including transformer construction and circuits' external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.power.com/ip.htm.

Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@power.com

GERMANY
Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@power.com

JAPAN
Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail:
taiwansales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@power.com

UK
Cambridge Semiconductor,
a Power Integrations company
Westbrook Centre, Block 5,
2nd Floor
Milton Road
Cambridge CB4 1YG
Phone: +44 (0) 1223-446483
e-mail: eurosales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
Fax: +86-755-8672-8690
e-mail: chinasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI)
Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@power.com