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Revisions

Rev	Description	Date	Approved
XA	Initial Release	APR-13-2016	O. Romero
A	Prototype Production	APR-14-2016	O. Romero
AX1	Development	AUG-16-2016	O. Romero
B	2nd Release	SEP-02-2016	O. Romero

S32K144EVB-Q100

freescale semiconductor

Microcontroller Solutions Group

6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: ____ FIUO: X PUBI: ____

Designer: Osvaldo Romero	Drawing Title: S32K144EVB-Q100		
Drawn by: Osvaldo Romero	Page Title: TITLE PAGE		
Approved: APPROVER	Size C	Document Number SCH-29248 PDF: SPF-29248	Rev B
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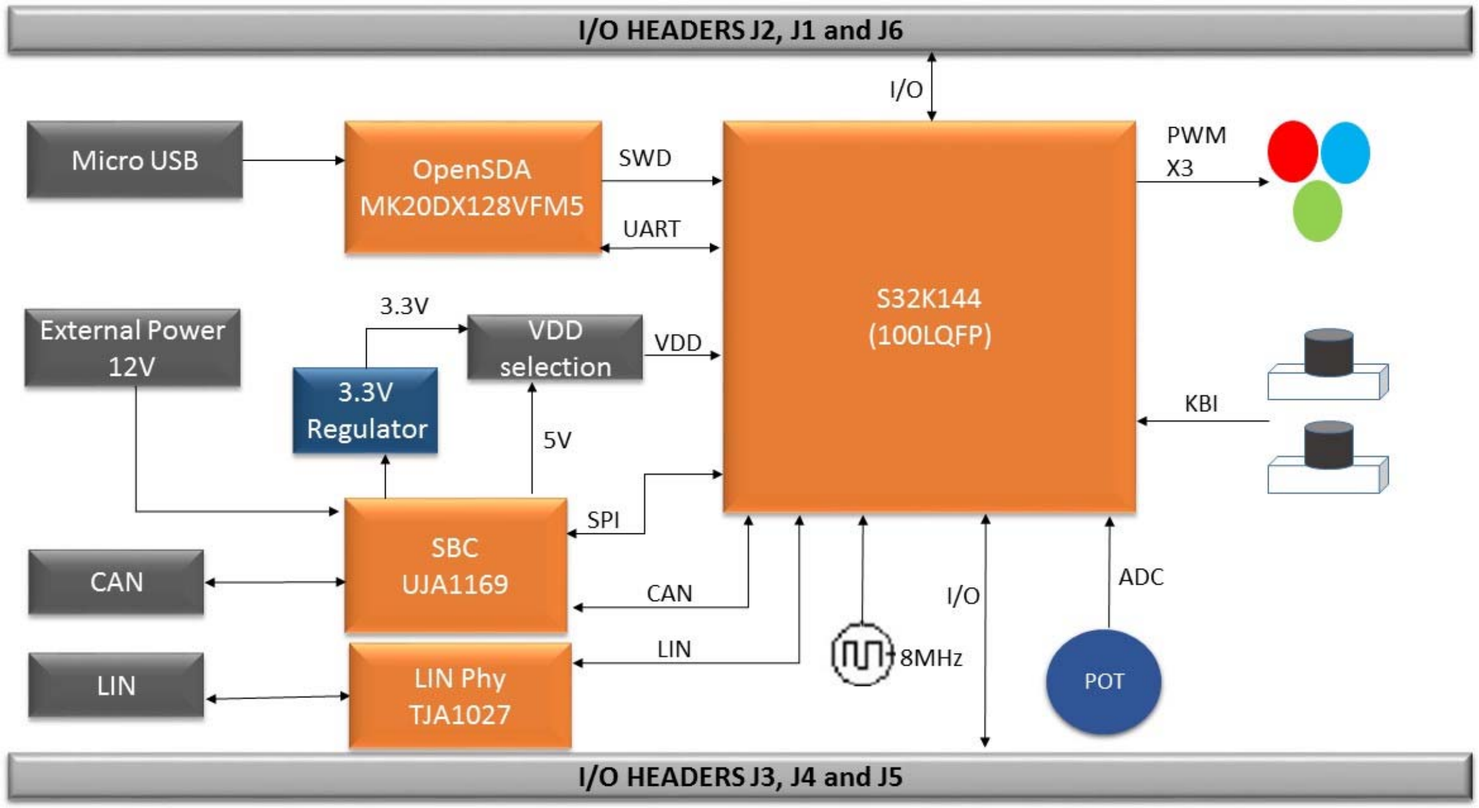
1. Unless Otherwise Specified:
   All resistors are in ohms, 1% and 5 %
   All capacitors are in uF, 10% , 20 % and 5%
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



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ICAP Classification:	FCP: ___ FIUO: X PUBI: ___	
Drawing Title:	**S32K144EVB-Q100**	
Page Title:	**Notes and Block Diagram**	
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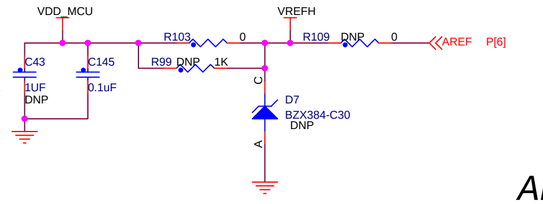
Note: VREFH can be selected from the following 3 options:
- Option 1(default): VREFH = VDD_MCU, place R103, dnp R99, R109 and D7.
- Option 2: VREFH = 3.0V from D7, place D7 and R99, dnp R103 and R109.
- Option 3: VREFH=AREF, place R109, dnp R103,R99 and D7.



AREF

VDD_MCU

C129 1UF DNP
C140 0.1uF
C131 1UF DNP
C141 0.1uF
C133 1UF DNP
C142 0.1uF
C146 1UF DNP
C143 0.1uF
C137 1UF DNP
C144 0.1uF
C147 1000PF DNP
C148 1000PF DNP

VREFH

11 VDDA
10 VDD1
38 VDD2
61 VDD3
87 VDD4
13 VREFL
12 VREFH

P[4,5] JTAG_TMS/SWD_DIO_PTA4 — R122 0 — P[6] PTA4

P[4,5,6] RST_TGTMCU_B

CAD Note: R125 and R126 POKA-YOKE: Place R125 and R126 with the same orientation and provide same airgap between the two resistors terminals in a square fashion

P[5] JTAG_TDO — R123 0 — P[6] PTA10

P[5] SBC_SCK — R124 0 — P[6] PTB14

P[5] SBC_MISO — R125 0 — P[6] PTB15

P[5] SBC_MOSI — R126 0 — P[6] PTB16

P[5] SBC_CS — R129 0 — P[6] PTB17

P[4,5] JTAG_TCLK/SWD_CLK — R127 0 — P[6] PTC4

P[5] JTAG_TDI — R128 0 — P[6] PTC5

P[4] UART_RX — R161 0 — P[6] PTC6

P[4] UART_TX — R162 0 — P[6] PTC7

P[6] BTN0 — R152 0 — P[6] PTC12

P[6] BTN1 — R153 0 — P[6] PTC13

P[6] ADC0_SE12 — R164 0 — P[6] PTC14

79	PTA0/ADC0_SE0/CMP0_IN0/FTM2_CH1/LPI2C0_SCLS/FXIO_D2/FTM2_QD_PHA/LPUART0_CTS/TRGMUX_OUT3	P[6] PTA0	
78	PTA1/ADC0_SE1/CMP0_IN1/FTM1_CH1/LPI2C0_SDAS/FXIO_D3/FTM1_QD_PHA/LPUART0_RTS/TRGMUX_OUT0	P[6] PTA1	
73	PTA2/ADC1_SE0/FTM3_CH0/LPI2C0_SDA/EWM_OUT/FXIO_D4/LPUART0_RX	P[6] PTA2	
72	PTA3/ADC1_SE1/FTM3_CH1/LPI2C0_SCL/EWM_IN/FXIO_D5/LPUART0_TX	P[6] PTA3	
98	PTA4/JTAG_TMS/SWD_DIO/CMP0_OUT/EWM_OUT		
97	PTA5/RESET/TCLK1		
58	PTA6/ADC0_SE2/FTM0_FLT1/LPSPI1_PCS1/LPUART1_CTS	P[6] PTA6	
57	PTA7/ADC0_SE3/FTM0_FLT2/RTC_CLKIN/LPUART1_RTS	P[6] PTA7	
100	PTA8/LPUART2_RX/LPSPI2_SOUT/FXIO_D6/FTM3_FLT3	P[6] PTA8	
99	PTA9/LPUART2_TX/LPSPI2_PCS0/FXIO_D7/FTM3_FLT2/FTM1_FLT3	P[6] PTA9	
92	PTA10/JTAG_TDO/NOETM_TRACE_SWO/FTM1_CH4/FXIO_D0		
91	PTA11/FTM1_CH5/FXIO_D1/CMP0_RRT	P[6] PTA11	
90	PTA12/FTM1_CH6/CAN1_RX/FTM2_QD_PHB	P[6] PTA12	
89	PTA13/FTM1_CH7/CAN1_TX/FTM2_QD_PHA	P[6] PTA13	
88	PTA14/FTM0_FLT0/FTM3_FLT1/EWM_IN/FTM1_FLT0	P[6] PTA14	
83	PTA15/ADC1_SE12/FTM1_CH2/LPSPI0_PCS3/LPSPI2_PCS3	P[6] PTA15	
82	PTA16/ADC1_SE13/FTM1_CH3/LPSPI1_PCS2	P[6] PTA16	
62	PTA17/FTM0_CH6/FTM3_FLT0/EWM_OUT	P[6] PTA17	
54	PTB0/ADC0_SE4/ADC1_SE14/LPUART0_RX/LPSPI0_PCS0/LPTMR0_ALT3/CAN0_RX	P[6] PTB0	
53	PTB1/ADC0_SE5/ADC1_SE15/LPUART0_TX/LPSPI0_SOUT/TCLK0/CAN0_TX	P[6] PTB1	
48	PTB2/ADC0_SE6/FTM1_CH0/LPSPI0_SCK/FTM1_QD_PHB/TRGMUX_IN3	P[6] PTB2	
47	PTB3/ADC0_SE7/FTM1_CH1/LPSPI0_SIN/FTM1_QD_PHA/TRGMUX_IN2	P[6] PTB3	
28	PTB4/FTM0_CH4/LPSPI0_SOUT/TRGMUX_IN1	P[6] PTB4	
27	PTB5/FTM0_CH5/LPSPI0_PCS1/LPSPI0_PCS0/CLKOUT/TRGMUX_IN0	P[6] PTB5	
16	PTB6/XTAL/LPI2C0_SDA	P[6] PTB6	
15	PTB7/EXTAL/LPI2C0_SCL	P[6] PTB7	
77	PTB8/FTM3_CH0	P[6] PTB8	
76	PTB9/FTM3_CH1/LPI2C0_SCLS	P[6] PTB9	
75	PTB10/FTM3_CH2/LPI2C0_SDAS	P[6] PTB10	
74	PTB11/FTM3_CH3/LPI2C0_HREQ	P[6] PTB11	
68	PTB12/ADC1_SE7/FTM0_CH0/FTM3_FLT2/CAN2_RX	P[6] PTB12	
67	PTB13/ADC1_SE8/ADC0_SE8/FTM0_CH1/FTM3_FLT1/CAN2_TX	P[6] PTB13	
66	PTB14/ADC1_SE9/ADC0_SE9/FTM0_CH2/LPSPI1_SCK		
65	PTB15/ADC1_SE14/FTM0_CH3/LPSPI1_SIN		
64	PTB16/ADC1_SE15/FTM0_CH4/LPSPI1_SOUT		
63	PTB17/FTM0_CH5/LPSPI1_PCS3		
40	PTC0/ADC0_SE8/FTM0_CH0/LPSPI2_SIN/FTM1_CH6	P[6] PTC0	
39	PTC1/ADC0_SE9/FTM0_CH1/LPSPI2_SOUT/FTM1_CH7	P[6] PTC1	
30	PTC2/ADC0_SE10/CMP0_IN5/FTM0_CH2/CAN0_RX/LPUART0_RX	P[6] PTC2	
29	PTC3/ADC0_SE11/CMP0_IN4/FTM0_CH3/CAN0_TX/LPUART0_TX	P[6] PTC3	
96	PTC4/JTAG_TCLK/SWD_CLK/CMP0_IN2/FTM1_CH0/RTC_CLKOUT/EWM_IN/FTM1_QD_PHB		
95	PTC5/JTAG_TDI/FTM2_CH0/RTC_CLKOUT/FTM2_QD_PHB		
81	PTC6/ADC1_SE4/LPUART1_RX/CAN1_RX/FTM3_CH2/FTM1_QD_PHB		
80	PTC7/ADC1_SE5/LPUART1_TX/CAN1_TX/FTM3_CH3/FTM1_QD_PHA		
56	PTC8/LPUART1_RX/FTM1_FLT0/LPUART0_CTS	P[6] PTC8	
55	PTC9/LPUART1_TX/FTM1_FLT1/LPUART0_RTS	P[6] PTC9	
52	PTC10/FTM3_CH4/TRGMUX_IN11	P[6] PTC10	
51	PTC11/FTM3_CH5/TRGMUX_IN10	P[6] PTC11	
50	PTC12/FTM3_CH6/FTM2_CH6/LPUART2_CTS		
49	PTC13/FTM3_CH7/FTM2_CH7/LPUART2_RTS		
46	PTC14/ADC0_SE12/FTM1_CH2/LPSPI2_PCS0/TRGMUX_IN9		
45	PTC15/ADC0_SE13/FTM1_CH3/LPSPI2_SCK/TRGMUX_IN8		
44	PTC16/ADC0_SE14/FTM1_FLT2/CAN2_RX		
43	PTC17/ADC0_SE15/FTM1_FLT3/CAN2_TX		

14 VSS1
37 VSS2
60 VSS3
86 VSS4

U17
PS32K144HFT0VLLT

4	PTD0/FTM0_CH2/LPSPI1_SCK/FTM2_CH0/FXIO_D0/TRGMUX_OUT1	P[6] PTD0	R156 0 — RGB_BLUE P[6]
3	PTD1/FTM0_CH3/LPSPI1_SIN/FTM2_CH1/FXIO_D1/TRGMUX_OUT2	P[6] PTD1	R130 0 — LIN_RX P[5]
71	PTD2/ADC1_SE2/FTM3_CH4/LPSPI1_SOUT/FXIO_D4/FXIO_D6/TRGMUX_IN5	P[6] PTD2	
70	PTD3/ADC1_SE3/FTM3_CH5/LPSPI1_PCS0/FXIO_D5/FXIO_D7/TRGMUX_IN4/NMI	P[6] PTD3	R131 0 — LIN_TX P[5]
69	PTD4/ADC1_SE6/FTM0_FLT3/FTM3_FLT3	P[6] PTD4	
33	PTD5/FTM2_CH3/LPTMR0_ALT2/FTM2_FLT1/TRGMUX_IN7	P[6] PTD5	
32	PTD6/CMP0_IN7/LPUART2_RX/FTM2_FLT2		
31	PTD7/CMP0_IN6/LPUART2_TX/FTM2_FLT3		
42	PTD8/FTM2_FLT2/FTM1_CH4	P[6] PTD8	
41	PTD9/FTM2_FLT3/FTM1_CH5	P[6] PTD9	
36	PTD10/FTM2_CH0/FTM2_QD_PHB	P[6] PTD10	
35	PTD11/FTM2_CH1/FTM2_QD_PHA/LPUART2_CTS	P[6] PTD11	
34	PTD12/FTM2_CH2/LPUART2_RTS	P[6] PTD12	
25	PTD13/FTM2_CH4/LPUART1_RX/RTC_CLKOUT	P[6] PTD13	R154 0 — RGB_RED P[6]
24	PTD14/FTM2_CH5/LPUART1_TX/CLKOUT	P[6] PTD14	
22	PTD15/FTM0_CH0/LPSPI0_SCK		R155 0 — RGB_GREEN P[6]
21	PTD16/FTM0_CH1/LPSPI0_SIN/CMP0_RRT		PTD16 P[6]
20	PTD17/FTM0_FLT2/LPUART2_RX	P[6] PTD17	
94	PTE0/LPSPI0_SCK/TCLK1/LPSPI1_SOUT/FTM1_FLT2	P[6] PTE0	
93	PTE1/LPSPI0_SIN/LPI2C0_HREQ/LPSPI1_PCS0/FTM1_FLT1	P[6] PTE1	
85	PTE2/ADC1_SE10/LPSPI0_SOUT/LPTMR0_ALT3/FTM3_CH6/LPUART1_CTS	P[6] PTE2	R137 0 — SBC_CAN_RX P[5]
18	PTE3/FTM0_FLT0/LPUART2_RTS/FTM2_FLT0/TRGMUX_IN6/CMP0_OUT	P[6] PTE3	
9	PTE4/FTM2_QD_PHB/FTM2_CH2/CAN0_RX/FXIO_D6/EWM_OUT		PTE4 P[6]
8	PTE5/TCLK2/FTM2_QD_PHA/FTM2_CH3/CAN0_TX/FXIO_D7/EWM_IN		R136 0 — SBC_CAN_TX P[5]
84	PTE6/ADC1_SE11/LPSPI0_PCS2/FTM3_CH7/LPUART1_RTS		PTE5 P[6]
59		P[6] PTE6	
26	PTE7/FTM0_CH7/FTM3_FLT0	P[6] PTE7	
23	PTE8/CMP0_IN3/FTM0_CH6	P[6] PTE8	
6	PTE9/FTM0_CH7/LPUART2_CTS		R529 0 — LIN_SLP P[5]
5	PTE10/CLKOUT/LPSPI2_PCS1/FTM2_CH4/FXIO_D4/TRGMUX_OUT4	P[6] PTE10	PTE9 P[6]
19	PTE11/LPSPI2_PCS0/LPTMR0_ALT1/FTM2_CH5/FXIO_D5/TRGMUX_OUT5	P[6] PTE11	
7	PTE12/FTM0_FLT3/LPUART2_TX		PTE12 P[6]
17	PTE13/LPSPI2_PCS2/FTM2_FLT0		R532 0 — SBC_LIMP P[5]
2	PTE14/FTM0_FLT1/FTM2_FLT1	P[6] PTE14	PTE13 P[6]
1	PTE15/LPUART1_CTS/LPSPI2_SCK/FTM2_CH6/FXIO_D2/TRGMUX_OUT6	P[6] PTE15	
	PTE16/LPUART1_RTS/LPSPI2_SIN/FTM2_CH7/FXIO_D3/TRGMUX_OUT7	P[6] PTE16	

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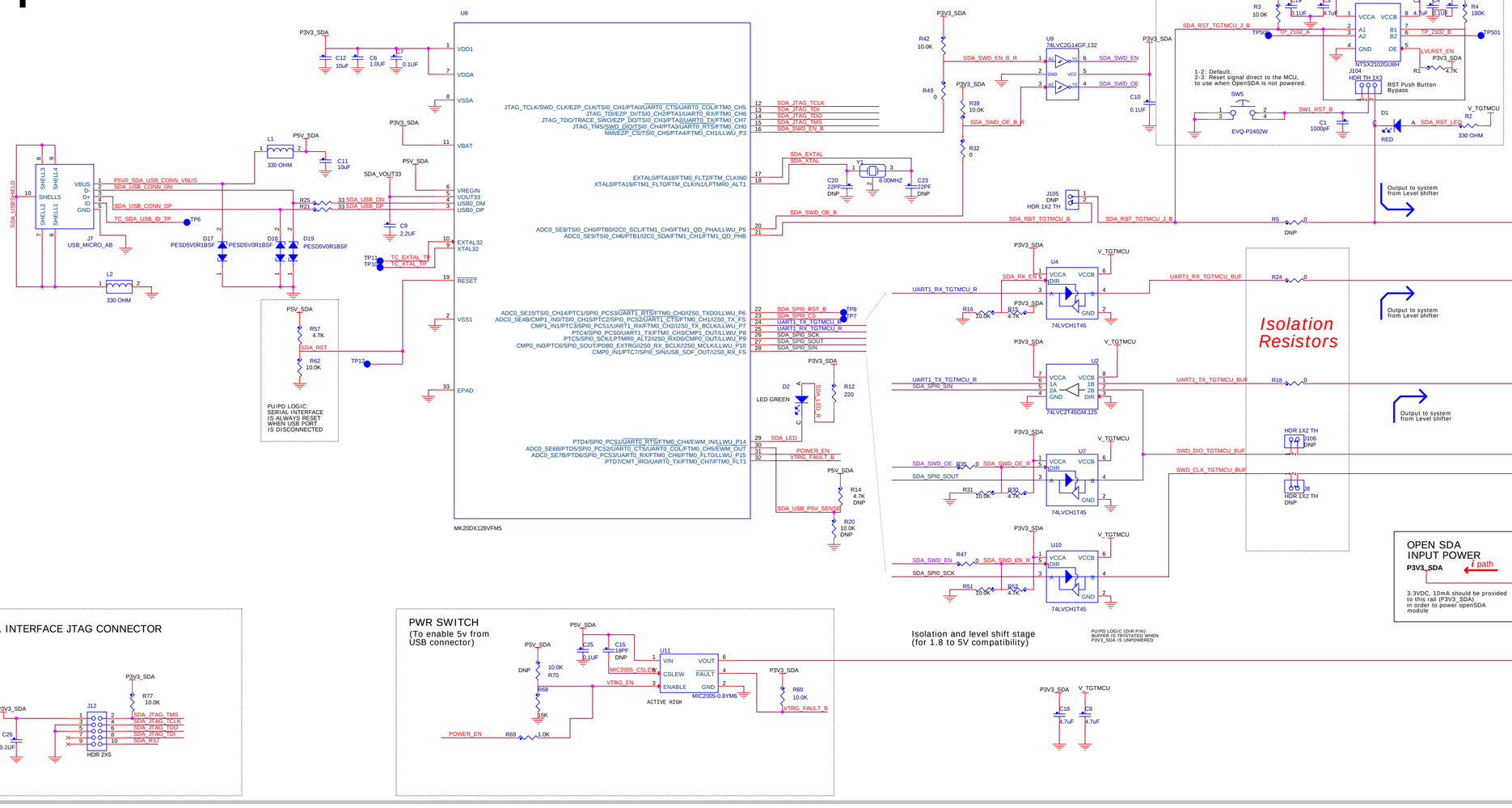
OpenSDA Interface



OpenSDA INTERFACE JTAG CONNECTOR

PWR SWITCH
(To enable 5v from USB connector)

{For enablement purposes only}

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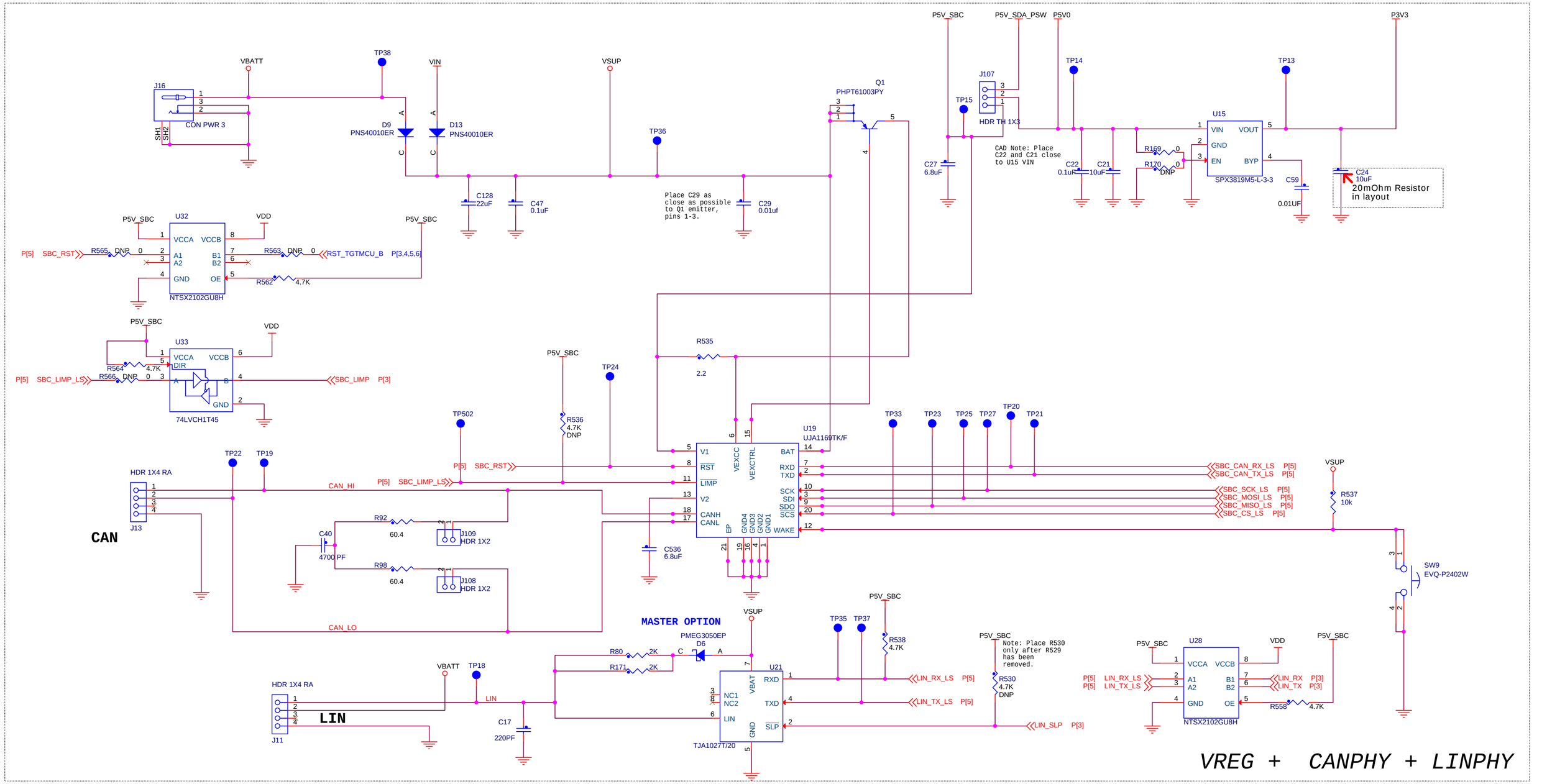

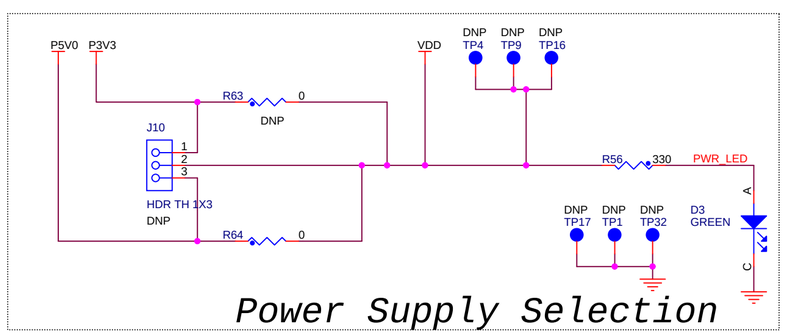

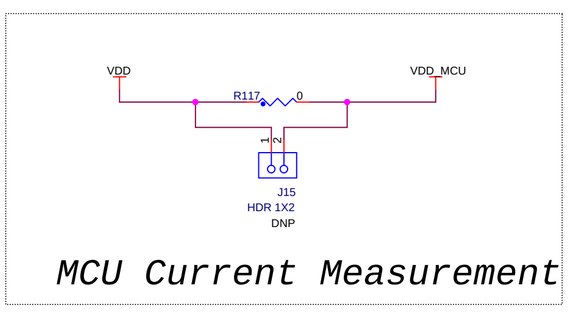

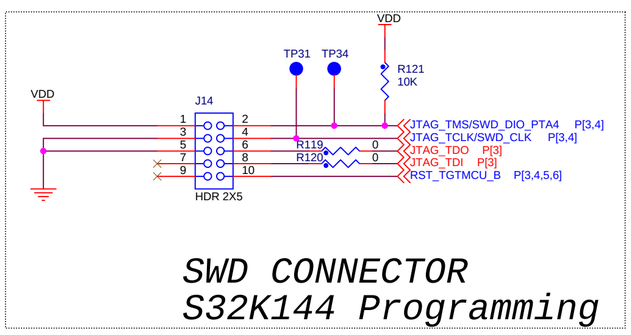

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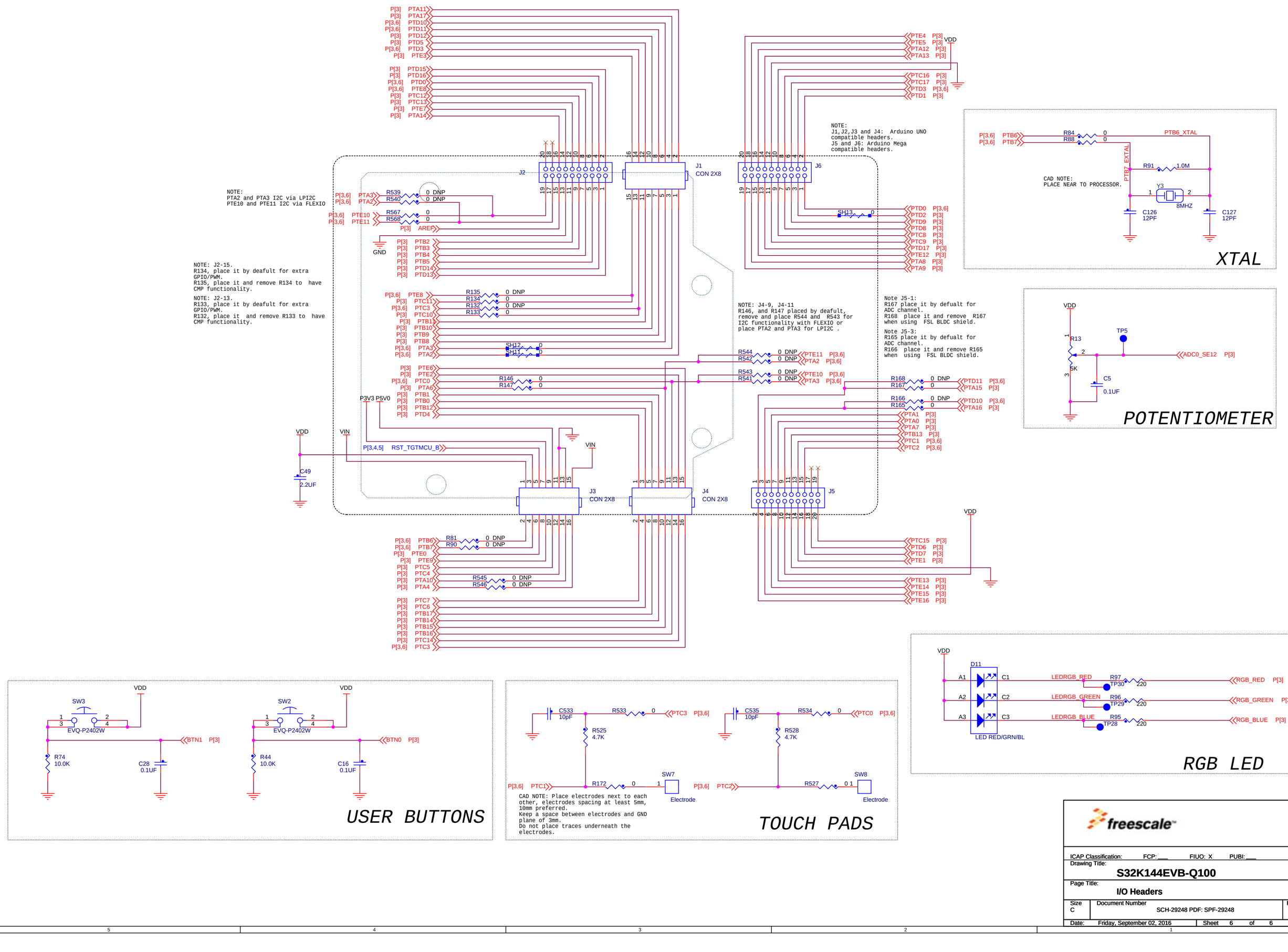
J1
CON 2X8
J2
J3
CON 2X8
J4
CON 2X8
J5
J6
NOTE:
PTA2 and PTA3 I2C via LPI2C
PTE10 and PTE11 I2C via FLEXIO
NOTE: J2-15.
R134, place it by deafult for extra GPIO/PWM.
R135, place it and remove R134 to have CMP functionality.
NOTE: J2-13.
R133, place it by deafult for extra GPIO/PWM.
R132, place it and remove R133 to have CMP functionality.
NOTE:
J1,J2,J3 and J4: Arduino UNO compatible headers.
J5 and J6: Arduino Mega compatible headers.
NOTE: J4-9, J4-11
R146, and R147 placed by deafult, remove and place R544 and R543 for I2C functionality with FLEXIO or place PTA2 and PTA3 for LPI2C .
Note J5-1:
R167 place it by defualt for ADC channel.
R168 place it and remove R167 when using FSL BLDC shield.
Note J5-3:
R165 place it by defualt for ADC channel.
R166 place it and remove R165 when using FSL BLDC shield.
VDD
VIN
P3V3 P5V0
C49
2.2UF
P[3,4,5] RST_TGTMCU_B
R539 0 DNP
R540 0 DNP
R567 0
R568 0
R135 0 DNP
R134 0
R132 0 DNP
R133 0
SH12 0
SH11 0
R146 0
R147 0
R544 0 DNP
R542 0 DNP
R543 0 DNP
R541 0 DNP
R168 0 DNP
R167 0
R166 0 DNP
R165 0
R81 0 DNP
R90 0 DNP
R545 0 DNP
R546 0 DNP
SH13 0
XTAL
R84 0
R88 0
PTB6_XTAL
PTB7_EXTAL
R91 1.0M
Y3
8MHZ
C126 12PF
C127 12PF
CAD NOTE:
PLACE NEAR TO PROCESSOR.
POTENTIOMETER
R13 5K
TP5
C5 0.1UF
ADC0_SE12 P[3]
USER BUTTONS
SW3
SW2
EVQ-P2402W
R74 10.0K
C28 0.1UF
R44 10.0K
C16 0.1UF
BTN1 P[3]
BTN0 P[3]
TOUCH PADS
C533 10pF
R533 0
R525 4.7K
R172 0
SW7
Electrode
C535 10pF
R534 0
R528 4.7K
R527 0
SW8
Electrode
CAD NOTE: Place electrodes next to each other, electrodes spacing at least 5mm, 10mm preferred.
Keep a space between electrodes and GND plane of 3mm.
Do not place traces underneath the electrodes.
RGB LED
D11
LED RED/GRN/BL
LEDRGB_RED
LEDRGB_GREEN
LEDRGB_BLUE
R97 220
R96 220
R95 220
TP30
TP29
TP28
RGB_RED P[3]
RGB_GREEN P[3]
RGB_BLUE P[3]
freescale
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