Description

The ZNRG2061 is a smart system-on-chip for arc-fault detection in photovoltaic (PV) solar power systems. Its trainable algorithm delivers safe and reliable signaling of arc-faults while tolerating typical noise patterns present in solar power systems.

The algorithm continuously monitors the photovoltaic DC current and observes any current fluctuation, ultimately performing a fast Fourier transform (FFT) analysis. The frequency spectrum is compared to a previously memorized baseline. If the signature of an arc-fault is detected, a failure event is generated. To prevent nuisance tripping, the baseline and other criteria are determined with a training procedure. Training is initiated via the graphical user interface (GUI) configuration software.

In addition to a current transformer, which also acts as galvanic isolator from the primary high voltage, the ZNRG2061 system-on-chip requires only a few external components. It contains all necessary data acquisition, signal conditioning, and DSP functions to provide reliable arc-fault signaling.

Self-diagnosis is performed continuously, ensuring that the device operates safely at all times.

To simplify design-in and accelerate future systems UL listings, the ZNRG2061 is designed in compliance with UL 1699B and recognized according to UL 1998.

Typical Applications

Integrated arc-fault detection in

- PV solar power inverters
- Combiner boxes
- DC optimizers
- Stand-alone arc-fault circuit interrupters (AFCI)

Physical Characteristics

- Operating temperature -40°C to 85°C
- Supply voltage 6V to 24V
- 32-PQFN package $5 \times 5 \times 0.9$ mm
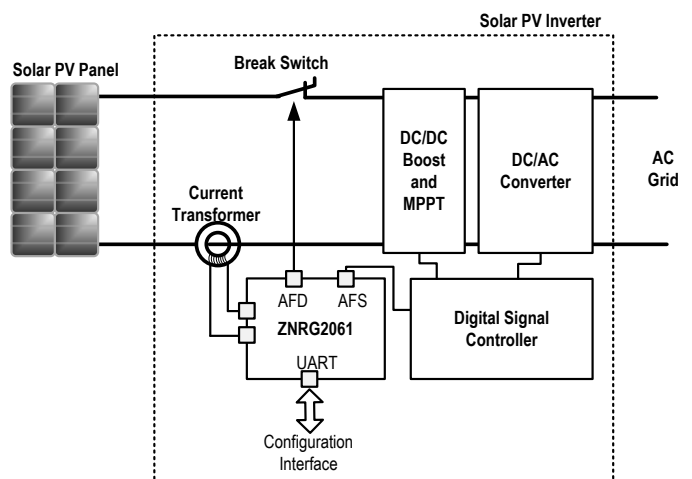
Available Support

- Evaluation Kit
- Application Notes

Features

- Complete DC line arc-fault detection solution in a single IC
- UL 1699B design compliant and UL 1988 recognized
- Advanced signal processing via FFT
- Small footprint package 5×5 mm – compact package with only a few external components significantly contributes to optimized application's bill-of-materials (BOM) and circuit board area utilization
- Smart automated, trainable algorithm empowers system customization and adaptation to avoid nuisance tripping
- Signaling with a latched (static) and non-latched (dynamic) digital output
- Wide supply voltage range
- Built-in self-test
- Ability to interface with pseudo arc signal
- Automatic gain adjustment
- Fault clear from annunciator (via communication)
- UL recognition simplifies UL listing of the end product

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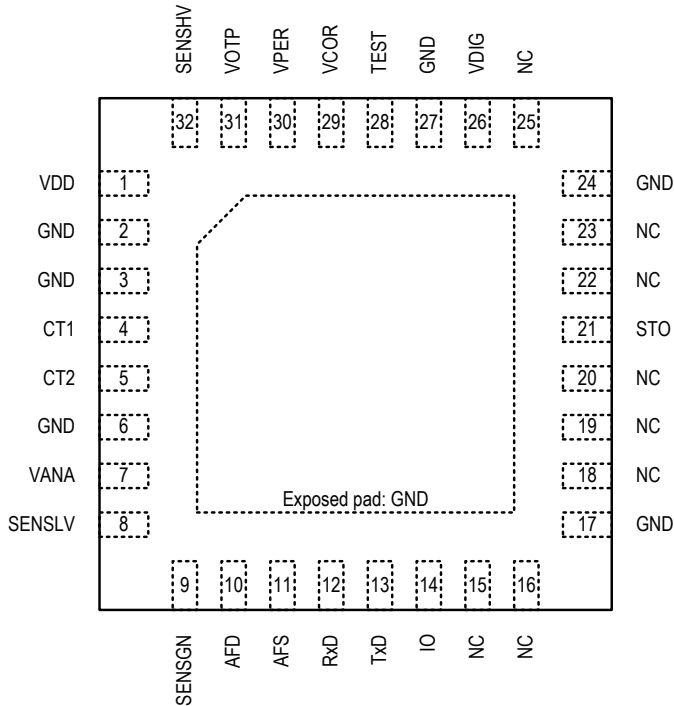
2. Pin Descriptions

Table 1.   Pin Descriptions

Number	Name	Type	Description
1	VDD	Supply	Supply voltage.
2	GND	Ground	Analog/digital ground.
3	GND	Ground	Analog/digital ground.
4	CT1	Analog Input	Differential voltage input.
5	CT2	Analog Input	Differential voltage input.
6	GND	Ground	Analog/digital ground.
7	VANA	Analog Output	VANA regulator output; external capacitance 470nF to board GND.
8	SENSLV	Analog Input	Voltage sensing input.
9	SENSGN	Analog Input	Voltage sensing input.
10	AFD	Digital Output	Arc-fault detected; latched output.
11	AFS	Digital Output	Arc feature signal; non-latched output.

Number	Name	Type	Description
12	RxD	Output	RxD. Pull-up to VPER via 4.7kΩ resistor.
13	TxD	Input	TxD. Pull-down to GND via 4.7kΩ resistor.
14	IO	Unused	Digital output.
15	NC	Unused	Unused. Pull up to VPER via 4.7kΩ resistor.
16	NC	Unused	Unused. Pull up to VPER via 4.7kΩ resistor.
17	GND	Ground	Analog/digital ground.
18	NC	Unused	Unused. Pull up to VPER via 4.7kΩ resistor.
19	NC	Unused	Unused. Pull up to VPER via 4.7kΩ resistor.
20	NC	Unused	Unused. Pull up to VPER via 4.7kΩ resistor.
21	STO	Digital Output	Safety trouble output.
22, 23	NC	Unused	Unused. Leave unconnected.
24	GND	Ground	Analog/digital ground.
25	NC	Unused	Unused. Leave unconnected.
26	VDIG	Analog Output	VDIG regulator output; external capacitance 10nF to board GND.
27	GND	Ground	Analog/digital ground.
28	TEST	Digital IO	Unused. Leave unconnected.
29	VCOR	Analog Output	VCOR regulator output; external capacitance 2.2µF to board GND.
30	VPER	Analog Output	VPER regulator output; external capacitance 2.2µF to board GND.
31	VOTP	Supply	OTP supply voltage input.
32	SENSHV	Analog Input	Voltage sensing input.
Exposed Pad	GND	Ground	Analog/digital ground.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the ZNRG2061 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability.

Table 2.   ZNRG2061 Absolute Maximum Ratings

No	Parameter	Symbol	Conditions	Min	Max	Unit
3.1.1.	External power supply	V_{DD}		V_{GND} - 0.3	40	V
3.1.2.	Current sensing, CT1 pin	V_{CT1}		V_{GND} - 0.3	V_{ANA} + 0.3	V
3.1.3.	Current sensing, CT2 pin	V_{CT2}		V_{GND} - 0.3	V_{ANA} + 0.3	V
3.1.4.	Voltage sensing, SENSHV pin	V_{SENSHV}		0	33	V
3.1.5.	Voltage sensing, SENSLV pin	V_{SENSLV}		V_{GND} - 0.3	V_{ANA} + 0.3	V
3.1.6.	Voltage sensing, SENSGN	V_{SENSGN}		V_{GND} - 0.3	V_{ANA} + 0.3	V
3.1.7.	AFD pin	V_{AFD}		V_{GND} - 0.3	V_{PER} + 0.3	V
3.1.8.	AFS pin	V_{AFS}		V_{GND} - 0.3	V_{PER} + 0.3	V
3.1.9.	RxD pin	V_{RxD}		V_{GND} - 0.3	V_{PER} + 0.3	V
3.1.10.	TxD pin	V_{TxD}		V_{GND} - 0.3	V_{PER} + 0.3	V
3.1.11.	IO pin	V_{IO}	Reserved	V_{GND} - 0.3	V_{PER} + 0.3	V
3.1.12.	Ambient temperature under bias	T_A			125	°C
3.1.13.	Junction temperature	T_j			135	°C
3.1.14.	Storage temperature	T_S		-50	125	°C

4. Recommended Operating Conditions

Table 3.   ZNRG2061 Recommended Operating Conditions

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
4.1.1.	Operating temperature range	T_A	Ambient, RTHP = 35K/W	-40		85	°C
4.1.2.	Supply voltage at VDD pin	V_{DD}		6		24	V
4.1.3.	Digital input voltage LOW	V_{IL}		0		$0.3 * V_{PER}$	V
4.1.4.	Digital input voltage HIGH	V_{IH}		$0.7 * V_{PER}$		V_{PER}	V

5. Electrical Characteristics

Table 4.   ZNRG2061 Electrical Characteristics

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply							
5.1.1.	Average supply current at VDD	I_{DD_avg}			20		mA
5.1.2.	Average power dissipation	P_{DD_avg}			240		mW
5.1.3.	Internal analog power supply voltage	V_{ANA}		2.4	2.5	2.6	V
5.1.4.	Internal digital and RAM power supply voltage	V_{DIG}		1.62	1.8	1.98	V
5.1.5.	Internal power supply voltage for microcontroller unit (MCU) core	V_{COR}		1.62	1.8	1.98	V
5.1.6.	Internal power supply voltage (periphery)	V_{PER}		2.97	3.3	3.63	V
Primary ADC Channel							
5.2.1.	Input signal range [a]	$Range_{CT}$		-300		300	mV
5.2.2.	Input leakage current [a]	I_{LEAK_C}	T_A = 25°C	-3		+3	nA
Auxiliary ADC Channel							
5.3.1.	Input signal range SENSHV [a]	V_{SENSHV}		0		28.8	V
5.3.2.	Input signal range SENSLV [a]	V_{SENSLV}		V_{SENSGN}		V_{SENSGN} + 1.2	V
5.3.3.	Input signal range SENSGN [a]	V_{SENSGN}		0		1.2	V
Power-on Reset (POR)							
5.4.1.	Power-on reset	V_{PORB}	At V_{DD}	2.75	3.0	3.6	V
5.4.2.	Power-on-reset hysteresis	$Hyst_{PORB}$	At V_{DD}		300		mV
5.4.3.	Low-voltage flag	low_voltage	At V_{DD}	1.8	2.0	2.3	V
5.4.4.	V_{VPER} high [a]	VPER_high	At V_{DD}	3.9	4.05	4.2	V
5.4.5.	V_{VPER} high hysteresis [a]	$Hyst_{VPER\_high}$	At V_{DD}		400		mV
Oscillator							
5.5.1.	Frequency	f_{HPO}			20		MHz
5.5.2.	Accuracy (including temperature drift) [a]			-1		1	%

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Microcontroller Platform							
5.6.1.	MCU start-up time after POR[a]				80		µs
5.6.2.	MCU start-up time after Standby Mode wake up[a]				1		µs
Functional Timing							
5.7.1.	AFD maximum trip time[b]	t_{MTT}				800	ms
5.7.2.	AFD complete calculation time	t_{CCT}				700	ms
5.7.3.	AFD single arc calculation loop	t_{SACL}	Not in command mode			40	ms
5.7.4.	Start-up built-in self-test	t_{SBIST}				200	ms
5.7.5.	Communication frame response	t_{CFR}	Confirm with product valid			40	ms
5.7.6.	Transport protocol timeout	t_{TPT}				100	ms
5.7.7.	Command mode timeout	t_{CMT}				5	min
Electrostatic Discharge							
5.8.1.	ESD on system level[c]		IEC61000-4-2			±2	kV
5.8.2.	ESD, SENSHV on system level		IEC61000-4-2			±2	kV

[a] Not tested in production test. Given by design and/or characterization.

[b] Combined system of AFD + external relay.

[c] With external protection diode GSOT36.

# 6. Theory of Operation

6.1 Overview

The DC current of solar installations contains specific noise patterns, some of which are due to potentially dangerous arcing events, while others have no potentially dangerous consequence. The latter noise originates from typical sources like inverters, maximum power point tracker (MPPT) optimization, changing exposure of solar panels to the sun, and load changes at the output of the inverter, which are all multiplied by parasitic capacitive and inductive components of wiring and connectors.

The main current is sensed through a current transformer that also provides galvanic isolation. The number of turns on the current transformer must be chosen such that the maximum AC output voltage is lower than ±300mVp. The signal from the current transformer is fed into an external low-pass filter before reaching the input pins of the IC. The cutoff frequency of the filter should be 16kHz.

The primary current is subsequently pre-amplified and converted into a digital bit stream by a 24-bit sigma-delta analog-to-digital converter (ADC). The time domain signal is then fed into an FFT block that provides a representation of the primary current in the frequency domain. A microcontroller analyzes the FFT data for both level and duration of selected spectral frequency bands to provide reliable detection of potential hazardous arc conditions. There is a trade-off between the fastest possible detection time and achieving minimal probability of false positive alarms. UL's 1699B standard was used as a reference for detection time. The ZNRG2061 is designed such that the detector output reacts 100 milliseconds faster than the limits in the UL standard, leaving sufficient time for the customer's system to react to the arc detector signal.

Upon detecting an arc fault, the digital output pin AFD is set with a built-in latch function. AFD can be reset only by interrupting the supply (power-on reset). The alternative output signal AFS digitally indicates whenever arc-like features have been detected in the current flow. This output resets itself as soon as the suspicious current characteristics have disappeared. See section 7 for details.

Figure 2.   Functional Description Diagram

Time Domain ⟶   Frequency Domain
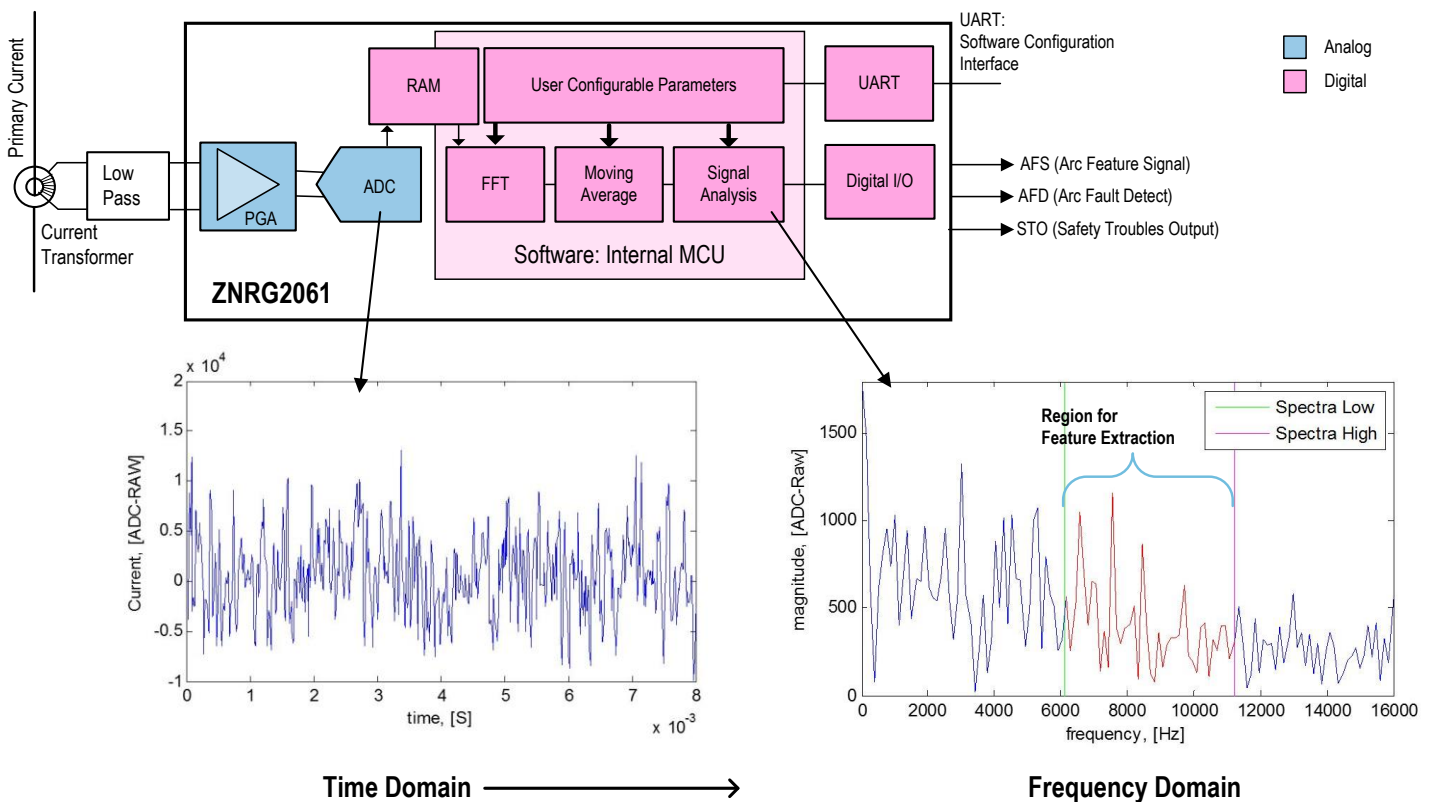
6.1.1   Arc Power

The power of the arc determines the maximum tripping time allowed. The higher the arc power, the shorter the allowed time before the arc detection alarm output is set. The tripping time is a sum of the detection time from the ZNRG2061 and the time for the external circuit (relay) to react accordingly.

Table 5.   Tripping Time vs. Arc Power

Note: The following specifications are from Underwriters Laboratory's document *UL 1699B: Outline of Investigation for Photovoltaic (PV) DC Arc-Fault Circuit Protection.*

Arc Power (Watts)	300W	500W	650W	900W
Maximum tripping time (sec)	2	1.5	1.2	0.8

Since power is not measured, ZNRG2061 will respond within less than 700ms, meeting the worst case of 800ms system's margin, as required by UL.

6.1.2   Selecting Spectral Frequencies for Analysis

The user can select a particular spectral range of interest. The range is defined by two frequencies, LOW and HIGH. All of the spectral bins between these two frequencies are the only frequencies selected for further analysis. Note that the choice of the low/high frequency is not random; they must correspond to existing frequencies in the discrete spectra. Alternatively, they can be defined as the index number from 0 to 127 in a FFT of 256 frequency bins. Refer to the *ZNRG2061 AFD GUI User Manual*.

6.1.3   Post Filter

A post filter is implemented in order to avoid false triggering by spikes, noises, or short time relay effects. The post filter counts the number of consecutively detected arcs. This filter defines the minimum duration of an arc before it triggers the "arc detected" alarm output. The post filter value is compared against a pre-programmed threshold.
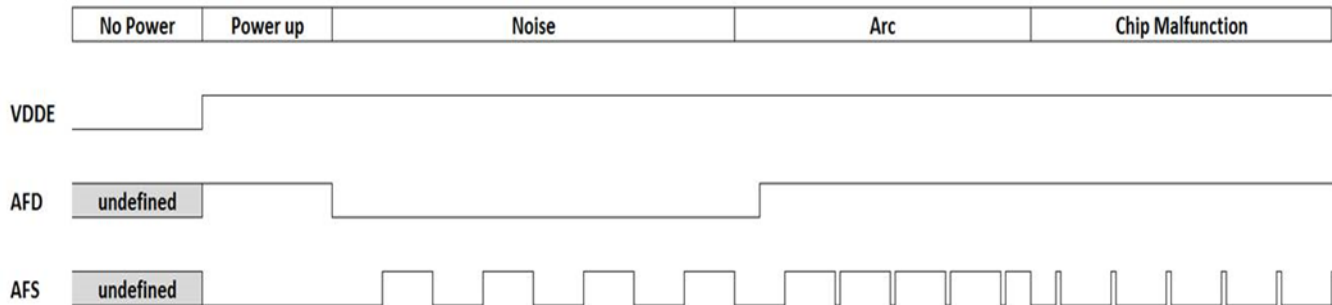
6.1.4   Training Sequence

Refer to the *ZNRG2061 Functional Safety Manual* for the training sequence.

7. Output Signal Description

Figure 3 illustrates the signal behavior for the AFD and AFS signals under various conditions.

Figure 3. Output Signal Diagram

7.1 AFD – Arc Fault Detector

AFD is a static pin, which can be used to directly control a DC break switch. If an arc is detected, the AFD output level goes high.

If the built-in self-test (BIST) detects a malfunction, the AFD will be set to high as well. In the event of a malfunction, the device might attempt to recover automatically. However, the AFD will be set to HIGH if the final recovery attempt is not successful.

Once set, the AFD pin is latched (permanently set) HIGH and the device will not reset the output by itself. Only a power off/on cycle or a GUI command can reset this pin.

7.2 AFS – Arc Feature Signal

AFS is a dynamic pin, which outputs a signal similar to pulse width modulation (PWM). The information on AFS is defined by the width (in ms) of the positive pulse width. It has three clearly distinguishable states:

- PWMe: Error and/or failure   Pulse width < 10ms (or permanent 0V) or pulse width > 40ms (or permanent 3.3V)
- PWMn: There is no ARC and no failure   Pulse width of 16ms to 18ms
- PWMa: There is ARC and/or failure   Pulse width of 32ms to 34ms

This pin can be used for the following purposes:

- The AFS can serve as secondary validation pin. This can be implemented on a system level. The AFS pin is made to be complementary (dynamic vs. static) to the AFD pin, so that there is an opportunity for detecting a complete component failure.
- The AFS output can be used to indicate an error condition as part of its normal functions. It will stop its PWM-like pulses if a malfunction is detected. Thus a small external circuit (watchdog for example) can be used to display the state on an LED.

Example: In the unlikely case of a ZNRG2061 malfunction during an arcing event, the AFD might not be triggered. In this case, the AFS pin will remain static HIGH or LOW (PWM 0% or 100%) thus indicating the error.

8. Application Circuit

The typical application circuits in Figure 4 and Figure 5 are implemented in the ZNRG2061 Evaluation Board included in the ZNRG2061 Evaluation Kit (see section 14).

Figure 4.   Input Circuit Schematic
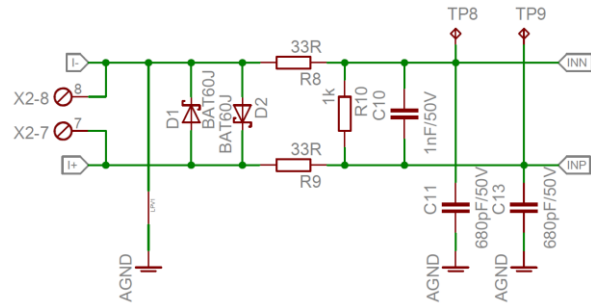
Input terminals I+ and I- are directly fed from the current transformer. The output voltage of the current transformer is limited by D1 and D2 to their forward voltage drop of 0.32V maximum. The filter formed by R8, R9, R10 and C10, C11, C13 has a cut off frequency of 16kHz.

Figure 5.   Main Application Schematic
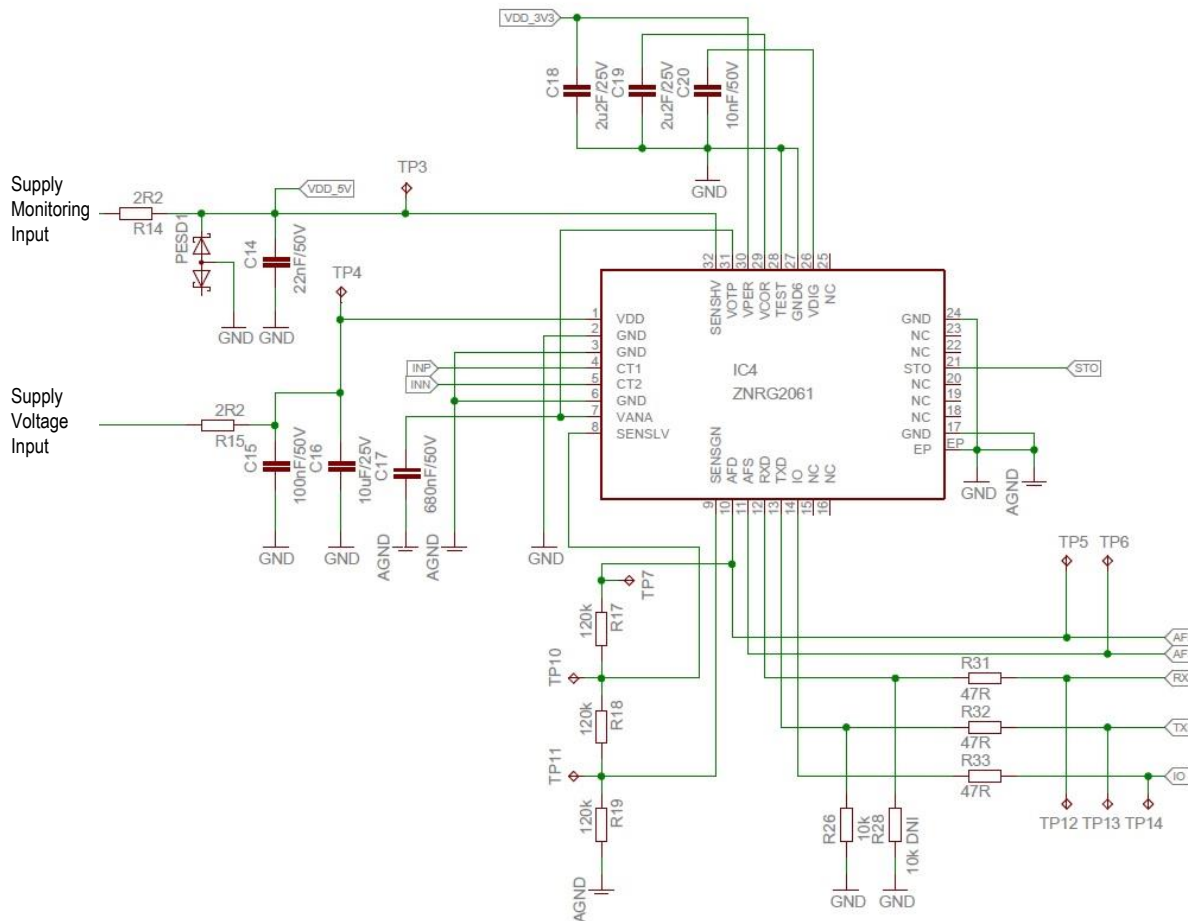
For more details on interfacing with a pseudo arc signal, refer to the *ZNRG2061 Evaluation Kit User Manual*.

9. Fail Safe Operation

Self-diagnostic and supervisory software are implemented within ZNRG2061. These functions rely on the close cooperation between the smart built in self-test (BIST) software and the hardware diagnostics block. The primary role of the BIST is to detect a malfunction occurring during run-time. Secondarily, the BIST will place the device into the Safe State and properly signal the malfunction if a malfunction is detected.

In normal operation mode, the device state is monitored using the AFD and AFS pins. However, the STO pin can be monitored in cases where high reliability is needed.

The STO (Safety Troubles Output) can be used as an indication of a severe malfunction. This output will be driven to HIGH when the reset of the system has finished. From this point forward, the STO pin will remain HIGH until the power down of the device. Any falling slope of the STO (high to low transition) is an indication of a malfunction occurring.

This enables the two following distinguishable situations:

- Low pulse. This indicates that the device has detected a failure and has gone into the Safe State. Functionality after this point might not be available.
- Permanent LOW. Complete device destruction might have occurred. If a very high level of reliability is needed from the system, the supply voltage can be monitored (by an external MCU for example) as well. In this case, a LOW level at the STO pin and a high supply is an indication of this hypothetical case.

In the event of a hardware malfunction, the normal outputs might not be functioning properly. The STO pin can be very useful in the case of a double fault of the AFD and the AFS outputs.
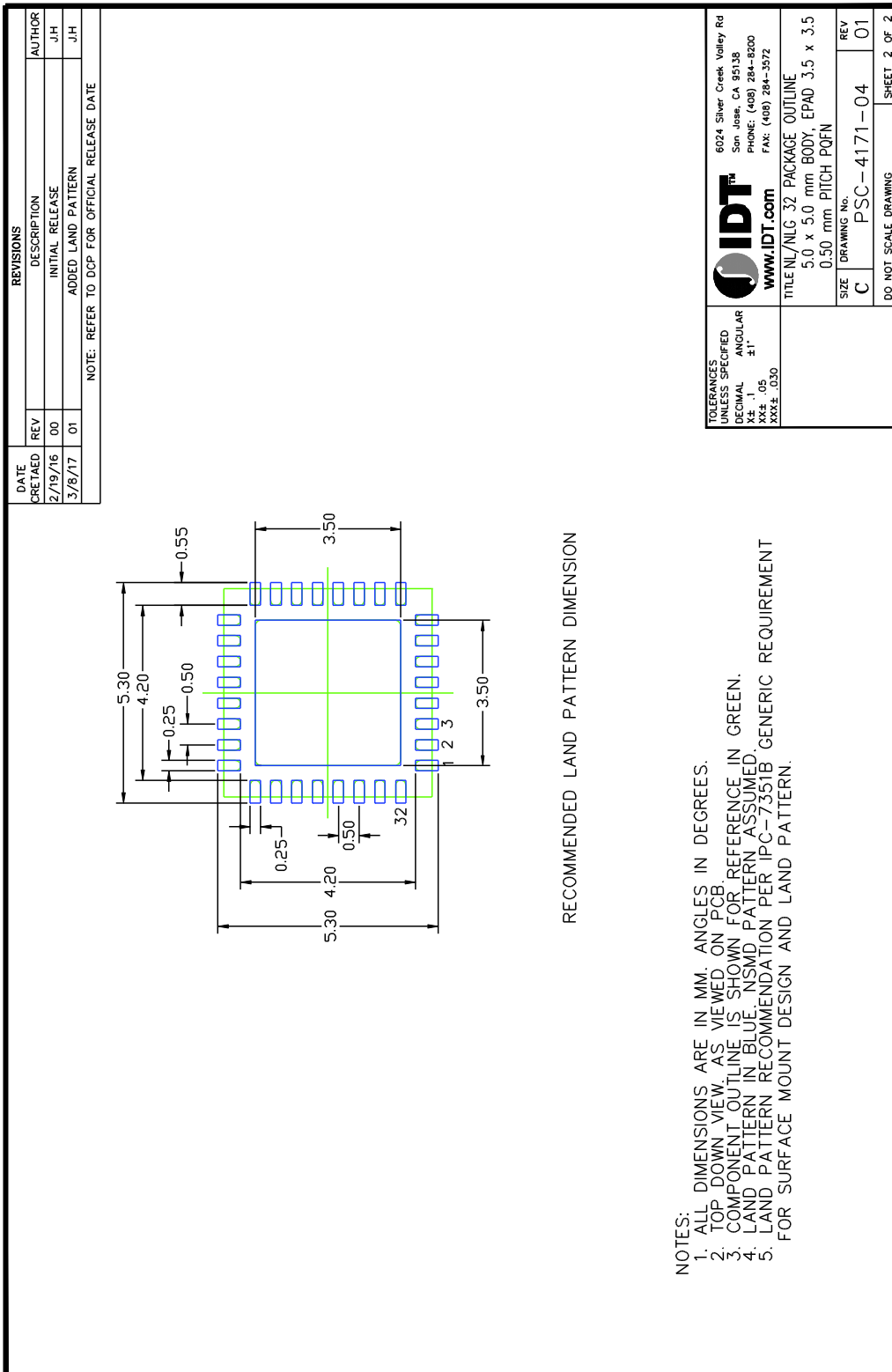
10. Package Drawing

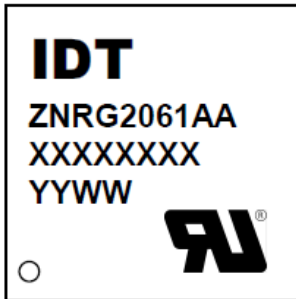**Figure 6.   32-PQFN Package Drawing of the ZNRG2061**
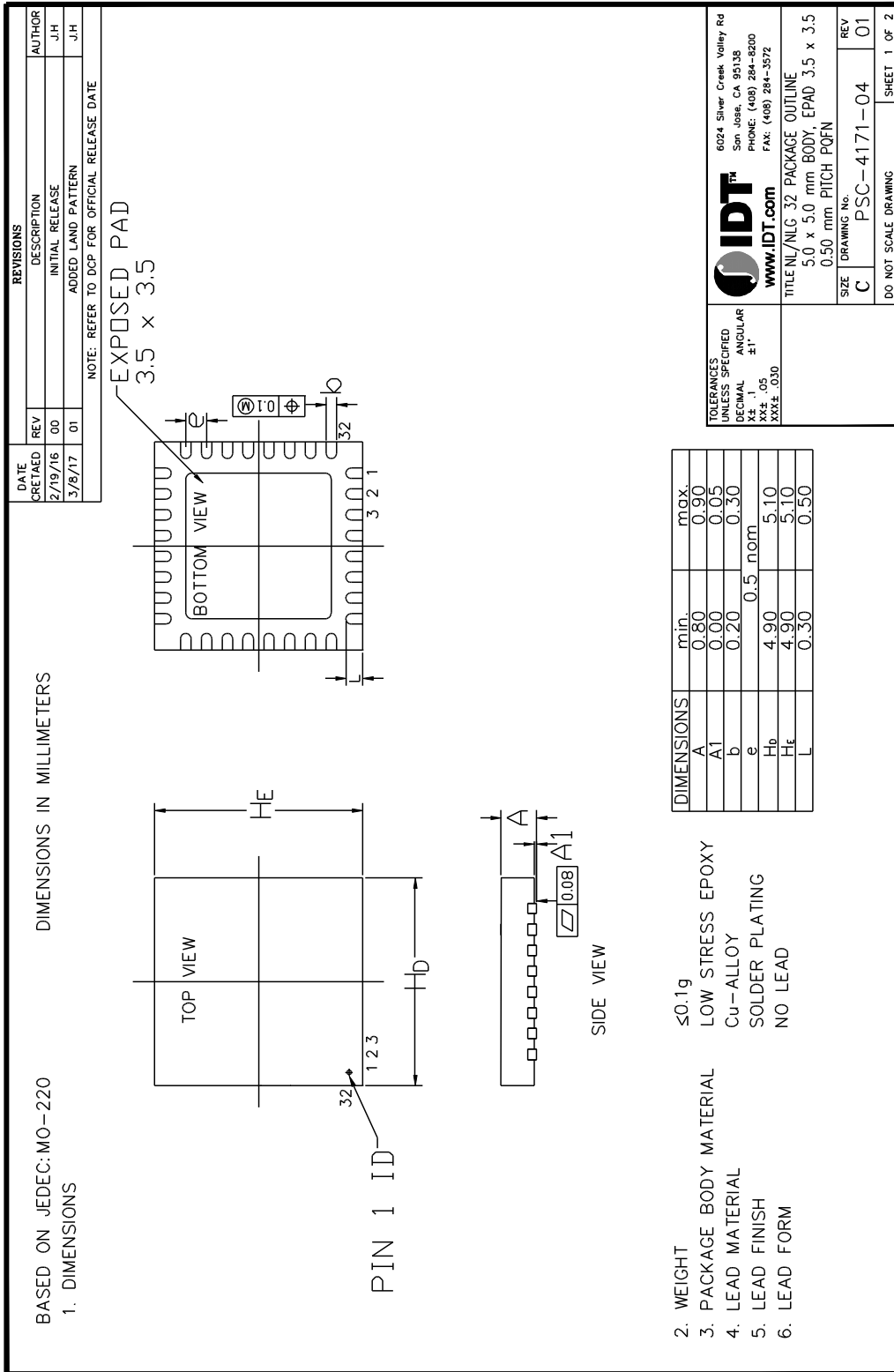
11. Recommended Land Pattern

Figure 7.   32-PQFN Landing Pattern

RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE IS SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

12. Marking Diagram

1. Line 1 is the company name.

2. Line 2 is the product name.

3. Line 3 is the lot number: XXXXXXXX (see purchase order, not the engraved lot number)

4. Line 4 is the date code. "YYWW" is the last two digits of the year followed by two digits for the week that the part was assembled.

5. Line 5 is the UL logo.

13. Glossary

Acronym	Definition
ADC	Analog-to-Digital Converter
AFCI	Arc-Fault Circuit Interrupter
AFD	Arc-Fault Detector/Detected
AFS	Arc Feature Signal
BIST	Built-in Self-Test
BOM	Bill of Materials
FFT	Fast Fourier Transform
GUI	Graphical User Interface
LED	Light Emitting Diode
MCU	Microcontroller Unit
MPPT	Maximum Power Point Tracker
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
POR	Power-on Reset
PV	Photovoltaic
PWM	Pulse Width Modulation
RTHP	Thermal Resistance of the Package
STO	Safety Troubles Output
UART	Universal Asynchronous Receiver/Transmitter

14. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Temperature
ZNRG2061AA1R	ZNRG2061 Arc-Fault Detector IC 5 × 5 mm 32-PQFN	3	Reel	-40°C to +85°C
ZNRG2061AA1V	ZNRG2061 Arc-Fault Detector IC 5 × 5 mm 32-PQFN	3	Tray	-40°C to +85°C
ZNRG2061KITV1P0	ZNRG2061 Evaluation Kit: Modular Evaluation Board for ZNRG2061, 100:100-turns current transformer, and micro-USB cable. Software and documentation can be downloaded from the product page at www.IDT.com/ZNRG2061 .			

15. Revision History

Revision Date	Description of Change
March 31, 2017	Correction for description of shipping package for ZNRG2061AA1V.
March 29, 2017	Update for part codes and kit contents.
March 16, 2017	Initial release of datasheet.

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