Application Report
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TPA31xxDx Bootstrap Circuit

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ABSTRACT

The full H-bridge output stages use only n-channel MOSFETs (NMOS) on TPA31xx devices. Therefore, bootstrap capacitors are required to correctly turn on the high side of each output. This document introduces this circuit on TPA31xxDx devices.

NOTE: This document only applies for TPA31xxDx devices.

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1 Introduction

In most switching applications, the bootstrap circuit is widely used to drive the high-side metal-oxide-semiconductor field-effect transistor (MOSFET). This bootstrap circuit technique has the advantage of being simple and low cost. The bootstrap capacitors connected between the BSxx pins and corresponding output pins function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

The purpose of this application note is to demonstrate in detail how the bootstrap circuit works on TP31xxDx devices, which are high-performance, class-D, audio amplifiers and application considerations which users must pay attention to are also included.

2 Device Overview

P-channel MOSFETs (PMOS) are typically approximately 3x larger than NMOS with the same RDS(on). To reduce the die area, replace the high-side PMOS device with NMOS. An all-NMOS output stage requires a bootstrap supply to power the high-side gate driver. The bootstrap diode forward biases while the output is low, to charge the bootstrap capacitor from GVDD. The bootstrap capacitor holds the bootstrap node at OUT+ GVDD. The bootstrap diode reverse biases when the output goes high. This process provides a floating power source for the high-side Gate Drive.

The bootstrap circuit is useful in a high-voltage gate driver and operates as follows. When OUT is pulled down to ground (the low-side switch is turned on and the high-side switch is turned off), the bootstrap capacitor charges through the bootstrap diode from the GVDD power supply, as shown in Figure 1. When the high-side switch is turned on and the low-side switch is turned off, OUT is pulled up to PVCC, then the bootstrap diode reverses bias and blocks the rail voltage from GVDD, as shown in Figure 2.

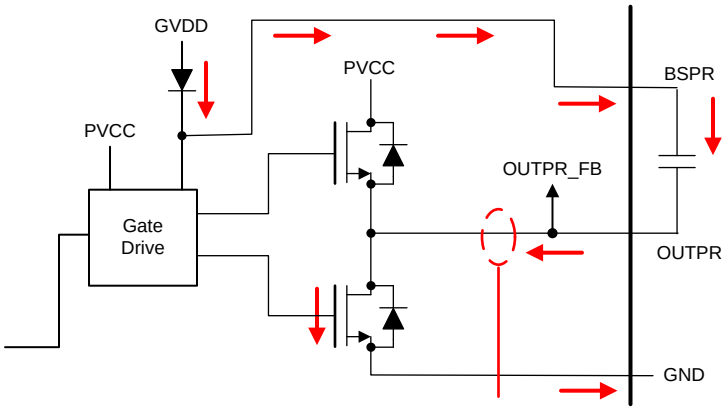

Figure 1. Bootstrap Capacitor Charging

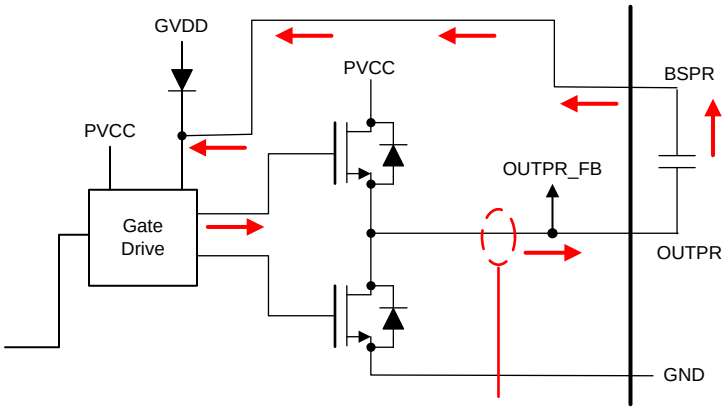

Figure 2. Bootstrap Capacitor Discharging

3 Application Considerations

The bootstrap circuit has the advantage of being both simple and low-cost. However, the requirement to refresh the charge on the bootstrap capacitor may result in some limitations. The flowing Figure 3 shows a failed case, which is caused by over-discharging on bootstrap capacitors. The red waveform in the following picture is for BSPR, the blue one is for OUTPR, and the green one is for FAULT. It is safe if the voltage difference between BSPR and OUTPT is larger than 5 V. From this screen capture, we can see that the FAULT is triggered because the voltage difference decreases to around 3 V. This measurement is based on 1-MHz switching frequency and 0.22-µF bootstrap capacitors.

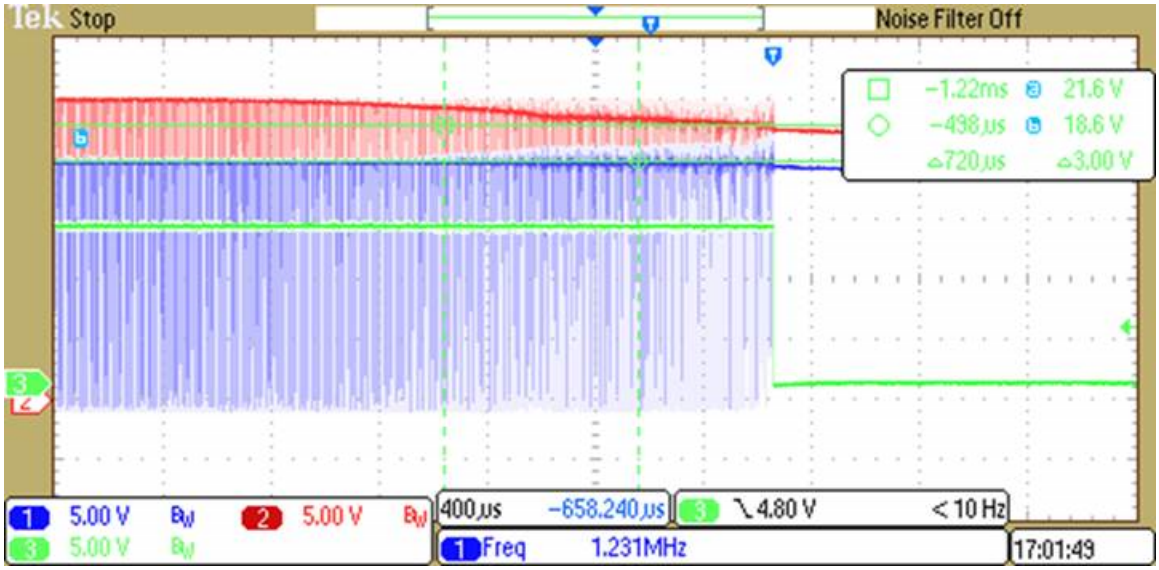

Figure 3. Bootstrap Voltage With F_{sw} = 1 MHz
(PVCC = 20 V, Open Load, F_{IN}= 10 Hz, V_{IN} = 900 mVrms, Gain = 26 dB)

In the following sections, some conditions that could cause this issue are introduced.

3.1 PWM Switching Frequency and Duty-Cycle

The charging time for the bootstrap capacitors is shorter for the high-PWM switching frequency than the low-PWM switching frequency case. The charge time is even shorter for the high-PWM duty-cycle case (the output signal is high). There is a probability that the voltage across the bootstrap capacitors is too low to turn on the high-side MOSFET.

Figure 4 shows the case with 400-kHz PWM frequency and Figure 5 shows the case with 1.2-MHz PWM frequency. Apparently, the charging time in each PWM cycle is shorter with higher PWM frequency. Figure 4 shows a 680-mVrms input signal, Figure 6 shows 300 mV, and all of the other conditions are the same. Apparently, the latter one has a longer charging time for the bootstrap capacitors.

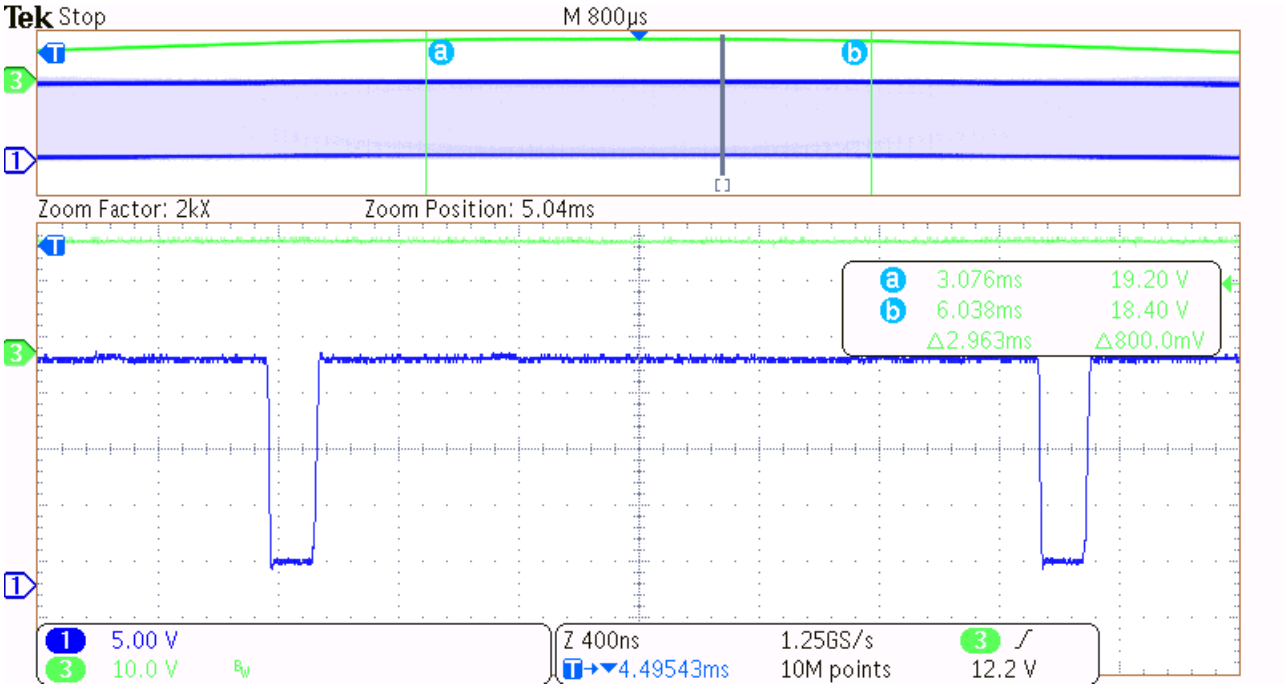

Figure 4. Output Duty-Cycle With F_{sw} = 400 kHz (PVCC = 20 V, Open Load, F_{IN}= 50 Hz, V_{IN}= 680 mVrms, Gain = 26 dB)

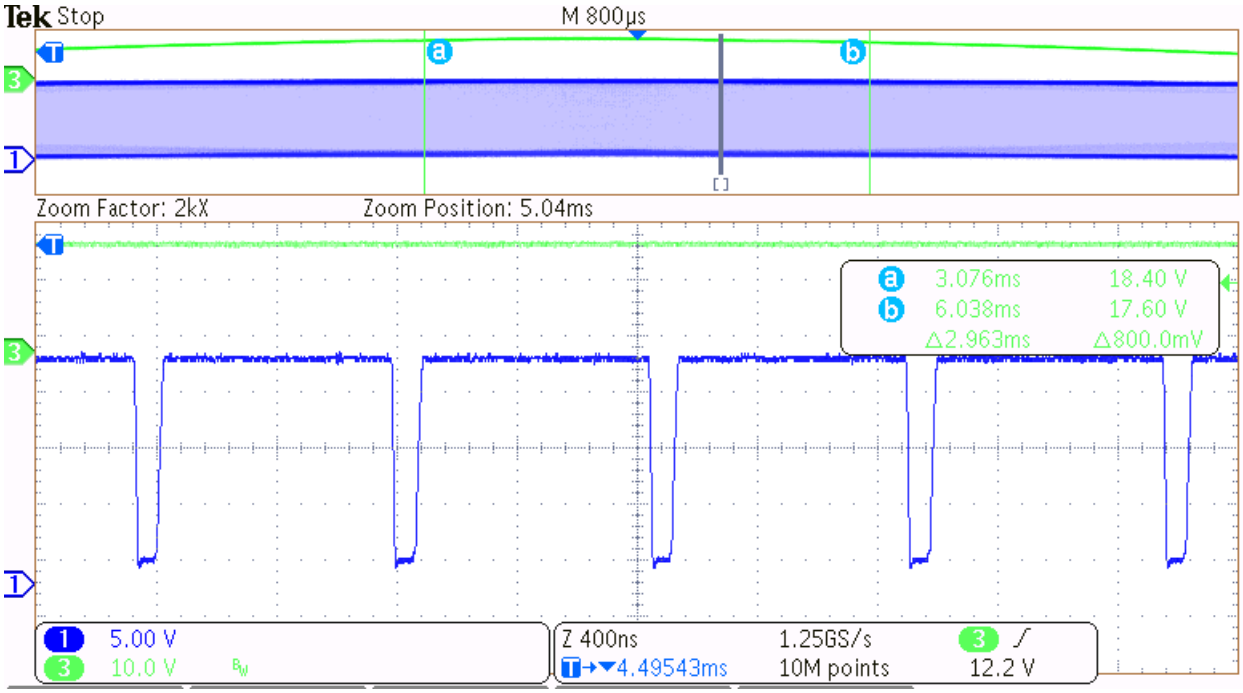

Figure 5. Output Duty-Cycle With F_{sw} = 1.2 MHz
(PVCC = 20 V, Open Load, F_{IN} = 50 Hz, V_{IN} = 680 mVrms, Gain = 26 dB)

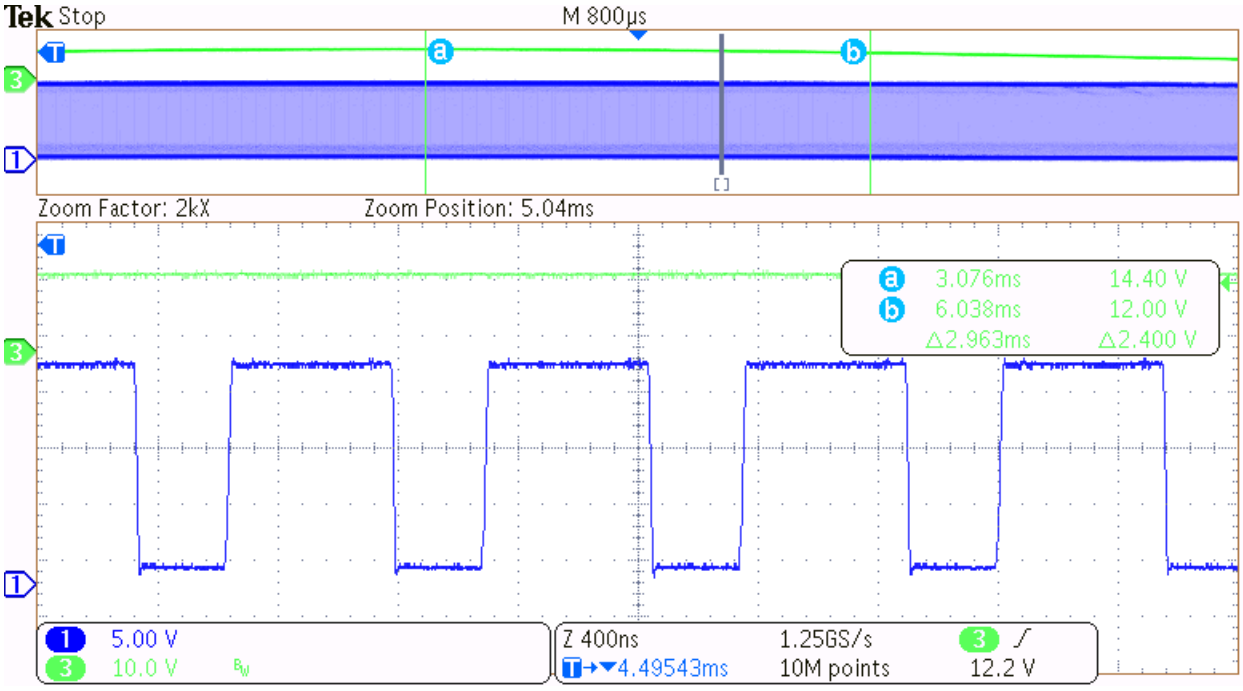

Figure 6. Output Duty-Cycle With F_{sw} = 400 kHz
(PVCC = 20 V, Open Load, F_{IN} = 50 Hz, V_{IN} = 300 mVrms, Gain = 26 dB)

3.2 Load Resistance

With a lower load resistance, the slew rate of the PWM switching is steep. While, for the higher load resistance, the slew rate is askew. Figure 7 shows two application cases: the first case is for a lower load resistance and the second case is for a higher load resistance. Then, the period of the low-level voltage (charging time for the bootstrap capacitors) in one cycle is actually longer with a lower load. So it is easier to cause the over-low voltage across the bootstrap capacitors with a higher load resistance.

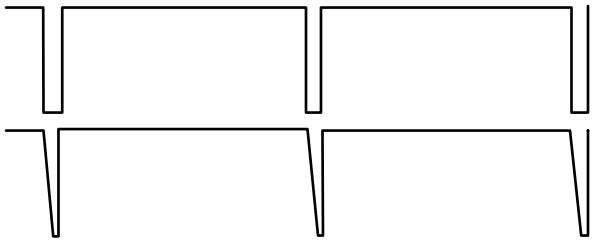

Figure 7. Slew Rate of Output PWM

3.3 Input Signal Frequency

With a lower-frequency input signal, the duration is longer with high output than the high frequency input signal. For example, a 50-Hz sinewave input and 1-kHz sinewave input, as shown in Figure 8 and Figure 9. The duration of high output for 50-Hz input is 20 times that of 1-kHz input. Then the possibility of overdischarging on bootstrap capacitors with a 50-Hz input signal is a lot higher than the 1-kHz input.

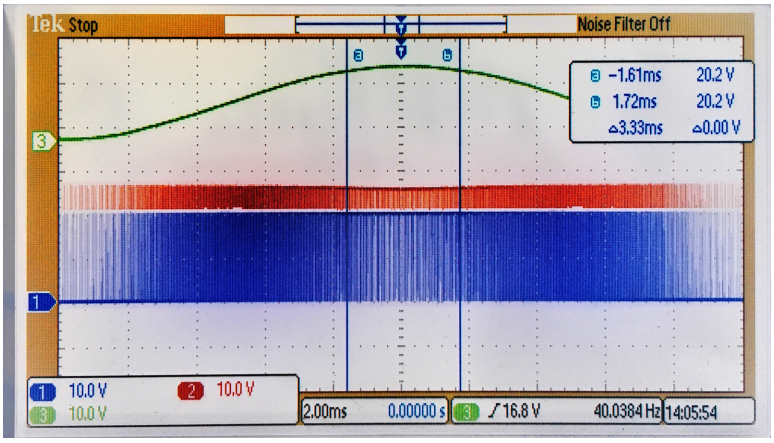

Figure 8. Output PWM With F_{IN} = 50 Hz
(PVCC = 20 V, Open Load, F_{sw} = 1.2 MHz, V_{IN} = 600 mVrms, Gain = 26 dB)

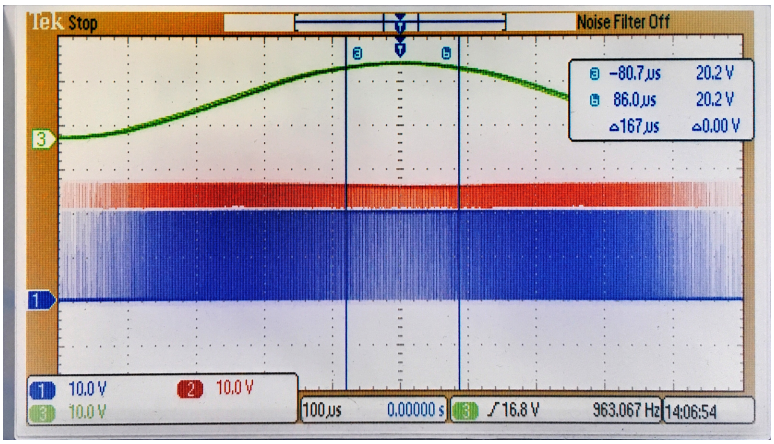

Figure 9. Output PWM With F_{IN} = 1 kHz (PVCC=20V, Open Load, F_{sw}=1.2MHz, V_{IN}=600mVrms, Gain=26dB)

3.4 PVCC

A power MOSFET has capacitances between the gate-drain, gate-source, and drain-source terminals, which also contribute to the discharging on the bootstrap capacitors. When the high-side MOFET is turned off, the voltage between gate-drain Vgd is –PVCC. When the high-side MOSFET is turned on, Vgd is changed to GVDD (the same as Vgs). Then the charge that must be supplied to Cgd is as follows in Equation 1.

$$Q = Cgd \times (GVDD - (-PVCC)) = Cgd \times (GVDD + PVCC). \quad (1)$$

Therefore, more charge is needed for a higher PVCC, and then it is easier to cause overdischarging on the bootstrap capacitors with a higher PVCC.

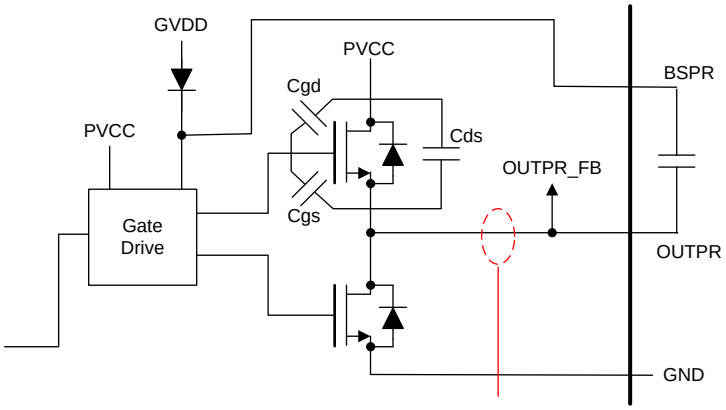

Figure 10. Capacitance Equivalent Circuit

Proper bootstrap capacitor selection and device configuration can drastically reduce these limitations. For extreme applications (large load and very low frequency input test signal), TI recommends using F_{sw} = 400 kHz and 0.47-µF bootstrap capacitors.

4 Conclusion

The bootstrap circuit is a very simple and low-cost solution for high-side MOSFET control on class-D audio amplifiers. Overdischarging on the bootstrap capacitors can occur in very extreme test cases. Using lower-frequency PWM settings (for example, 400 kHz) or a larger bootstrap capacitor (for example, 0.47 µF) can avoid this issue.

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