50 W 12 V 5 V SMPS demo board with ICE5QSAG and IPA80R650CE

AN-DEMO_5QSAG_50W1

About this document

Scope and purpose

This document is an engineering report that describes a universal input 50 W 12 V and 5 V offline flyback converter using the latest 5th generation Infineon QR controller ICE5QSAG and CoolMOS™ IPA80R650CE which offers high efficiency, low standby power with selectable entry and exit standby power options, wide VCC operating range with fast start up, robust line protection with input Over Voltage protection (OVP), brownout and various other protections for a highly reliable system. This demo board is designed for users who wish to evaluate the performance of ICE5QSAG, especially with regard to ease of use.

Intended audience

This document is intended for power supply design/application engineers, students, etc. who wish to design low cost and highly reliable off-line Switched Mode Power Supply (SMPS). These can be auxiliary power supplies for white goods, PCs, servers and TVs or enclosed adapters, Blu-ray players, set-top boxes, game consoles, etc.

Table of Contents

Abstract

1 Abstract

This application note is an engineering report for a 50 W 12 V and 5 V demo board designed in a QR Flyback converter topology using the 5th generation QR controller, ICE5QSAG and a MOSFET from the CE series of high voltage CoolMOS™ IPA80R650CE. The target applications for ICE5QSAG are auxiliary power supplies from white goods, PCs, servers and TVs or enclosed adapters, Blu-ray players, set-top boxes, game consoles, etc.

The novel and improved digital frequency reduction with proprietary QR operation offers lower EMI and higher efficiency for a wide AC range by reducing the switching frequency difference between low- and high-line. The enhanced active burst mode power enables flexibility in standby power operation range selection and QR operation during active burst mode. As a result, the system efficiency over the entire load range, is significantly improved compared to conventional free running QR converters implemented with only maximum switching frequency limitation at light load.

In addition, numerous adjustable protection functions have been implemented in the ICE5QSAG to protect the system and customize the IC for the chosen application. In case of failure modes such as brownout or line over voltage, VCC over/under voltage, open control loop or overload, output overvoltage, over temperature, VCC short to ground or CS short to ground, the device enters a protection mode.

Due to the cycle-by-cycle peak current limitation, the dimension of the transformer and current rating of the secondary diode can both be optimized. Thus, a cost effective solution can easily be achieved.

2 Demo board

This document contains a list of features, the power supply specification, schematic, Bill of Material (BOM) and transformer construction documentation. Typical operating characteristics such as performance curves and oscilloscope waveforms are shown at the end of the report.

Figure 1 DEMO_5QSAG_50W1

3 Specifications of demo board

Table 1 Specifications of DEMO_5QSAG_50W1

Input voltage and frequency	85 V AC (60 Hz) ~ 300 V AC (50Hz)
Output voltage, current and power	(12 V x 3.75 A) +(5 V x 1 A) = 50 W
Dynamic load response (5 V at 1 A and 12 V load change from 10% to 100%, slew rate at 0.4 A/µs, 100 Hz)	±5% of nominal output voltage
Output ripple voltage (full load, 85 V AC ~ 300 V AC)	5 $V_{ripple\_p\_p}$< 100 mV 12 $V_{ripple\_p\_p}$< 200 mV
Active mode four point average efficiency (25%, 50%, 75%, 100% load)	> 80% at 115 V AC and 230 V AC
No load power consumption	< 100 mW at 230 V AC
Conducted emissions (EN55022 class B)	Pass with 7 dB margin for 115 V AC and 6 dB margin for 230 V AC
ESD immunity (EN61000-4-2)	Special Level (±14 kV for contact and ±16 kV air discharge)
Surge immunity (EN61000-4-5)	Installation class 4 (±2 kV for line to line and ±4 kV for line to earth)
Form factor case size (L x W x H)	(160 x 83 x 43) mm^3

Note: "The demo board is designed for dual output with cross regulated loop feedback. It may not regulate properly if loading is applied only to a single output. If the user wants to evaluate for a single output (12 V only) condition, the following changes are necessary on the board.

1. Remove D22, L22, C28, C210, R25A (to disable 5 V output)
2. Change R26 to 10 kΩ and R25 to 38 kΩ (to disable 5 V feedback and enable 100% weighted factor on 12 V output)

Since the board (especially the transformer) is designed for dual output with optimized cross regulation, single output efficiency might not be optimized. It is only intended for IC functional evaluation under single output condition."

4 Circuit description

4.1 Line input

The AC line input side comprises the input fuse F1 as over current protection. The choke L11, X-capacitor C11 and Y-capacitor C12, C12A and C12B act as EMI suppressors. Optional spark gap devices SA1, SA2 and varistor VAR can absorb high voltage stress during lightning surge test. A rectified DC voltage (120~424 V DC) is obtained through the bridge rectifier BR1 together with the bulk capacitor C13.

4.2 Start-up

To achieve fast and safe start-up, ICE5QSAG has a startup resistor and VCC short to GND protection. When VCC reaches the turn-on voltage threshold of 16 V, the IC begins with a soft-start. The soft-start implemented in ICE5QSAG is a digital time-based function. The preset soft-start time is 12 ms with 4 steps. If not limited by other functions, the peak voltage on the CS pin will increase step by step from 0.3 V to 1 V. After the IC turns on, the VCC voltage is supplied by auxiliary windings of the transformer. VCC short to GND protection is implemented during the startup time.

4.3 PWM control and switching MOSFET

The PWM pulse is generated by the fifth generation QR PWM current-mode controller ICE5QSAG. This PWM pulse drives the high voltage power MOSFETs, IPA80R650CE. CoolMOS™ provides all the benefits of a fast switching superjunction (SJ) MOSFET while not sacrificing ease of use. It achieves extremely low conduction and switching losses and can make switching applications more efficient, more compact, lighter and cooler. The PWM switch-on is determined by the zero crossing input signal and the value of the up/down counter. The PWM switch-off is determined by the feedback signal V_{FB} and the current sensing signal V_{CS}. ICE5QSAG also performs all necessary protection functions in Flyback converters. Full details regarding this are contained in the product datasheet.

4.4 RCD clamper circuit

A clamper network (R11, R11A, C15 and D11) dissipates the energy of the leakage inductance and suppress ringing on the SMPS transformer.

4.5 Output stage

There are two outputs on the secondary side, 12 V and 5 V. The power is coupled out via Schottky diodes D21 and D22. Capacitors C22, C23 and C28 provide energy buffering followed by the L-C filters L21-C24 and L22-C210 to reduce the output ripple and prevent interference between the SMPS switching frequency and the line frequency. Storage capacitors C22, C23 and C28 are designed to have an internal resistance (ESR) that is as small as possible to minimize the output voltage ripple caused by the triangular current.

4.6 Feedback loop

For feedback, the output is sensed by the voltage divider of R26, R25, R25A and compared to IC21's (TL431) internal reference voltage. C25, C26 and R24 comprise the compensation network. The output voltage of IC21 (TL431) is converted to a current signal via optocoupler IC12 and two resistors R22 and R23 for regulation control.

4.7 Primary side peak current control

The MOSFET drain source current is sensed via external resistors R14 and R14A. As ICE5QSAG is a current mode controller, it has a cycle-by-cycle primary current and feedback voltage control which ensures that the maximum power of the converter is controlled during every switching cycle.

For a QR Flyback converter, the maximum possible output power is increased when a constant current limit value is used for the entire line input voltage range. This is usually not desired, as this will increase the cost of the transformer and output diode in the case of output over power conditions.

Internal current limitation with line dependent V_{CS} curve and the proprietary novel QR switching that reduces the switching frequency difference between minimum and maximum line are implemented in the ICE5QSAG. As the result, the maximum output power can be effectively limited against the input voltage.

4.8 Digital frequency reduction

During normal operation, the switching frequency for ICE5QSAG is digitally reduced with decreasing load. At light load, the MOSFET will not be turned on at the first minimum drain-source voltage time, but on the n^{th}. The counter is in the range of 1 to 8 for low line and 3 to 10 for high line, which depends on the feedback voltage in a time-base. The feedback voltage decreases when the output power requirement decreases, and vice versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

4.9 Active burst mode

Active burst mode entry and exit power (2 levels) can be selected in the ICE5QSAG. Details of this are shown in the product datasheet. Active burst mode power level 1 is used in this demo board (R17=open). At light load conditions, the SMPS enters into active burst mode with QR switching. At this stage, the controller is always active but VCC must be kept above the switch-off threshold. During active burst mode, the efficiency increases significantly and simultaneously supports low ripple on V_{out} and fast response on load jump.

For determination of entering active burst mode operation, three conditions apply:

1. the feedback voltage is lower than the threshold of V_{FB_EBLX}
2. the up/down counter is 8 for low line and 10 for high line and
3. a certain blanking time (t_{FB_BEB} =20 ms).

Once all of these conditions are fulfilled, the active burst mode flip-flop is set and the controller enters active burst mode operation. This multi condition determination for entering active burst mode operation prevents mis-triggering, so that the controller enters active burst mode operation only when the output power is actually low during the preset blanking time.

During active burst mode, the maximum current sense voltage is reduced from V_{CS_N} to V_{CS_BLX} so as to reduce conduction loss and audible noise. At burst mode, the feedback voltage is a sawtooth between V_{FB_BOFF} and V_{FB_BON}.

The feedback voltage immediately increases if there is a significant load jump. This is observed by one comparator. As the current limit is 31/35% during active burst mode a certain load is needed so that the feedback voltage can exceed V_{FB_LB}. After leaving active burst mode, maximum current can now be provided to stabilize V_{out}. In addition, the up/down counter will be set to 1 (low line) or 3 (high line) immediately after leaving active burst mode. This is helpful to decrease the output voltage undershoot.

5 Protection features

Protection is one of the major factors to determine whether the system is safe and robust. Therefore, sufficient protection is necessary. ICE5QSAG provides comprehensive protection to ensure that the system is operating safely. Protections include line over voltage, brownout, VCC over voltage and under voltage, overload, output over voltage, over temperature (controller junction), CS short to GND and VCC short to GND. When faults are found, the system will enter protection mode. When the fault is removed, the system resumes normal operation. A list of protections and the failure conditions are shown in the table below.

Table 2 Protection function of ICE5QSAG

Protection function	Failure condition	Protection mode
Line over voltage	V_{VIN} > 2.9 V	Non switch auto restart
Brownout	V_{VIN} < 0.4 V	Non switch auto restart
VCC over voltage	V_{VCC} > 25.5 V	Odd skip auto restart
VCC under voltage	V_{VCC} < 10 V	Auto restart
Overload	V_{FB} > 2.75 V & last for 30 ms	Odd skip auto restart
Output over voltage	V_{ZCD} > 2 V & last for 10 consecutive pulses	Odd skip auto restart
Over temperature (Junction temperature of controller chip only)	T_J > 140°C with 40°C hysteresis to reset	Non switch auto restart
CS short to GND	V_{CS} < 0.1 V, last for 5 µs and 3 consecutive pulses	Odd skip auto restart
VCC short to GND (V_{VCC}=0 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V)	V_{VCC}< 1.2 V, $I_{VCC\_Charge1}$≈0.2 A	Cannot start up

6 Circuit diagram

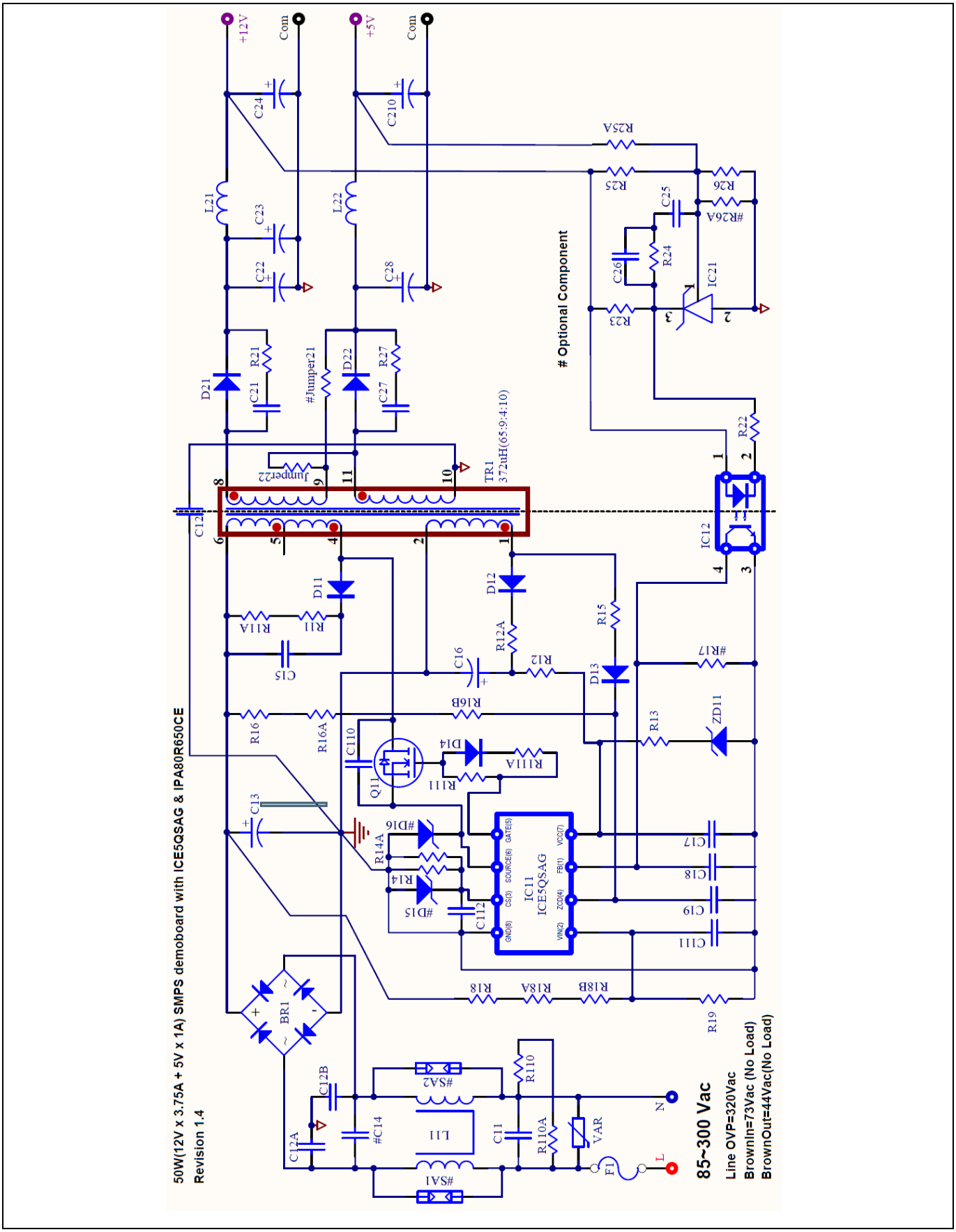


Figure 2 Schematic of DEMO_5QSAG_50W1

Circuit diagram

Note: General guideline for the layout design of the PCB:

1. *Star ground at bulk capacitor C13: all primary grounds should be connected to the ground of bulk capacitor C13 separately at one point. This can effectively reduce the switching noise entering the sensitive pins of the controller device. The primary star ground can be split into four groups as follows,*
    - i. *Combine signal ground (all small signal grounds connecting to the controller GND pin such as filter capacitor ground C17, C18, C19, C111, C112 and optocoupler ground) and power ground (Current Sense resistor R14 and R14A).*
    - ii. *VCC ground includes the VCC capacitor ground C16 and the auxiliary winding ground, pin 2 of the power transformer.*
    - iii. *EMI return ground includes Y capacitor C12.*
    - iv. *DC ground from bridge rectifier, BR1*
2. *Filter capacitor close to the controller ground: Filter capacitors, C17, C18, C19, C111 and C112 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.*
3. *High voltage traces clearance: High voltage traces should maintain sufficient spacing to the nearby traces. Otherwise, arcing will occur.*
    - i. *400 V traces (positive rail of bulk capacitor C13) to nearby trace: > 2.0 mm*
    - ii. *600 V traces (drain voltage of CoolMOS™ Q11) to nearby trace: > 2.5 mm*
4. *Power loop area (bulk capacitor C13, primary winding of the transformer TR1 (Pin 4 and 6), Q11 drain pin, IC11 CS pin and current sense resistor R14/R14A) should be as small as possible to minimize the switching emissions.*

7 PCB layout

7.1 Top side

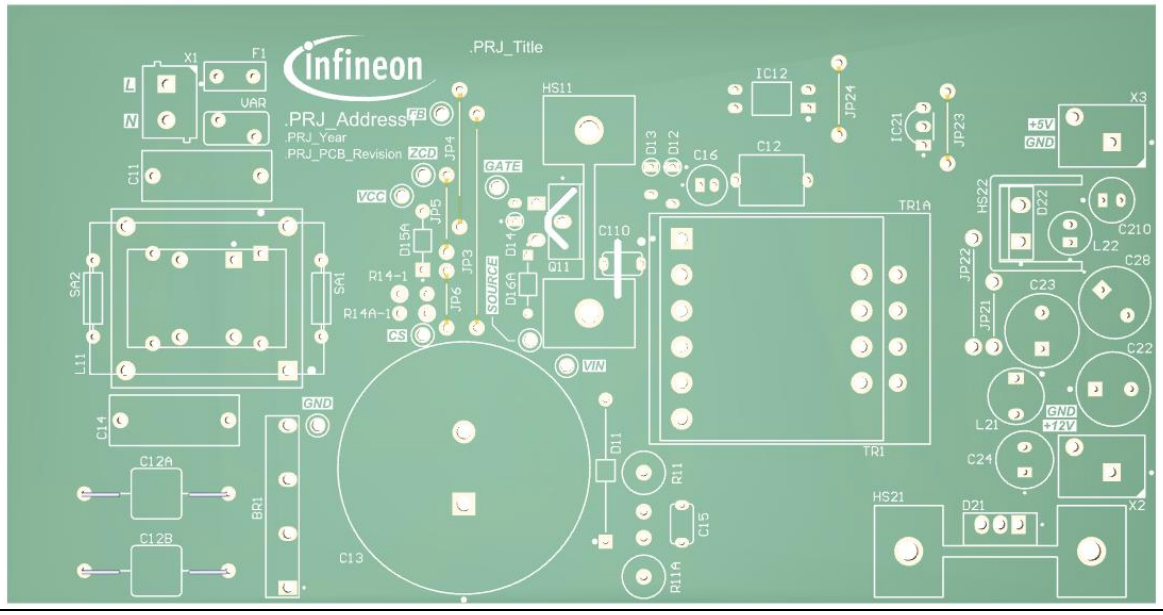


Figure 3 Top side component legend

7.2 Bottom side

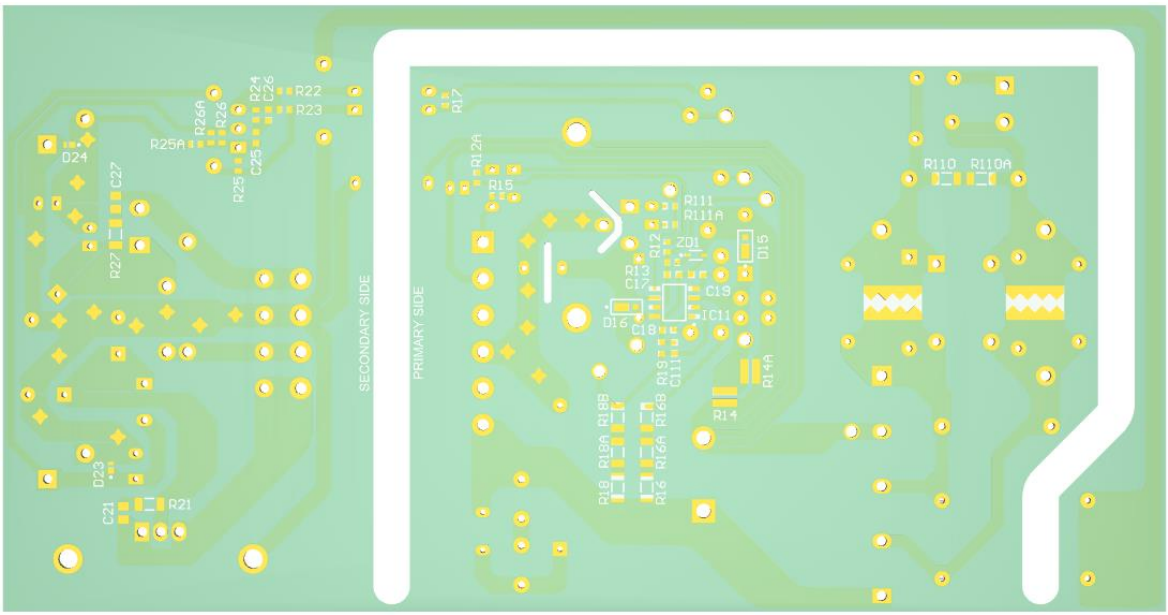


Figure 4 Bottom side copper and component legend

8 BOM

Table 3 BOM (V 1.4)

No.	Designator	Description	Part Number	Manufacturer	Quantity
1	BR1	600 V/4 A	D4SB60L	Shindengen	1
2	C11	0.47 µF/305 V	B32922C3474	Epcos	1
3	C12	1 nF/500 V	DE1E3RA102MA4BQ	Murata	1
4	C12A, C12B	470 pF/400 V	DE2B3SA471KA3BY	Murata	2
5	C13	180 µF/500 V	500VXG180MEFCSN35X30	Rubycon	1
6	C15	2.2 nF/1000 V	RDE7U3A222J3K1H03	Murata	1
7	C16	47 µF/50 V	35PX47MEFC5X11	Rubycon	1
8	C17	100 nF/50 V	GRM188R71H104KA93D	Murata	1
9	C18, C26	1 nF/50 V	GRM1885C1H102GA01D	Murata	2
10	C19	18 pF/50 V	GRM1885C1H180GA01D	Murata	1
11	C110	33 pF/1000 V	RDE7U3A330J2K1H03	Murata	1
12	C111	22 nF/50 V	GCM188R71H223KA37D	Murata	1
13	C112	33 nF/50 V	GRM188R71H333KA61D	Murata	1
14	C21, C27	1 nF/100 V	GRM2162C2A102JA01#	Murata	2
15	C22, C23	1500 uF/16 V	16ZLH1500MEFC10X20	Rubycon	2
16	C24	470 uF/16 V	16ZLH470MEFC8X11.5	Rubycon	1
17	C25	220 nF/50 V	GRM188R71H224KAC4D	Murata	1
18	C28	1500 uF/10 V	10ZLH1500MEFC10X16	Rubycon	1
19	C210	330 uF/10 V	10ZLH330MEFC6.3X11	Rubycon	1
20	D11	1 A/800 V	UF4006		1
21	D12	0.5 A/200 V	1N485B		1
22	D13, D14	0.2 A/150 V/50 ns	FDH400		1
23	D21	30 A/100 V	VF30100SG		1
24	D22	10 A/45 V	VFT1045BP		1
25	F1	3.15 A/300 V	36913150000		1
26	FB1	Ferrite bead @ D12	B64290P0035X038		1
27	HS11	Heatsink	513002B02500G		1
28	HS21	Heatsink	513102B02500G		1
29	HS22	Heatsink	577202B00000G		1
30	IC11	ICE5QSAG	ICE5QSAG	Infineon	1
31	IC12	Optocoupler	SFH617A-3		1
32	IC21	Shunt regulator	TL431BVLPG		1
33	JP3, JP4, JP5, JP6, JP22(Ø≈1.3 mm), JP23, JP24	Jumper			7
34	L11	27 mH/1.7 A	B82734R2172B030	Epcos	1
35	L21	2.2 uH/6 A	744772022	Wurth Electronics	1
36	L22	4.7 uH/4.2 A	7447462047	Wurth Electronics	1
37	Q11	800 V/650 mΩ	IPA80R650CE	Infineon	1

BOM

38	R11, R11A	15 kΩ /2 W/350 V	ERG-2SJ153A	Panasonic	2
39	R12, R13	27 Ω(0603)			2
40	R12A, R111A	0 Ω(0603)			2
41	R14	0.33 R/1 W/±1%	ERJ-B2BFR33V	Panasonic	1
42	R15	22 kΩ/±1%(0603)			1
43	R16, R16A, R16B	15 MΩ /0.25 W/5%	RC1206JR-0715ML		3
44	R18, R18A, R18B	3 MΩ/0.25 W/1%	RC1206FR-073ML		3
45	R19	58.3 kΩ /0.1 W/0.5%	RT0603DRE0758K3L		1
46	R110, R110A	1 MΩ/5%/200 V	RC1206JR-071ML		2
47	R111	15 Ω (0603)			1
48	R21	51 Ω / 0.25 W/ ±1%	ERJ8ENF51R0V	Panasonic	1
49	R22	820 Ω (0603)			1
50	R23	1.2 kΩ (0603)			1
51	R24	12 kΩ (0603)			1
52	R25	16 kΩ (0603)			1
53	R25A	6.2 kΩ (0603)			1
54	R26	2.5 kΩ (0603)			1
55	R27	13 R/0.25 W/±1%	ERJ8ENF13R0V	Panasonic	1
56	TR1	372 µH	750343268(Rev 0.3)	Wurth Electronics	1
57	Test point of FB, VIN, CS, ZCD, GATE, SOURCE, VCC, GND	Test point	5010		8
58	VAR	0.25 W/320 V	B72207S2321K101	Epcos	1
59	ZD1	20 V Zener	UDZS20B		1
60	Con(L N)	Connector	691102710002	Wurth Electronics	1
61	Con(+12 V Com), Con(+5 V Com)	Connector	691 412 120 002B	Wurth Electronics	2

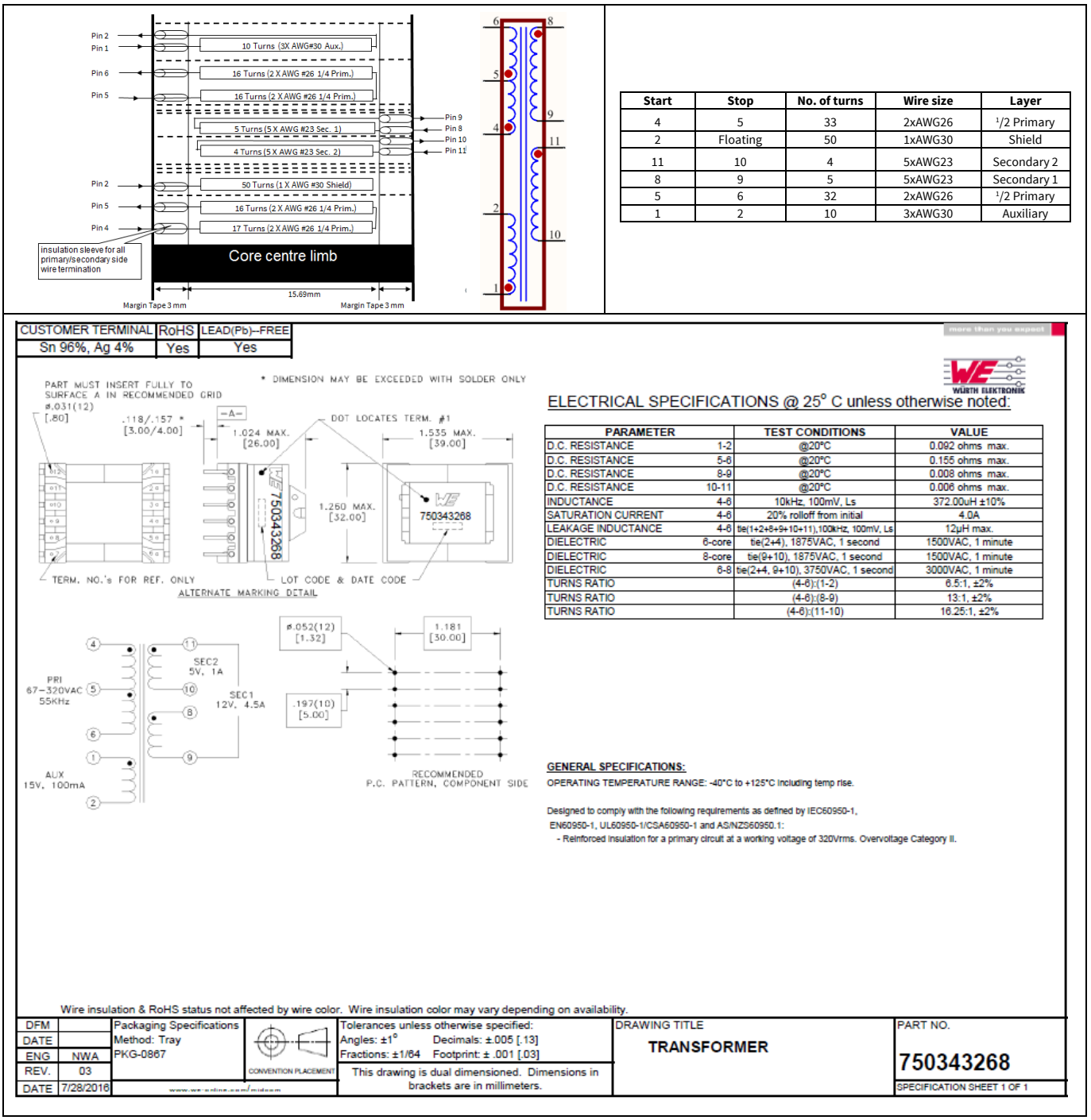
9 Transformer construction

Core and material: ER28/17, TP4A (TDG)

Bobbin: 070-5652 (12 Pin, THT, Horizontal Version)

Primary Inductance: Lp=372 µH (±10%), measured between pin 4 and pin 6

Manufacturer and part number: Wurth Electronics Midcom (750343268 R03)



Start	Stop	No. of turns	Wire size	Layer
4	5	33	2xAWG26	1/2 Primary
2	Floating	50	1xAWG30	Shield
11	10	4	5xAWG23	Secondary 2
8	9	5	5xAWG23	Secondary 1
5	6	32	2xAWG26	1/2 Primary
1	2	10	3xAWG30	Auxiliary

Figure 5 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation & output ripple

Input (V AC/Hz)	P_{in} (W)	V_{out1} (V DC)	I_{out1} (A)	V_{ORPP1} (mV)	V_{out2} (V DC)	I_{out2} (A)	V_{ORPP2} (mV)	P_{out} (W)	Efficiency η (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out2} (Fixed 5V at 1 A) (A)
85 V AC/ 60Hz	0.04803	5.12	0.000	18	11.95	0.000	39				75.70	4.54
	0.09079	4.96	0.006	66	12.39	0.000	40	0.03	32.78			
	14.89	5.18	0.060	23	11.82	1.000	45	12.13	81.47			
	15.42	5.11	0.250	20	12.02	0.938	40	12.55	81.36	80.95		
	30.75	5.12	0.500	22	12.01	1.875	50	25.08	81.56			
	46.34	5.12	0.750	27	12.01	2.813	60	37.62	81.18			
	62.97	5.11	1.000	40	12.02	3.750	95	50.19	79.70			
115 V AC/ 60Hz	0.05503	5.12	0.000	23	11.98	0.000	58				85.20	5.30
	0.09799	4.97	0.006	69	12.39	0.000	40	0.03	30.43			
	14.88	5.18	0.060	23	11.81	1.000	44	12.12	81.46			
	15.40	5.11	0.250	19	12.02	0.938	40	12.55	81.47	82.38		
	30.52	5.12	0.500	22	12.01	1.875	50	25.08	82.17			
	45.77	5.12	0.750	23	12.01	2.813	60	37.62	82.19			
	59.97	5.11	1.000	30	12.02	3.750	73	50.19	83.68			
230 V AC/ 50Hz	0.09543	5.13	0.000	17	11.95	0.000	39				87.20	5.57
	0.18668	5.02	0.006	46	12.23	0.000	91	0.03	16.13			
	15.38	5.18	0.060	24	11.80	1.000	46	12.11	78.74			
	15.90	5.12	0.250	20	12.01	0.938	42	12.54	78.86	80.85		
	31.01	5.12	0.500	22	12.01	1.875	45	25.08	80.87			
	46.11	5.12	0.750	24	12.00	2.813	60	37.59	81.52			
	61.06	5.11	1.000	27	12.01	3.750	80	50.15	82.13			
265 V AC/ 50Hz	0.11386	5.12	0.000	18	11.95	0.000	41				90.30	5.74
	0.20000	5.01	0.006	42	12.25	0.000	23	0.03	15.03			
	15.60	5.18	0.060	24	11.80	1.000	45	12.11	77.63			
	16.15	5.12	0.250	20	12.01	0.938	41	12.54	77.64	80.04		
	31.30	5.12	0.500	23	12.00	1.875	56	25.06	80.06			
	46.54	5.12	0.750	22	12.00	2.813	57	37.59	80.77			
	61.37	5.12	1.000	27	12.00	3.750	78	50.12	81.67			
300 V AC/ 50Hz	0.14030	5.12	0.000	18	11.96	0.000	43				92.80	5.90
	0.22000	5.01	0.006	42	12.27	0.000	23	0.03	13.66			
	15.89	5.18	0.060	24	11.79	1.000	45	12.10	76.15			
	16.41	5.11	0.250	22	12.00	0.938	46	12.53	76.34	79.10		
	31.69	5.12	0.500	23	12.00	1.875	55	25.06	79.08			
	47.05	5.12	0.750	22	12.00	2.813	55	37.59	79.89			
	61.82	5.12	1.000	27	12.00	3.750	85	50.12	81.07			

Minimum load condition : 5 V at 6 mA

Typical load condition : 5 V at 60 mA and 12 V at 1 A

Maximum load condition : 5 V at 1 A and 12 V at 3.75 A

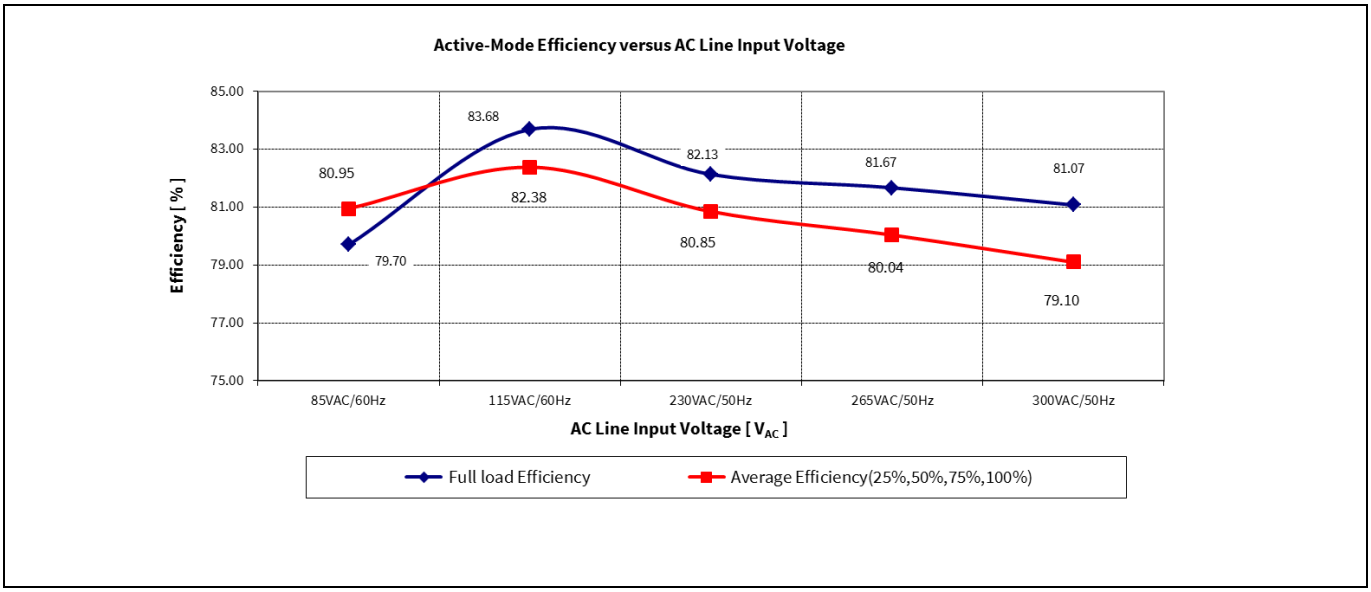


Figure 6 Efficiency vs. AC line input voltage

10.2 Standby power

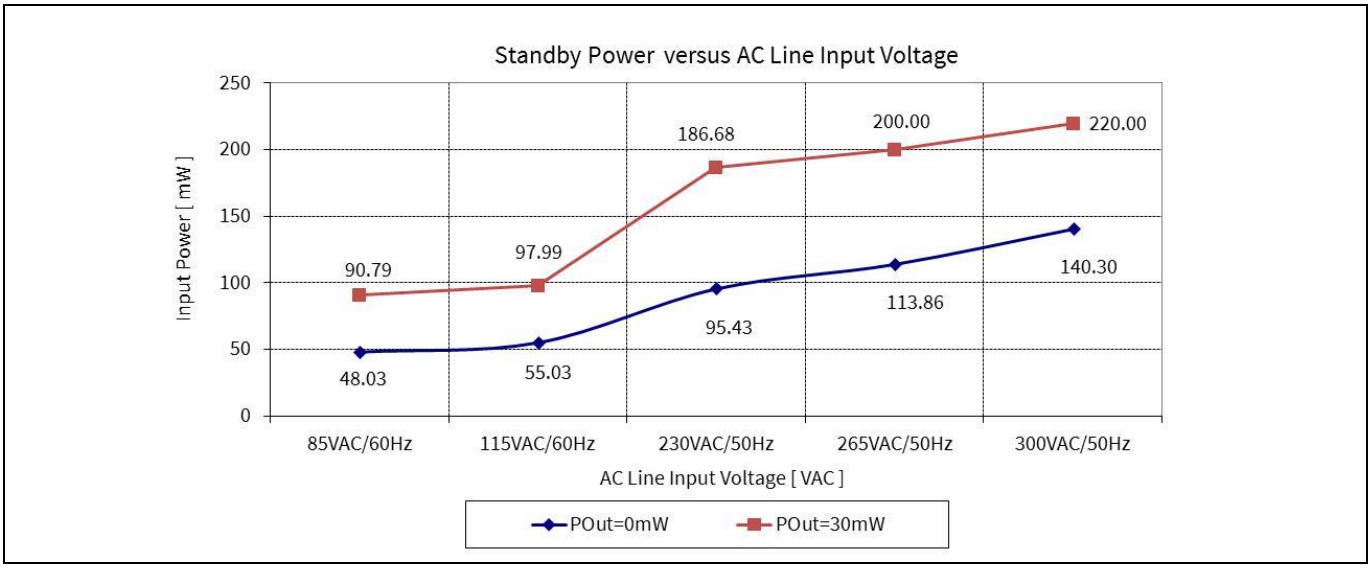


Figure 7 Standby power at no load and 30 mW load vs. AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

10.3 Line regulation

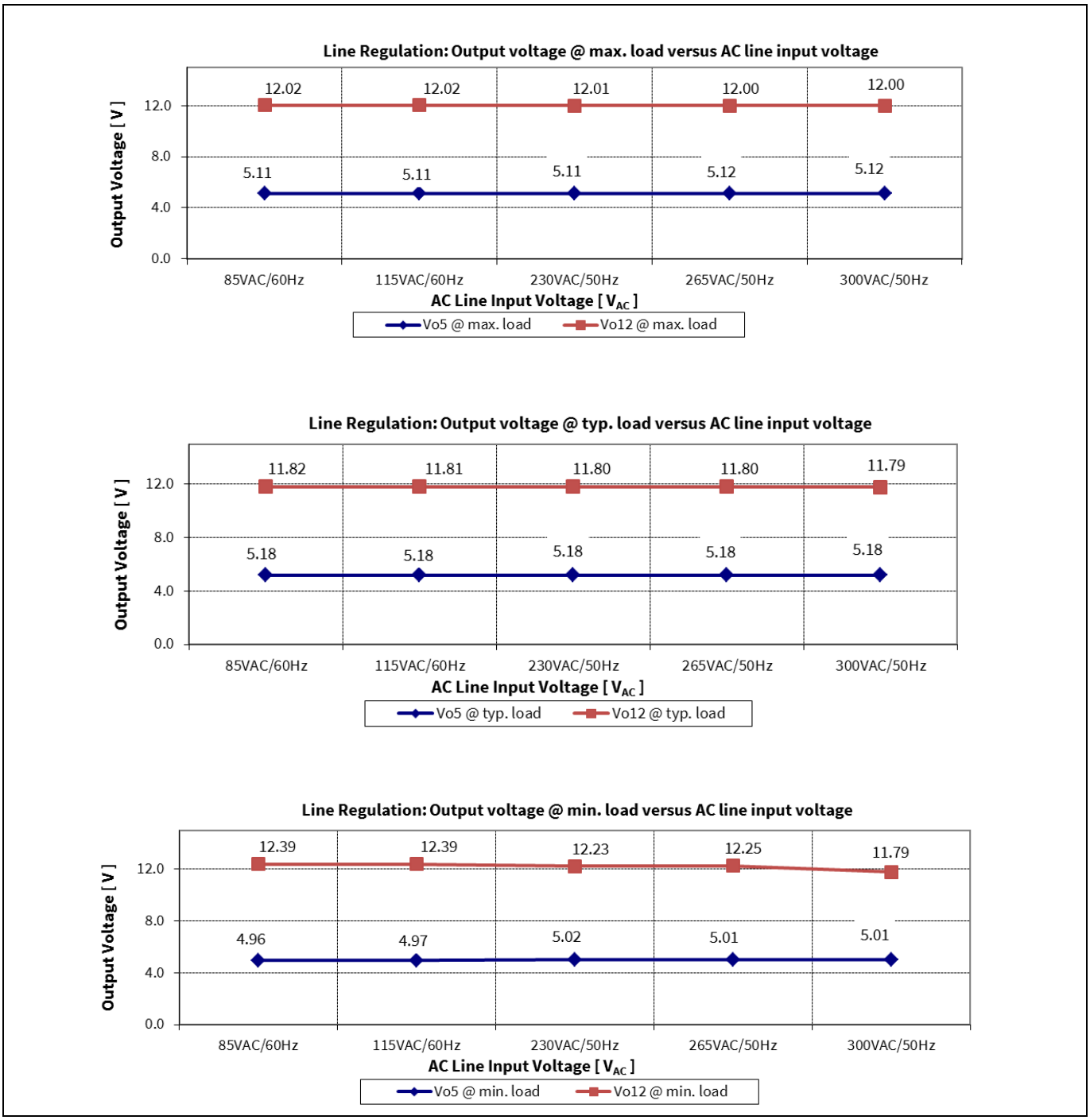


Figure 8 Line regulation V_{out} at full load vs AC line input voltage

10.4 Load regulation

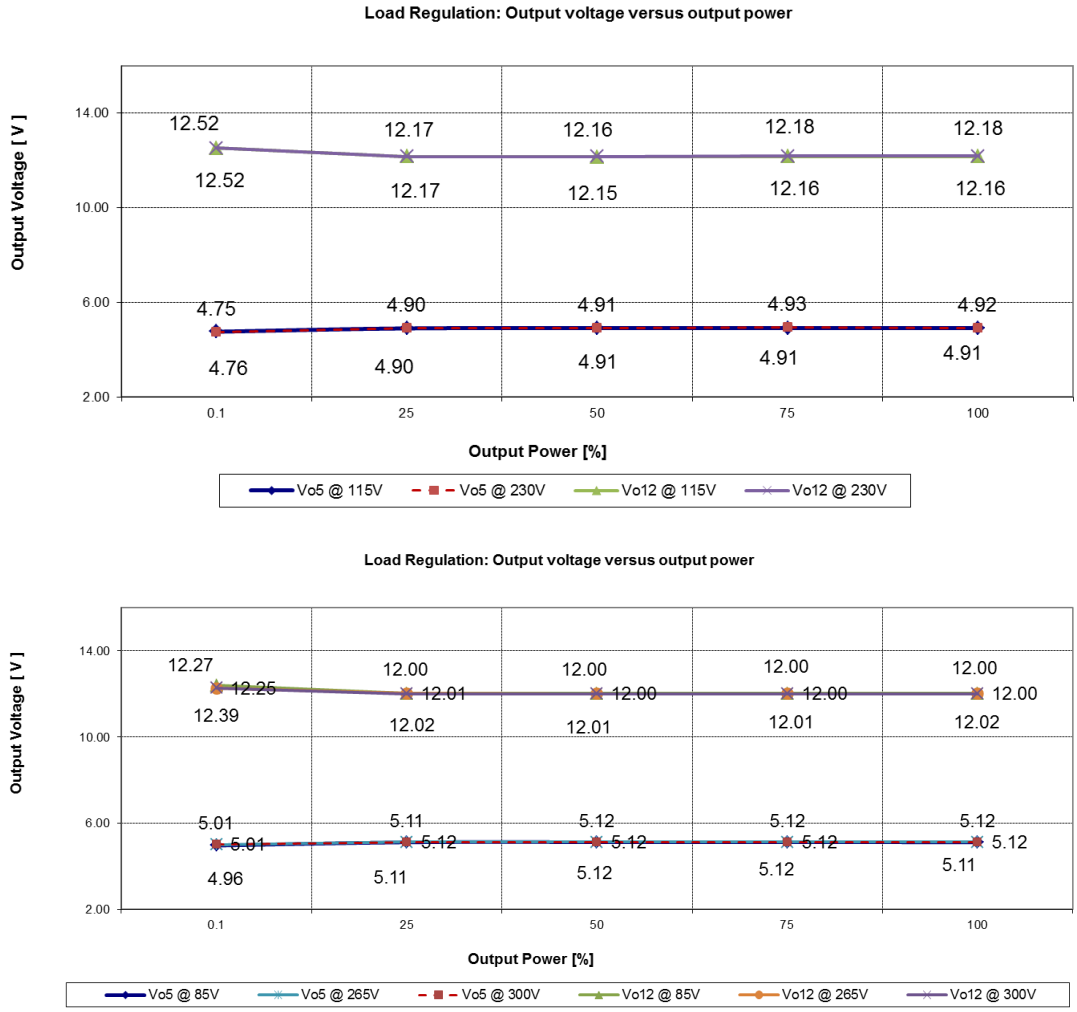


Figure 9 Load regulation V_{out} vs. output power

10.5 Maximum input power

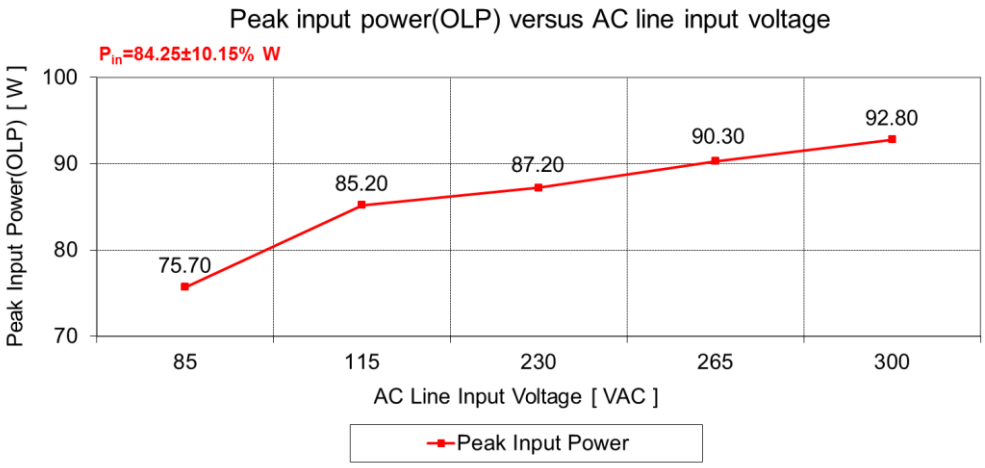


Figure 10 Maximum input power (before overload protection) vs. AC line input voltage

10.6 ESD immunity (EN61000-4-2)

Pass EN61000-4-2 Special Level (±14 kV for contact discharge and ±16 kV air discharge).

10.7 Surge immunity (EN61000-4-5)

Pass EN61000-4-5 Installation class 4 (±2 kV for line to line and ±4 kV for line to earth)[1].

10.8 Conducted emissions (EN55022 class B)

The conducted EMI was measured with a Schaffner SMR4503 in accordance with the test standard of EN55022 (CISPR 22) class B. The demo board was set up at maximum load (50 W) with input voltage of 115 V AC and 230 V AC.

[1] PCB spark gap distance needs to reduce to 0.5 mm.

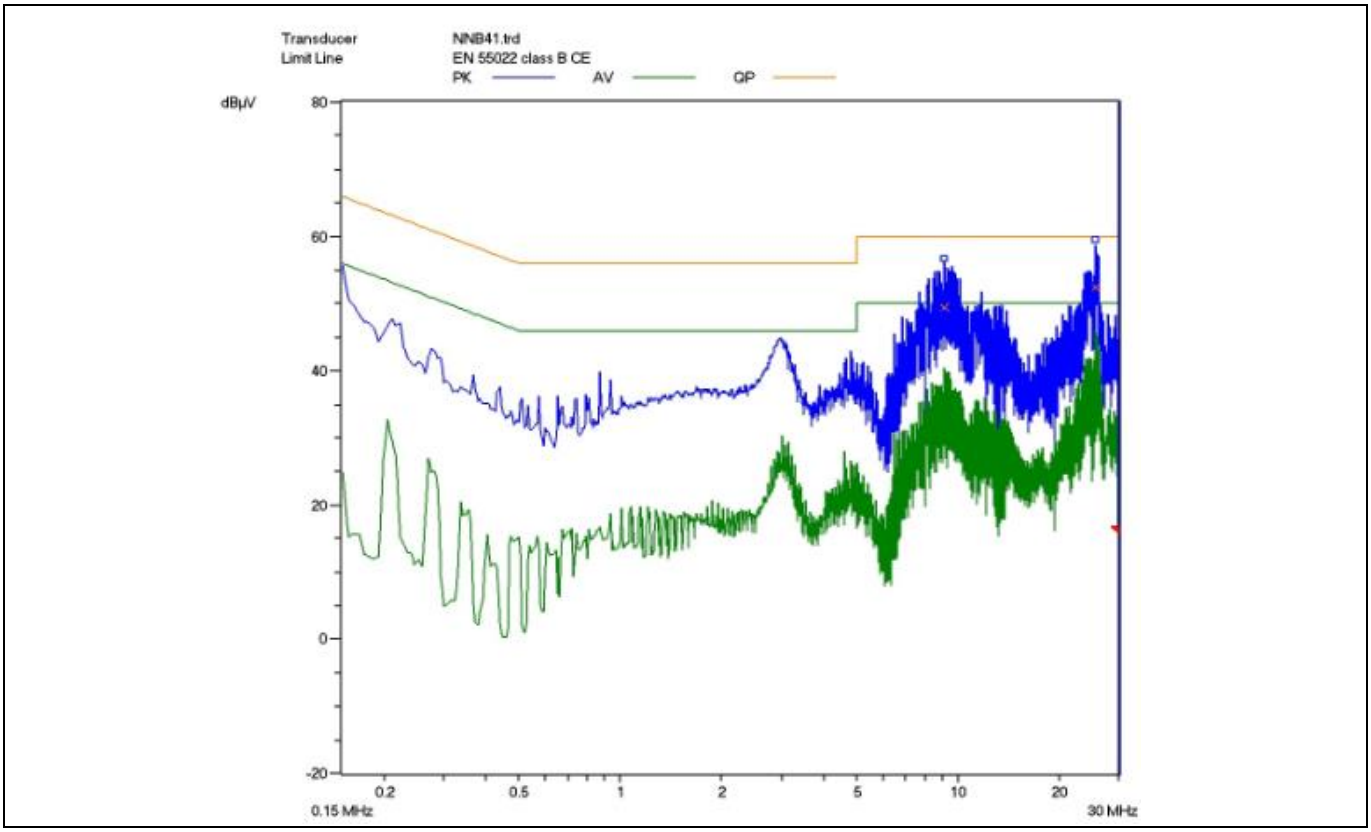


Figure 11 Conducted emissions (line) at 115 V AC and maximum load

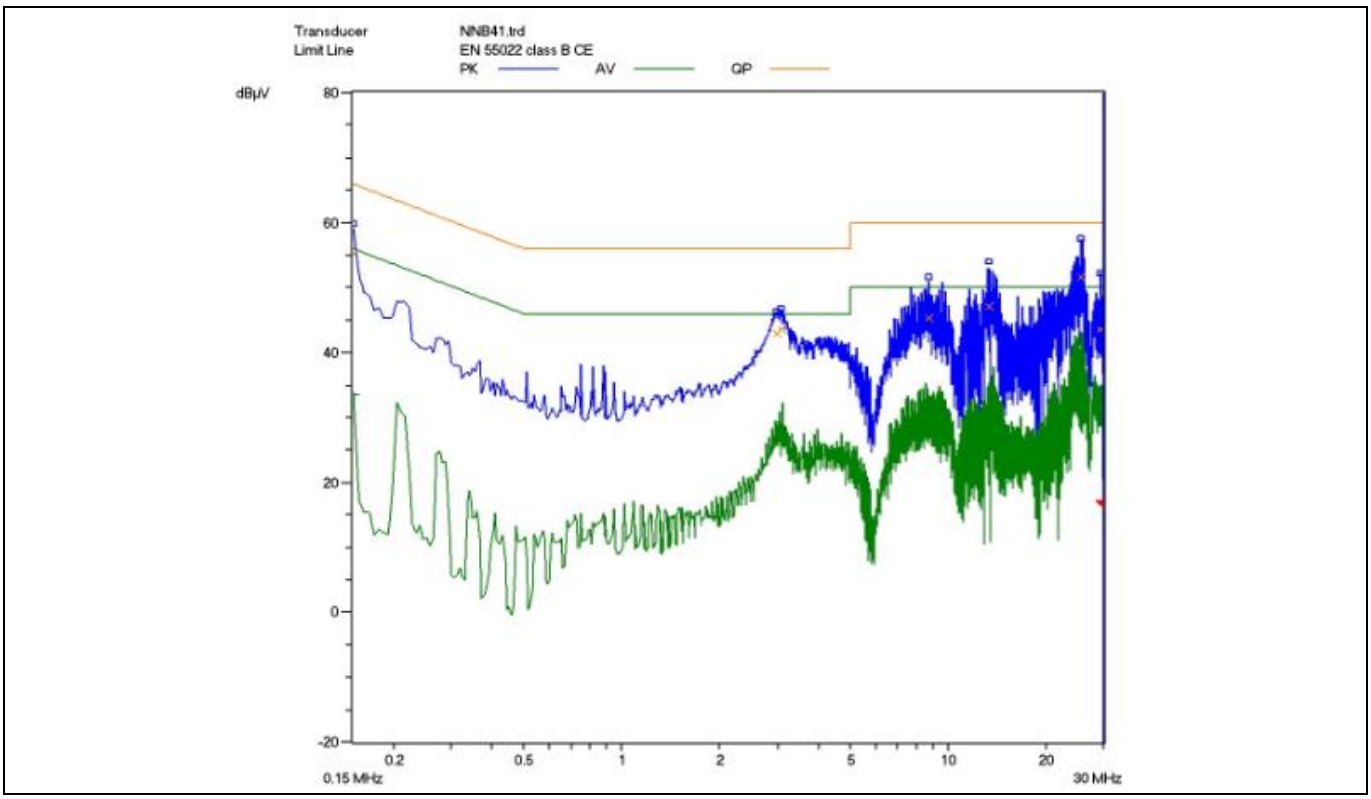


Figure 12 Conducted emissions (neutral) at 115 V AC and maximum load

Pass conducted emissions EN55022 (CISPR 22) class B with 7 dB margin for quasi-peak measurement at low line (115 V AC).

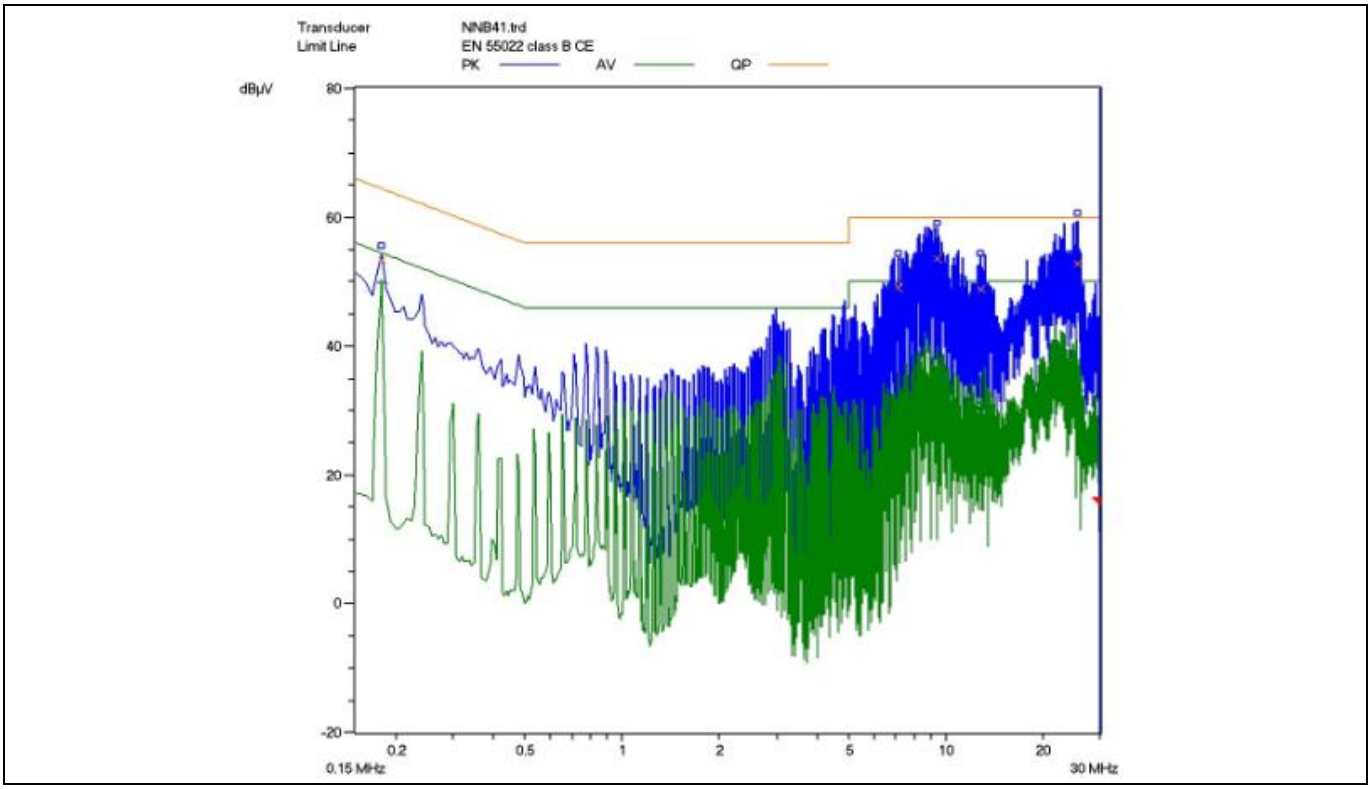


Figure 13 Conducted emissions (line) at 230 V AC and maximum load

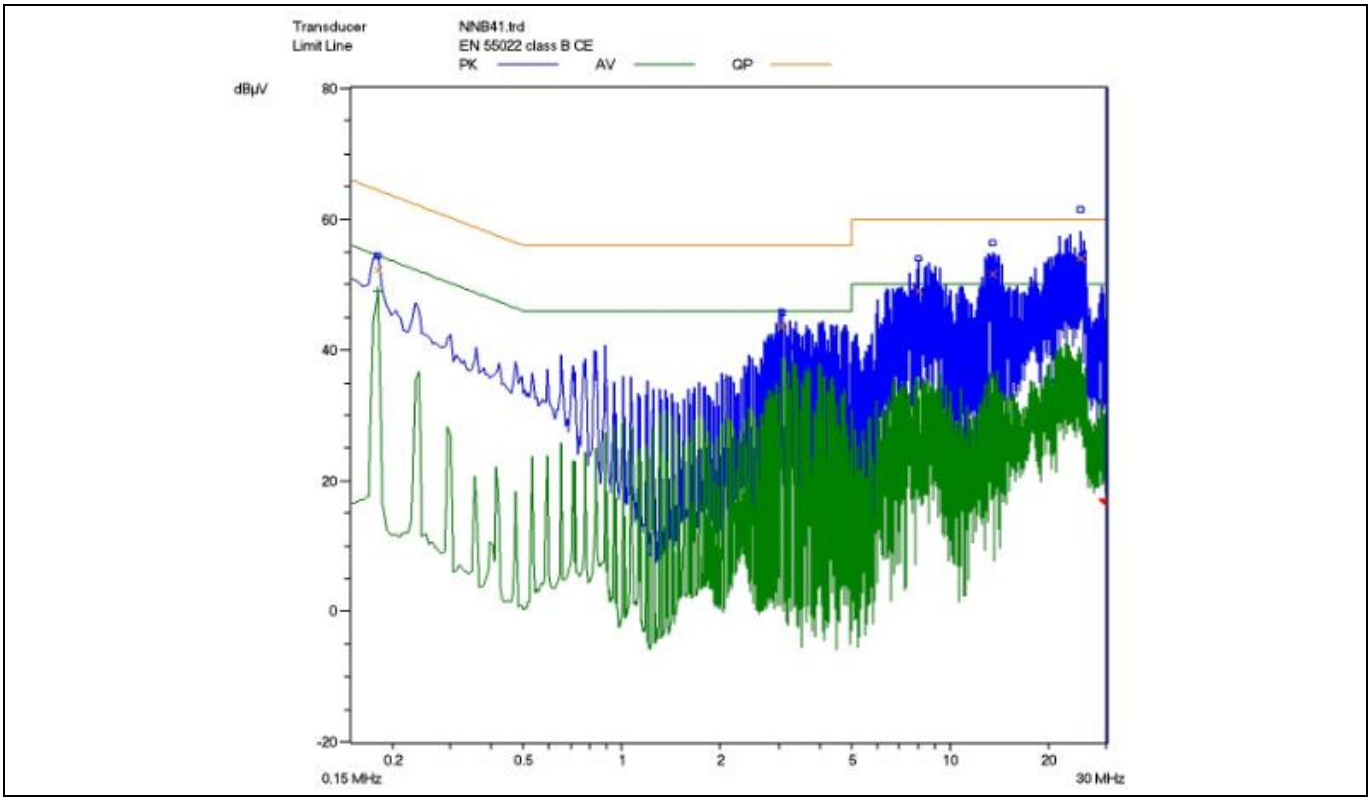


Figure 14 Conducted emissions (neutral) at 230 V AC and maximum load

Pass conducted emissions EN55022 (CISPR 22) class B with 6 dB margin for quasi-peak measurement at high line (230 V AC).

10.9 Thermal measurement

The thermal test of an open frame demo board was performed using an infrared thermography camera (TVS-500EX) at ambient temperature of 25°C. The measurements were taken after one hour running at full load.

Table 5 Hottest temperature of demo board

No.	Major component	85 V AC (°C)	300 V AC (°C)
1	IC11 (ICE5QSAG)	79.3	67.5
2	Q11 (IPA80R650CE)	51.3	61.7
3	R14 (current sense resistor)	59.5	48.2
4	TR1 (transformer)	87.2	102.5
5	BR1 (bridge diode)	58.7	38.2
6	R11(clamper resistor)	75.2	76.4
7	L11 (choke)	67.1	35.4
8	D21 (Secondary diode)	64.7	67.1
9	D22 (Secondary diode)	52.9	55.3
10	Ambient	25.0	25.0

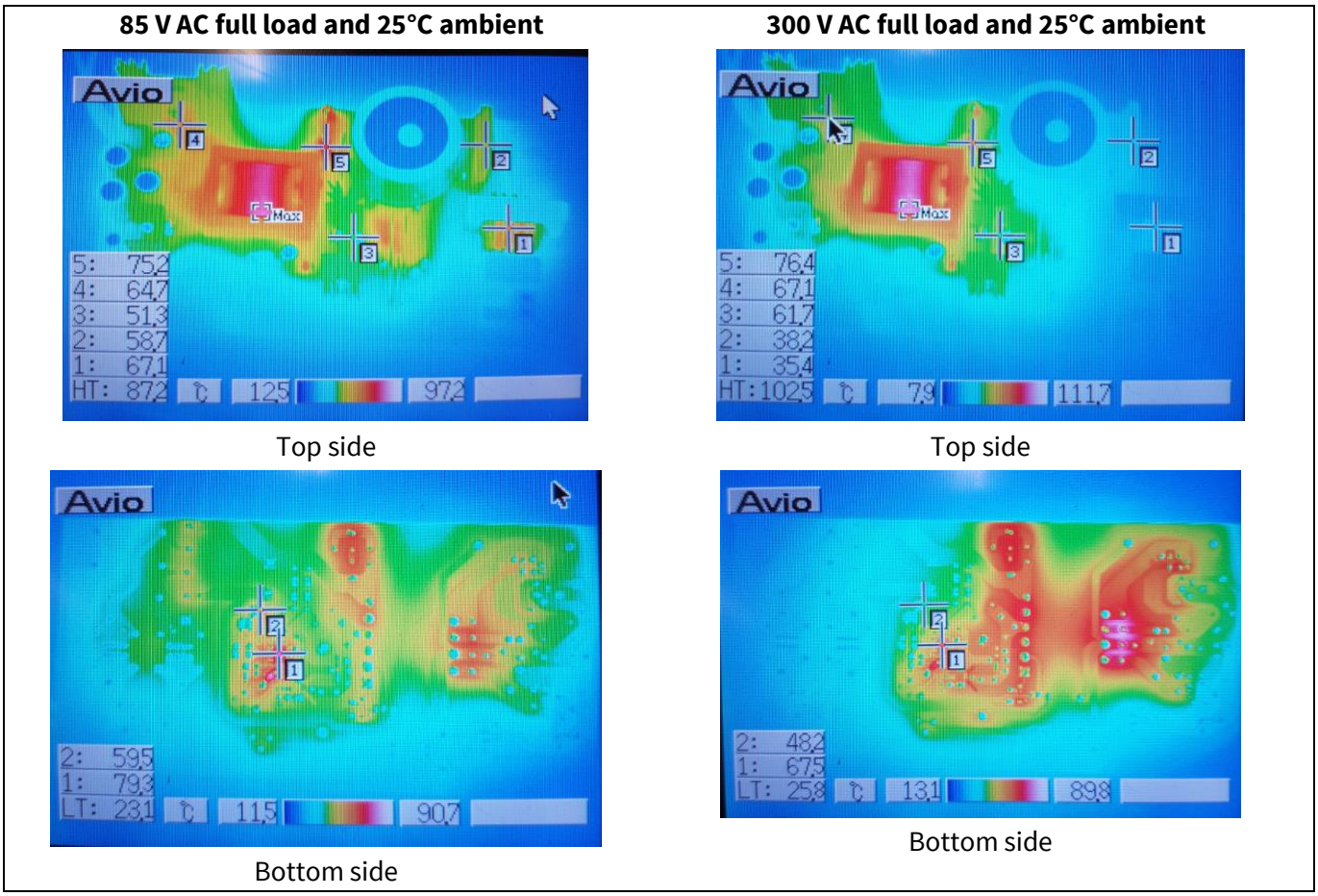


Figure 15 Infrared thermal image of DEMO_5QSAG_50W1

11 Waveforms and oscilloscope plots

All waveforms and scope plots were recorded with a TELEDYNE LECROY 606Zi oscilloscope.

11.1 Startup at low/high AC line input voltage with maximum load

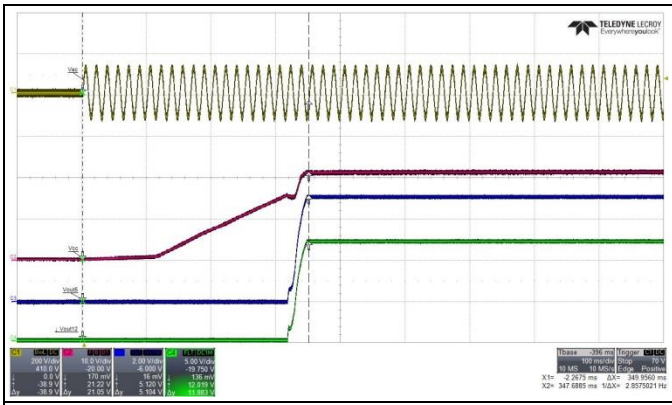
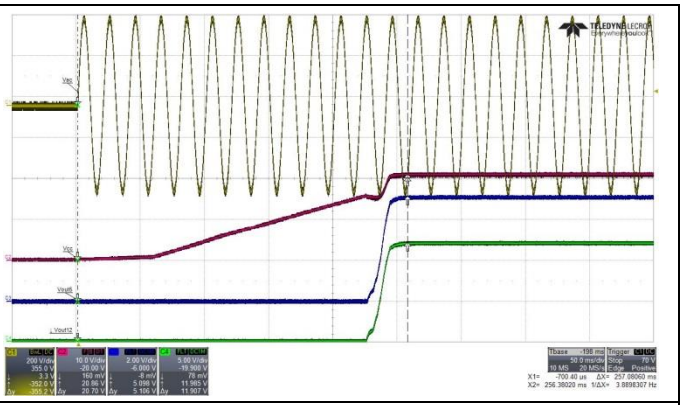
	
C1 (Yellow) : AC line voltage (V AC) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : 5 V output voltage (V_{Out5}) C4 (Green) : 12 V output voltage (V_{Out12})	C1 (Yellow) : AC line voltage (V AC) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : 5 V output voltage (V_{Out5}) C4 (Green) : 12 V output voltage (V_{Out12})
Startup time at 85 V AC and maximum load ≈ 350 ms	Startup time at 300 V AC and maximum load ≈ 257 ms

Figure 16 Startup

11.2 Soft start

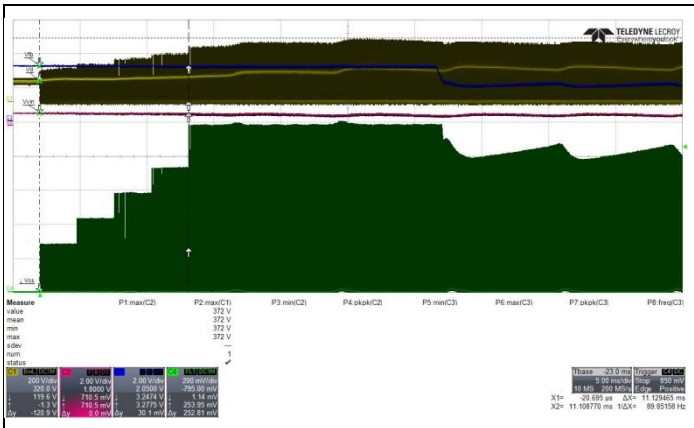
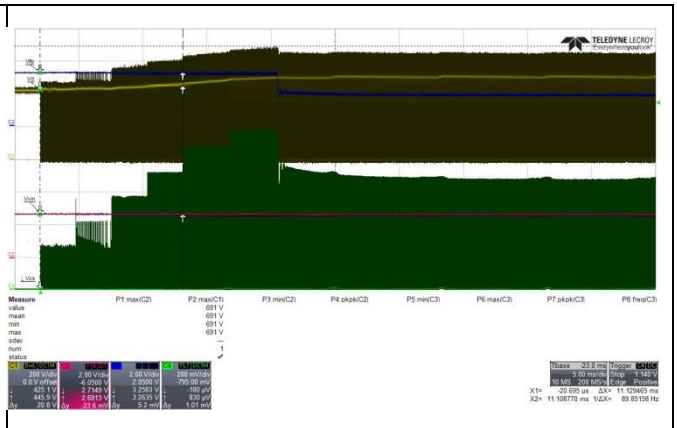
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
Soft-start time at 85 V AC and maximum load ≈ 11 ms	Soft-start time at 300 V AC and maximum load ≈ 11 ms

Figure 17 Soft start

11.3 Drain and current sense voltage at maximum load

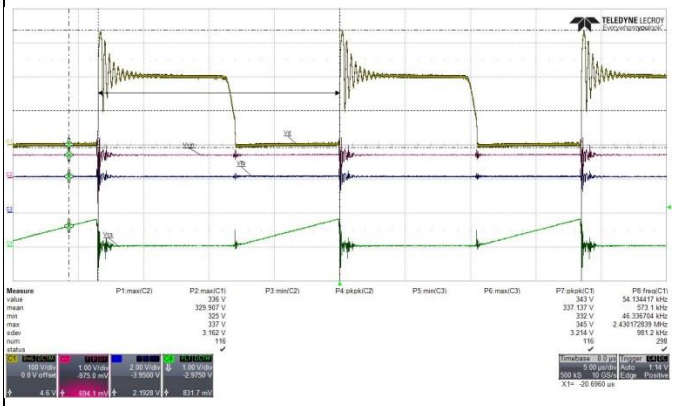
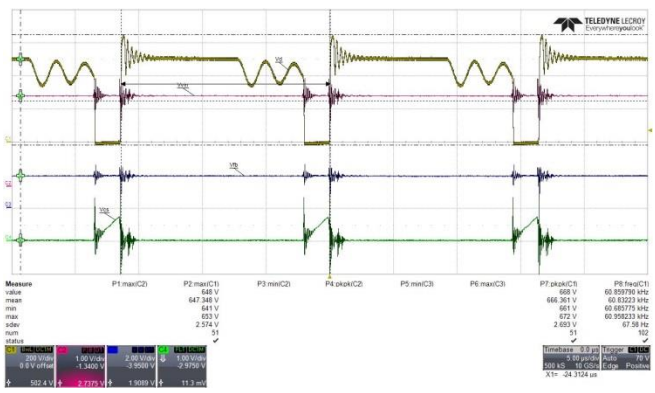
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
V_{Drain_peak} at 85 V AC ≈ 337 V with 1st ZC and f_S ≈ 46 kHz	V_{Drain_peak} at 300V AC ≈ 653 V with 3rd ZC and f_S ≈ 60 kHz

Figure 18 Drain and current sense voltage at maximum load

11.4 Zero crossing point during normal operation

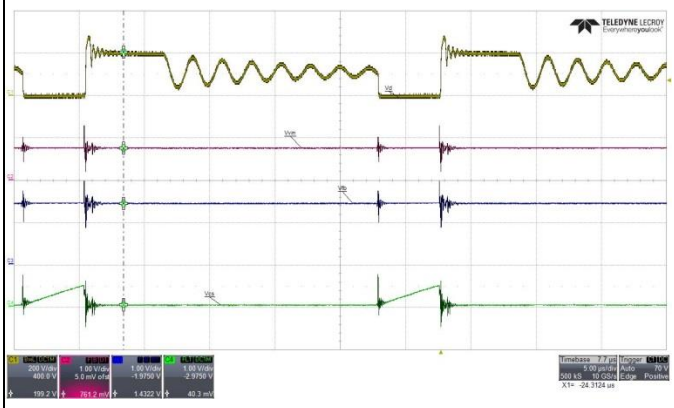
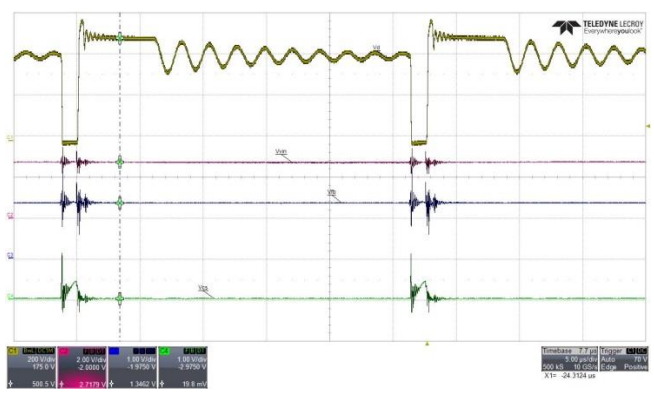
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
8th zero crossing at 85 V AC and 25% load (5 V x 0.25 A +12 V x 0.93 A) (zero crossing varies from 1~8 for low line)	10th zero crossing at 300 V AC and 25% load (5 V x 0.25 A +12 V x 0.93 A) (zero crossing varies from 3~10 for high line)

Figure 19 Zero crossing

11.5 Load transient response (dynamic load from 10% to 100%)

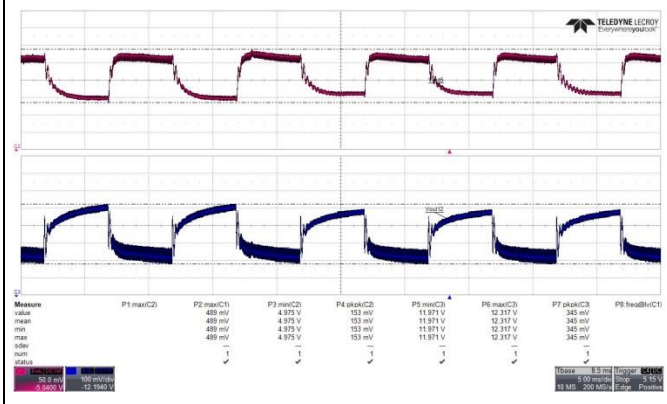
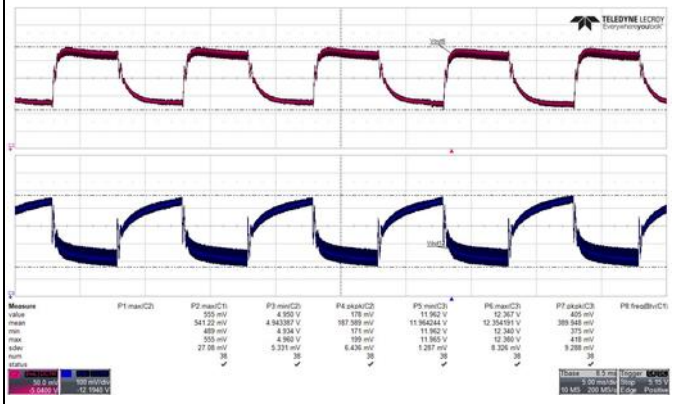
	
C2 (Purple) : 5 V output ripple voltage (V_{Out5}) C3 (Blue) : 12 V output ripple voltage (V_{Out12})	C2 (Purple) : 5 V output ripple voltage (V_{Out5}) C3 (Blue) : 12 V output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 153 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 345 mV (85 V AC, 12 V Load change from 10% to 100% and 5 V at 1 A load, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 199 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 418 mV (300 V AC, 12 V Load change from 10% to 100% and 5 V at 1 A load, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 20 Load transient response

11.6 Output ripple voltage at maximum load

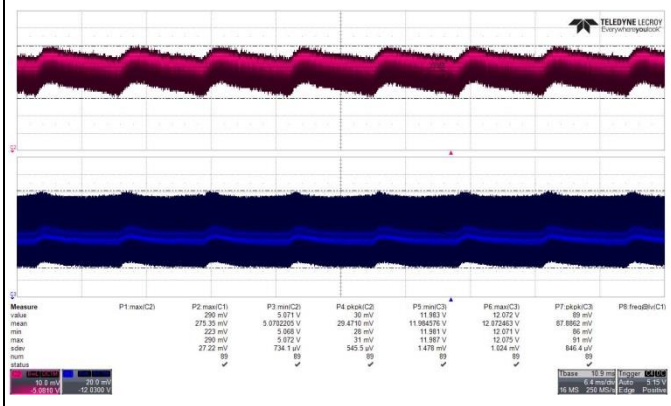
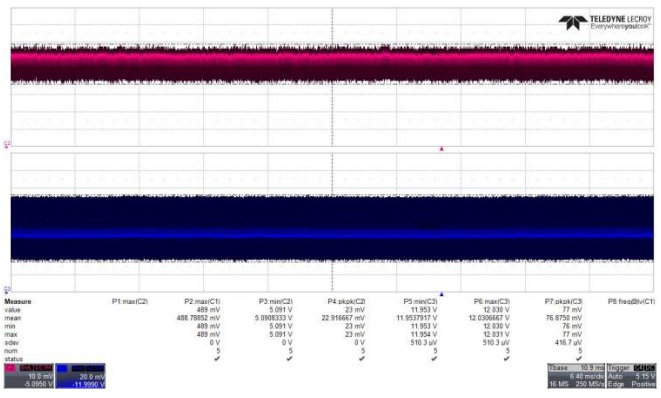
	
C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})	C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 31 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 91 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 23 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 77 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 21 Output ripple voltage at maximum load

11.7 Output ripple voltage at active burst mode 1 W load

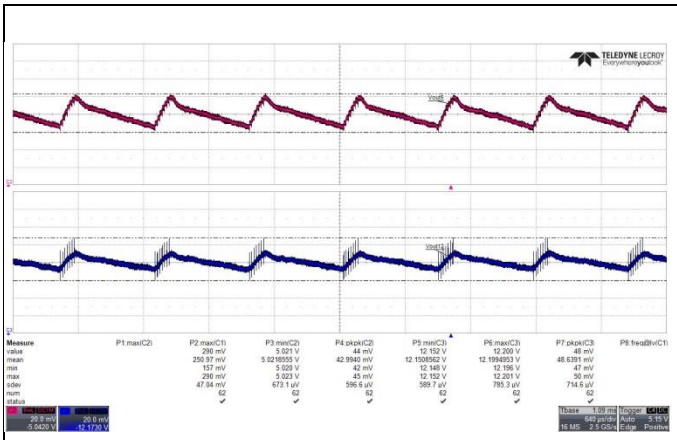
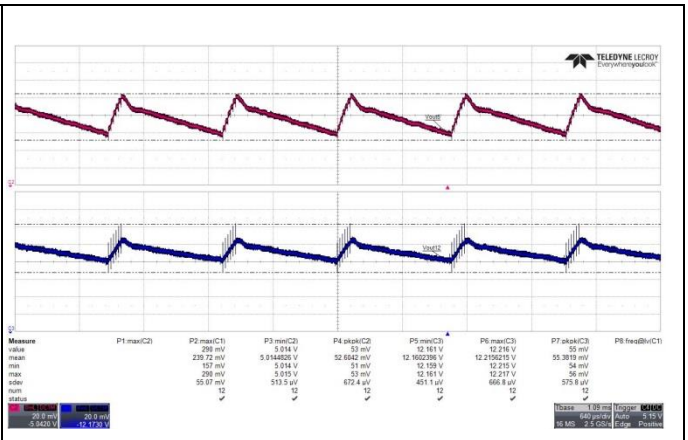
	
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 45 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 50 mV Load: 5 V at 60 mA and 12 V at 58 mA Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 53 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 56 mV Load: 5 V at 60 mA and 12 V at 58 mA Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(electrolytic), 20 MHz filter
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 45 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 50 mV Load: 5 V at 60 mA and 12 V at 58 mA Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 53 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 56 mV Load: 5 V at 60 mA and 12 V at 58 mA Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(electrolytic), 20 MHz filter

Figure 22 Output ripple voltage at burst mode 1 W load

11.8 Entering active burst mode

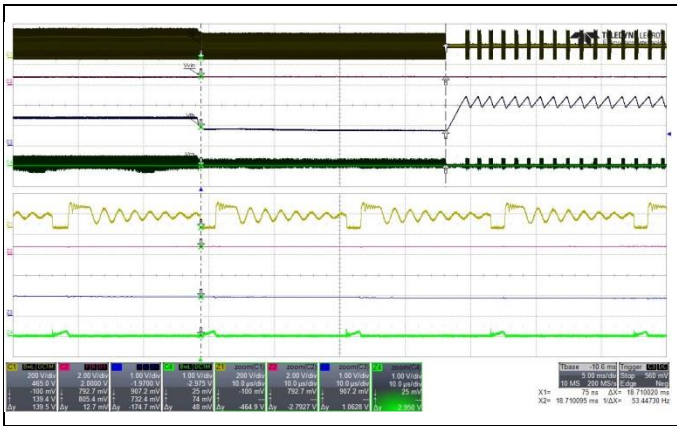
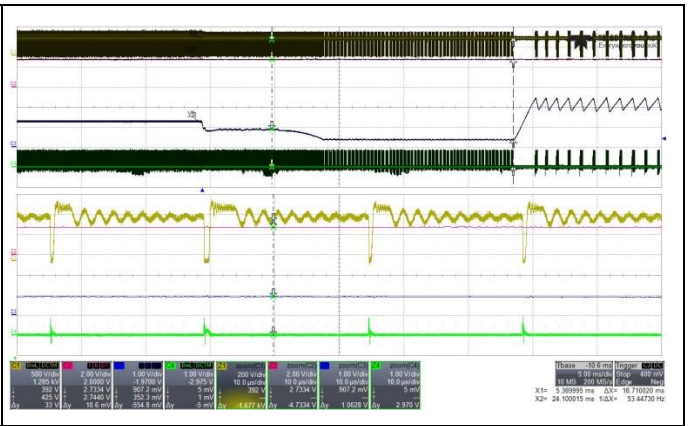
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
Condition to enter burst mode level 1 : V_{FB} < 0.9 V, N_{ZC} = 8 and $t_{blanking}$ = 20 ms (load change form 11.5 W [5 V, 60 mA & 12 V, 0.9375 A] to 1.5 W [5 V, 60 mA & 12 V, 0.1 A] at 85 V AC)	Condition to enter burst mode level 1 : V_{FB} < 0.9 V, N_{ZC} = 10 and $t_{blanking}$ = 20 ms (load change form 11.5 W [5 V, 60 mA & 12 V, 0.9375 A] to 1.5 W [5 V, 60 mA & 12 V, 0.1 A] at 300 V AC)

Figure 23 Entering active burst mode

11.9 During active burst mode

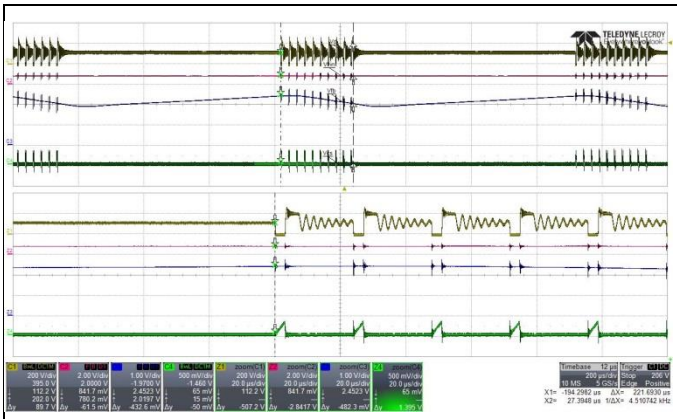
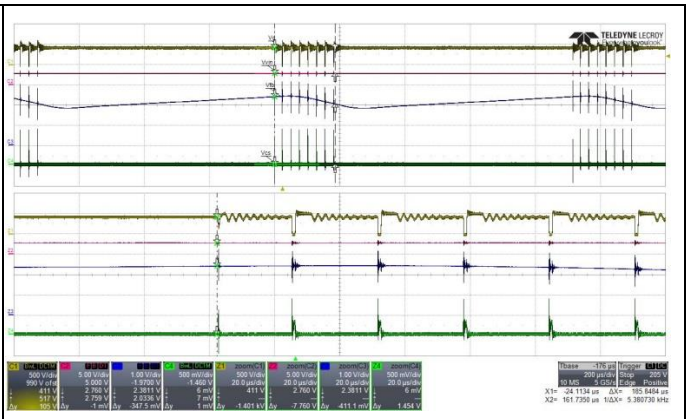
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
During active burst mode level 1 : V_{FB_BOn}=2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 8 (1.5 W [5 V, 60 mA & 12 V, 0.1 A] at 85 V AC)	During active burst mode level 1 : V_{FB_BOn}=2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 10 (1.5 W [5 V, 60 mA & 12 V, 0.1 A] at 300 V AC)

Figure 24 During active burst mode

11.10 Leaving active burst mode

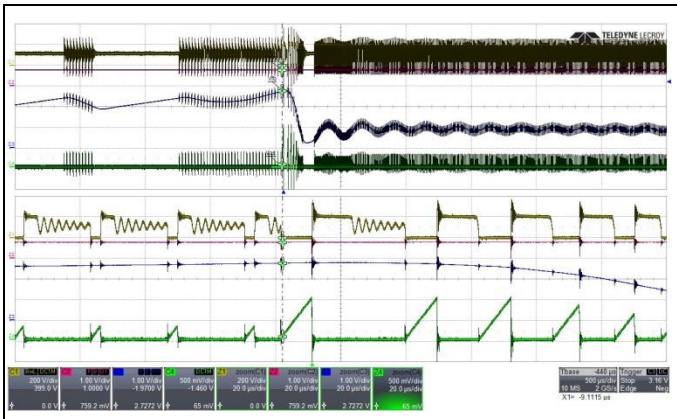
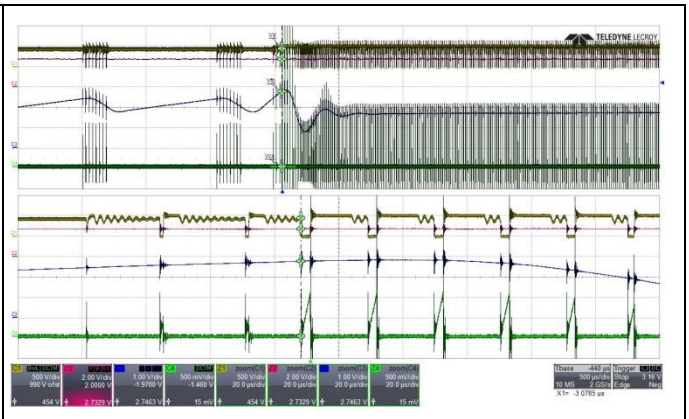
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
Condition to leave burst mode level 1 : V_{FB} >2.75 V (load change form 1.5 W [5 V, 60 mA & 12 V, 0.1 A] to full load at 85 V AC)	Condition to leave burst mode level 1 : V_{FB} >2.75 V (load change form 1.5 W [5 V, 60 mA & 12 V, 0.1 A] to full load at 300 V AC)

Figure 25 Leaving active burst mode

11.11 Line over voltage protection (non switch auto restart)

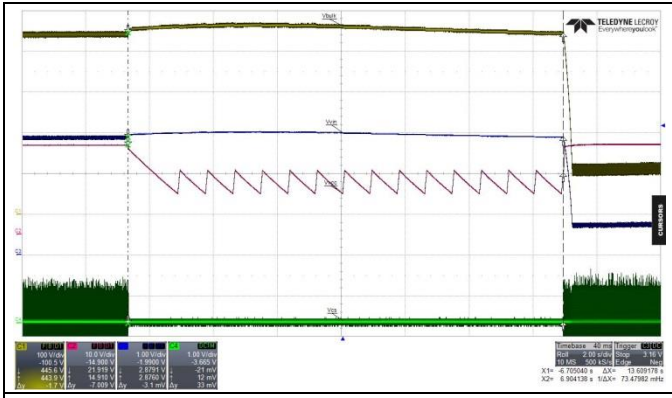
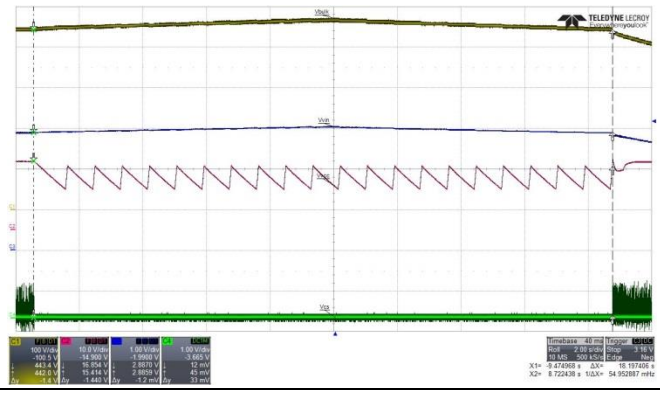
<table>
<tr><td>  </td><td>  </td></tr>
<tr><td>C1 (Yellow) : Bulk voltage (V_{Bulk})
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : VIN voltage (V_{VIN})
C4 (Green) : Current sense voltage (V_{CS})</td><td>C1 (Yellow) : Bulk voltage (V_{Bulk})
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : VIN voltage (V_{VIN})
C4 (Green) : Current sense voltage (V_{CS})</td></tr>
<tr><td colspan="2">Condition to detect Line over voltage protection : V_{VIN} > 2.9 V (V_{BULK} > 442 V DC [≈320 V AC])
Condition to reset Line over voltage protection : V_{VIN} < 2.9 V (V_{BULK} < 442 V)</td></tr>
<tr><td>(Gradually increase AC line voltage at full load till Line OVP detect and decrease AC line till Line OVP reset)</td><td>(Gradually increase AC line voltage at 1 W load [5 V, 60 mA & 12 V, 0.058 A] (Active burst mode) till Line OVP detect and decrease AC line till Line OVP reset)</td></tr>
</table>

Figure 26 Line over voltage protection

11.12 Brownout protection (non switch auto restart)

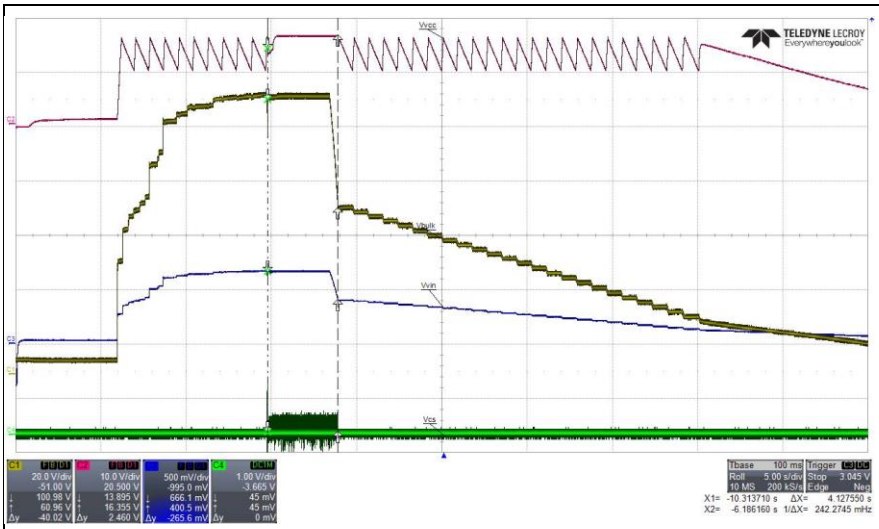
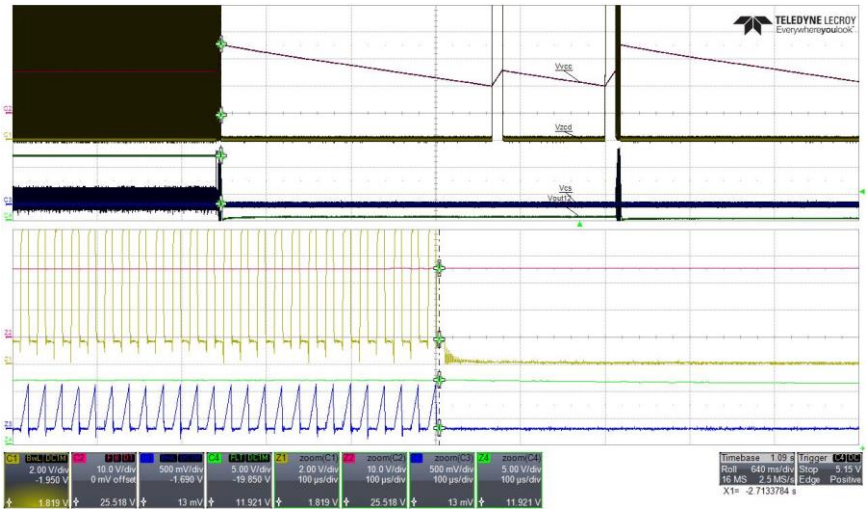
<table>
<tr><td colspan="2">  </td></tr>
<tr><td colspan="2">C1 (Yellow) : Bulk voltage (V_{Bulk})
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : VIN voltage (V_{VIN})
C4 (Green) : Current sense voltage (V_{CS})</td></tr>
<tr><td colspan="2">Condition to reset Brownout protection (Brownin) : V_{VIN} > 0.66 V (V_{BULK} > 100 V DC [≈73 V AC])
Condition to detect Brownout protection : V_{VIN} < 0.4 V (V_{BULK} < 61 V_{DC} [≈44 V AC])</td></tr>
<tr><td colspan="2">(Gradually increase AC line voltage at active burst mode 1 W [5 V, 60 mA & 12 V, 0.058 A] load until the system starts switching and reduce the line until brownout is detected)</td></tr>
</table>

Figure 27 Brownout protection

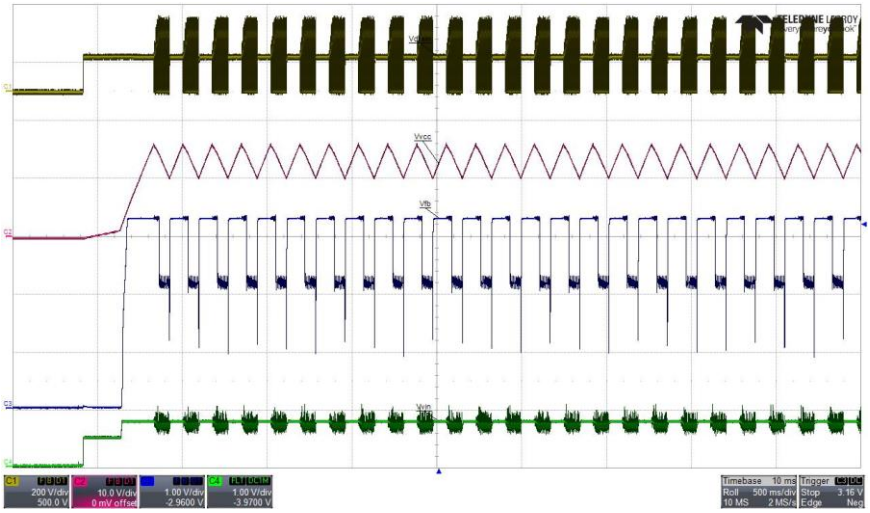
11.13 V_{CC} over voltage protection (odd skip auto restart)



C1 (Yellow)	: Zero crossing detection voltage (V_{ZCD})
C2 (Purple)	: Supply voltage (V_{VCC})
C3 (Blue)	: 12 V output voltage (V_{O12})
C4 (Green)	: Current sense voltage (V_{CS})
Condition to enter V_{VCC} over voltage protection: V_{VCC} > 25.5 V (85 V AC and remove R13, load change form no load to full load)	

Figure 28 V_{CC} over voltage protection

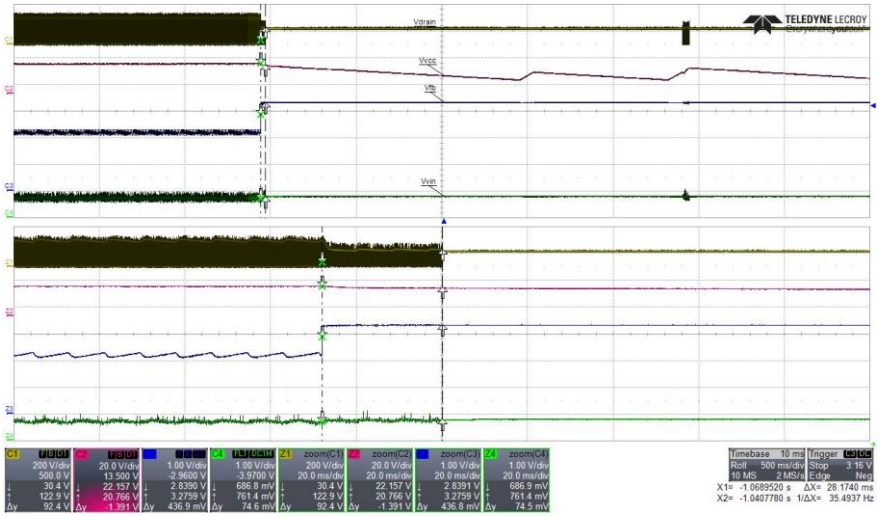
11.14 V_{CC} under voltage protection (auto restart)



C1 (Yellow)	: Drain voltage (V_D)
C2 (Purple)	: Supply voltage (V_{VCC})
C3 (Blue)	: Feedback voltage (V_{FB})
C4 (Green)	: V_{IN} voltage (V_{VIN})
Condition to enter VCC under voltage protection: V_{CC} < 10 V (Remove R12A and power on the system with full load at 85 V AC)	

Figure 29 V_{CC} under voltage protection

11.15 Over load protection (odd skip auto restart)

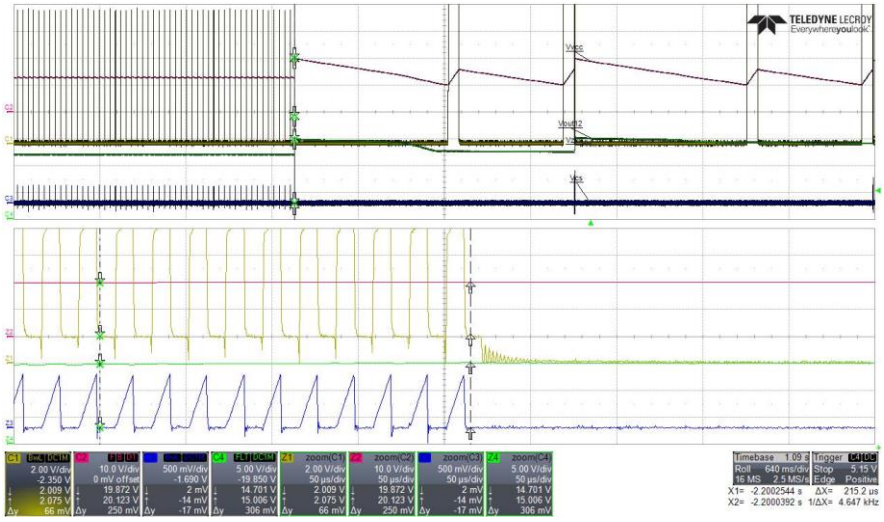


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : Feedback voltage (V_{FB})
C4 (Green) : VIN voltage (V_{VIN})

Condition to enter over load protection: V_{FB} > 2.75 V & last for 30 ms blanking time
(5 V at 1 A while 12 V load change from full to short at 85 V AC)

Figure 30 Over load protection

11.16 Output over voltage protection (odd skip auto restart)

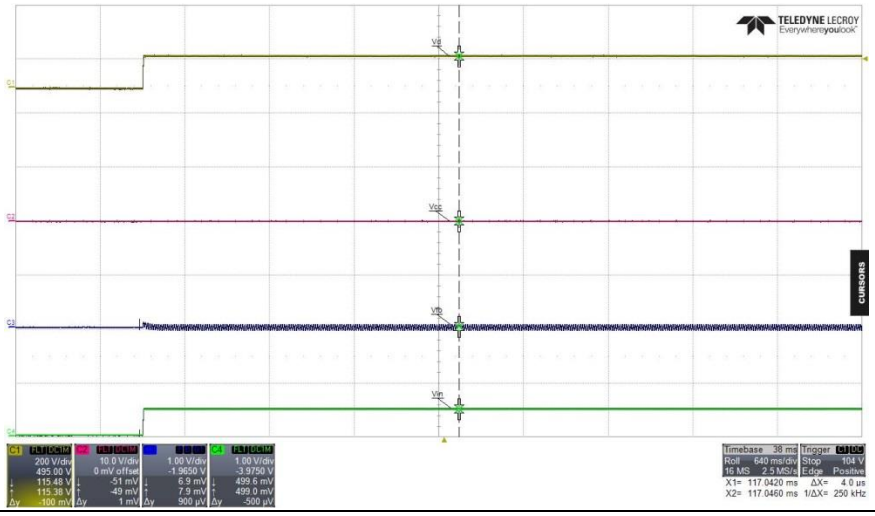


C1 (Yellow) : Zero crossing detection voltage (V_{ZCD})
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : Current sense voltage (V_{CS}) 12 V output voltage (V_{O12})
C4 (Green) : 12 V output voltage (V_{O12})

Condition to enter output OVP: V_{O12}>14 V (V_{ZCD}>2 V)
(85 V AC, short R26 during system operation at no load)

Figure 31 Output over voltage protection

11.17 V_{CC} short to GND protection



C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : VCC voltage (V_{VCC})
C3 (Blue) : Feedback voltage (V_{FB})
C4 (Green) : VIN voltage (V_{VIN})

Condition to enter V_{CC} short to GND : if $V_{CC} < V_{VCC\_SCP}$ $I_{VCC} = I_{VCC\_Charge1}$
(Short VCC pin to Gnd and measure the current with multi-metre before system startup, $I_{VCC} \approx 280$ µA and input power is ≈ 36 mW at 85 V AC)

Figure 32 V_{CC} short to GND protection

12 References

[1] ICE5QSAG datasheet, Infineon Technologies AG

[2] AN-201609_PL83_026-5th Generation Quasi-Resonant Design Guide

Revision history

Major changes since the last revision

Page or Reference	Description of change
--	First release.

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