MPC5748G Low Cost Evaluation Board (MPC5748G-LCEVB)

Table Of Contents:

Revision Information

Rev	Date	Designer	Comments
x1	14 Apr 2015	Alasdair Robertson	Start of capture, Working version (256BGA)
x2	08 May 2015	Alasdair Robertson	Changed to 176 QFP Package and changed periperhal Matrix
x3	18 May 2015	Alasdair Robertson	Changes required for initial placement
x4	19 May 2015	Alasdair Robertson	Tidy Up, Replaced some "hard to source" components
x5	26 May 2015	Alasdair Robertson	Renumber and Back Annoted from Layout
x6	27 May 2015	Alasdair Robertson	Correction to GND on 3v3 Regulator circuit
x7	29 May 2015	Alasdair Robertson	Correction to CAN Test points
x8	31 May 2015	Alasdair Robertson	Few refdes changes after layout tweaks
x9	01 Jun 2015	Alasdair Robertson	Correction to user LED Refdes after re-number
x10	01 Jun 2015	Alasdair Robertson	DNP Jumpers. 0 Ohm resistors added accross LIN jumpers
A	11 Jun 2015	Andrew MacDonald	Prototype Manufacture Release
AX1	29 Sep 2015	Alasdair Robertson	Prodn Build changes (LIN0 default to Slave, LIN1 Master only) PN Changed to MPC5748G-LCEVB
AX2	26 Oct 2015	Alasdair Robertson	Change to JTAG Pulls to meet latest RM Spec
AX3	29 Oct 2015	Alasdair Robertson	Changed RV1 current limit resistor. SW4 / SW5 refdes swap
AX4	09 Dec 2015	Alasdair Robertson	Pull DOWN on TCLK to mitigate against STANDBY exit issue.
AX5	20 Jan 2016	Alasdair Robertson	Updated NXP Logos
B	12 Feb 2016	Alasdair Robertson	Updated NXP Logos
B1	26 Aug 2016	Karthikeyan	The text mentioned as "Calypso" in all places updated to "MPC5748". Title block document number changed.

Caution:

These schematics are provided for reference purposes only.
As such,NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP MPC5748G family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and NXP does not assume any liability for such a hardware design.

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hile Pad Large (for standard 0.1" header).
Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2. 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

Automotive Microcontroller Applications
East Kilbride, Scotland

Designer: A. Robertson	Drawing Title: **MPC5748G-LCEVB**	
Drawn by: A. Robertson	Page Title: **Index and Title Page**	
Approved: A. Robertson	Size B / Document Number SCH-28822 PDF: SPF-28822	Rev B1
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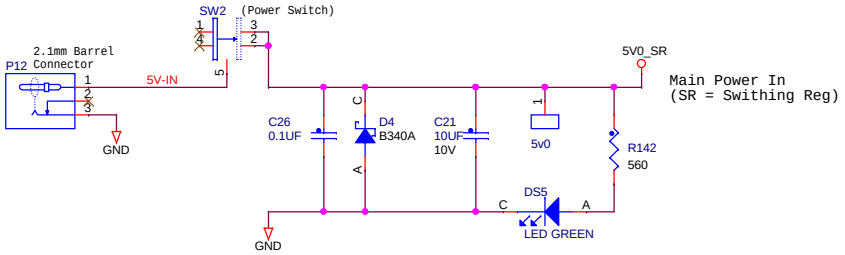
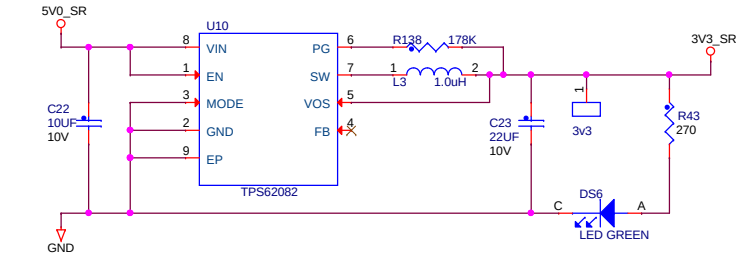
Power Input and Linear Voltage Regulators

Power Supply Input

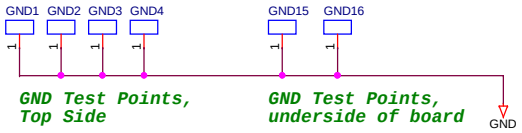


3.3v Switching Regulator



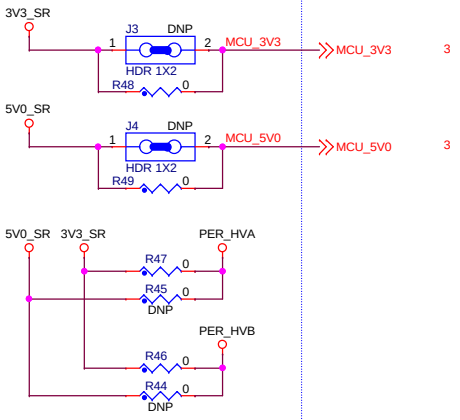
Inoput Voltage 5V, Output 3.3V at 700mA. Ripple 1.4mV, Approx 90% efficient

Test and reference points



Power Control

Jumpers can be fitted to facilitate power measurements



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MPC5748G MCU Power Connections

Power Supply Contraints:

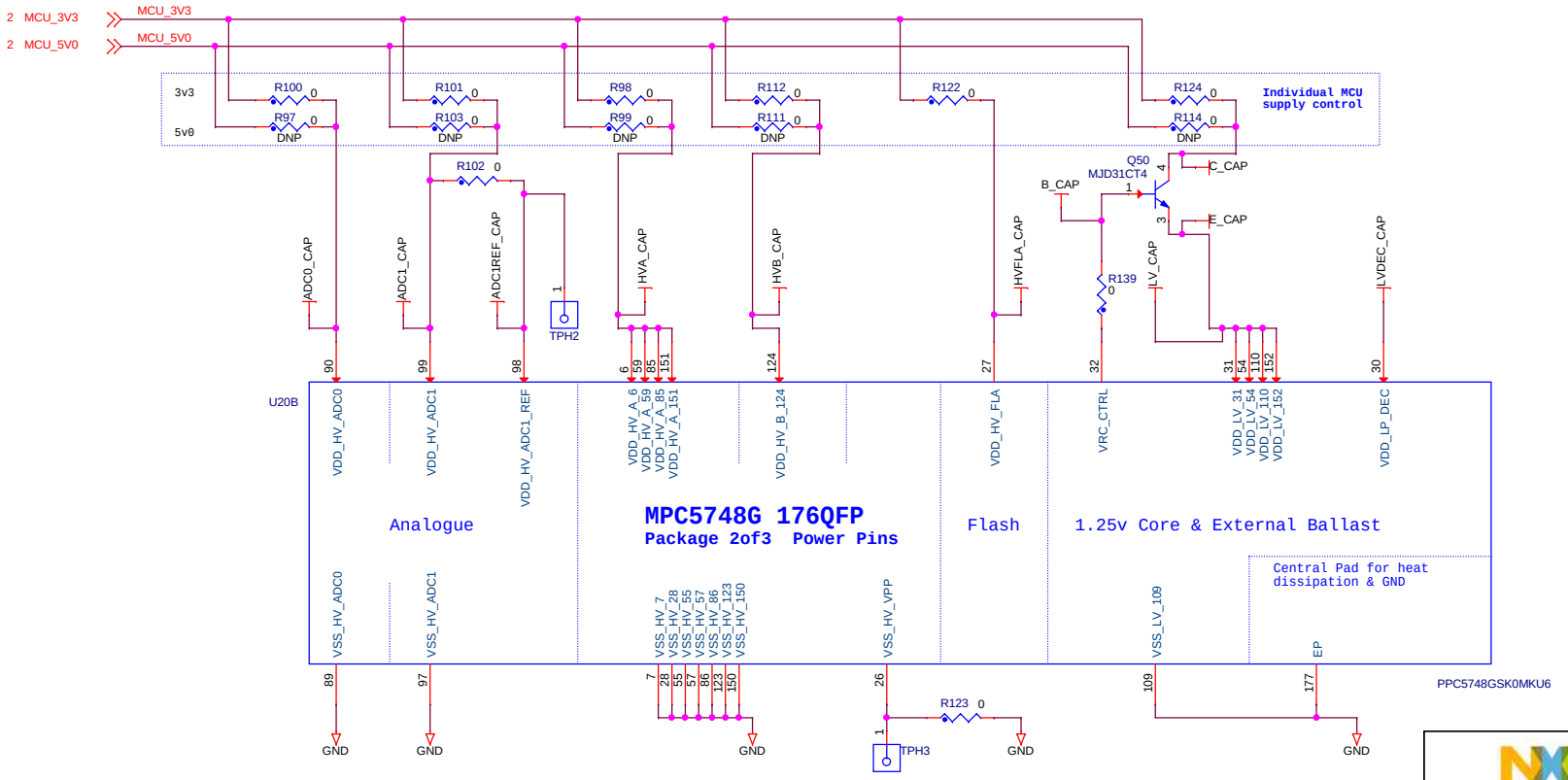
- If VDD_HV_A is driven from 3.3V, VDD_HV_FLA must also be supplied from 3.3V
- If VDD_HV_A is driven from 5V, the VDD_HV_FLA pin must be disconnected from 3.3V

- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protectrion on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuration:

- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD_HV_A, VDD_HV_B, VDD_HV_C, VBallast)
- VDD_HV_FLA = External 3.3V supplied (jumper fitted)

The analogue pins can only be driven to the same voltage as the VDD_HV_x domain they are situated in (ie max 3.3V) so makes sense for the analogue supply and reference to be 3.3V



Notes on signal Grounds:

- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue grond plane with single entry point (or ferrite) to digital ground plane.

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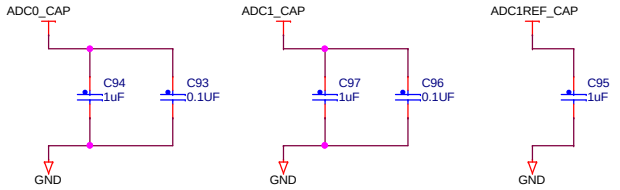
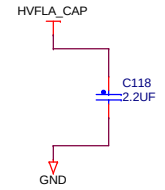
MPC5748G MCU Decoupling and bulk storage

ADC



Place small Caps as close as possible to MCU pins

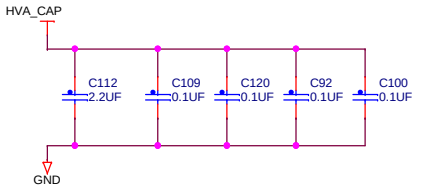
Flash



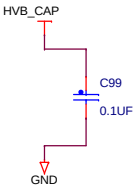
Capacitor Types:

```
4700pF - Ceramic X7R, 50V 10% 0402
0.1uF  - Ceramic X7R, 16V 10%  0402 (Kemet C0402C104K4RAC)
0.68uF - Ceramic X7R, 16V 10% 0805 (Murata GCM219R71C684KA37)
1uF    - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMK107B7105KA-T)
2.2uF  - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMK107B7225KA-TR)
```

VDD_HVA

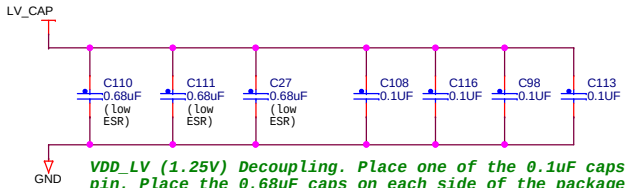


VDD_HVB



One 0.1uF cap per VDD_HV_x pin. Place as close as possible to pin

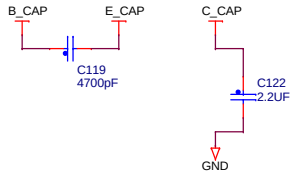
VDD_LV



VDD_LV (1.25V) Decoupling. Place one of the 0.1uF caps close to each VDD_LV pin. Place the 0.68uF caps on each side of the package such that there is no cap on the side with the ballast transistor

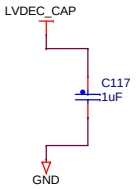
(For regulator stability the total capacitance should be around 2.2uF).

Ballast Transistor



Place close to transistor

LP Internal Reg Cap



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Drawing Title: MPC5748G-LCEVB		
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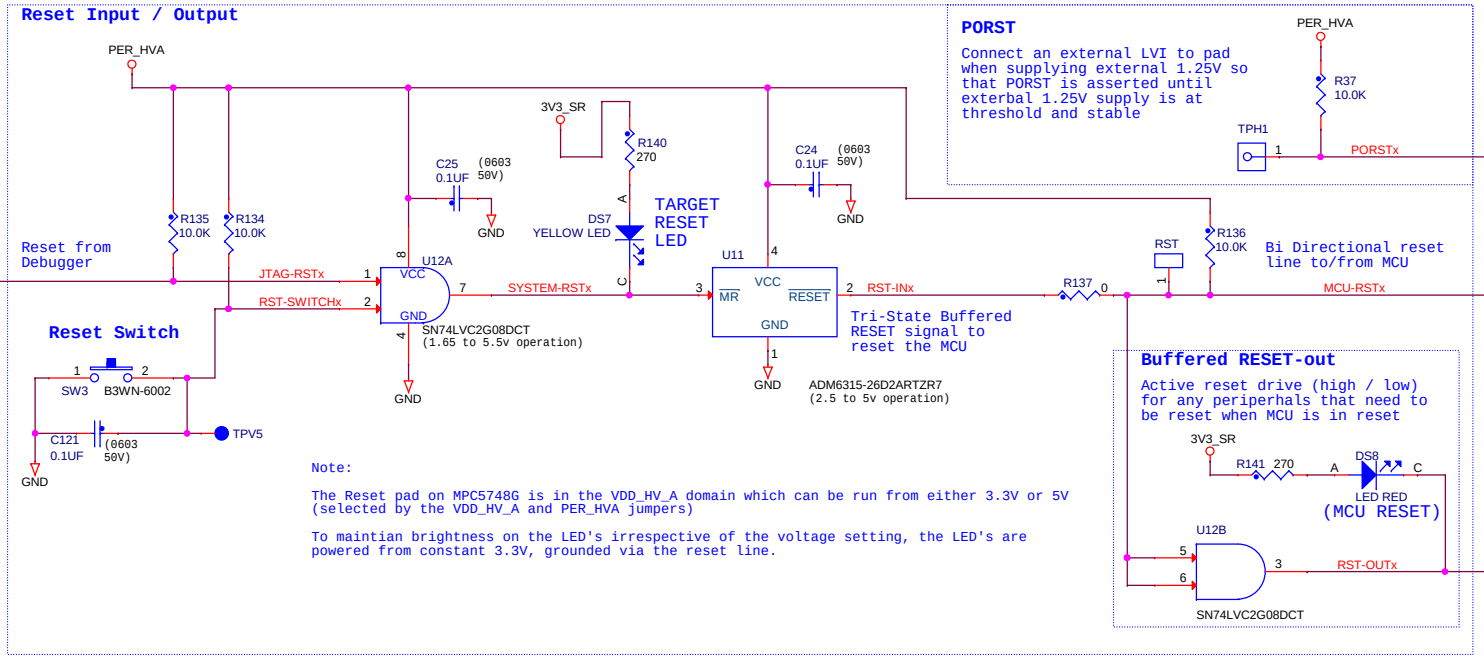
Reset and External Clock In

Reset is in the VDD_HVA domain.



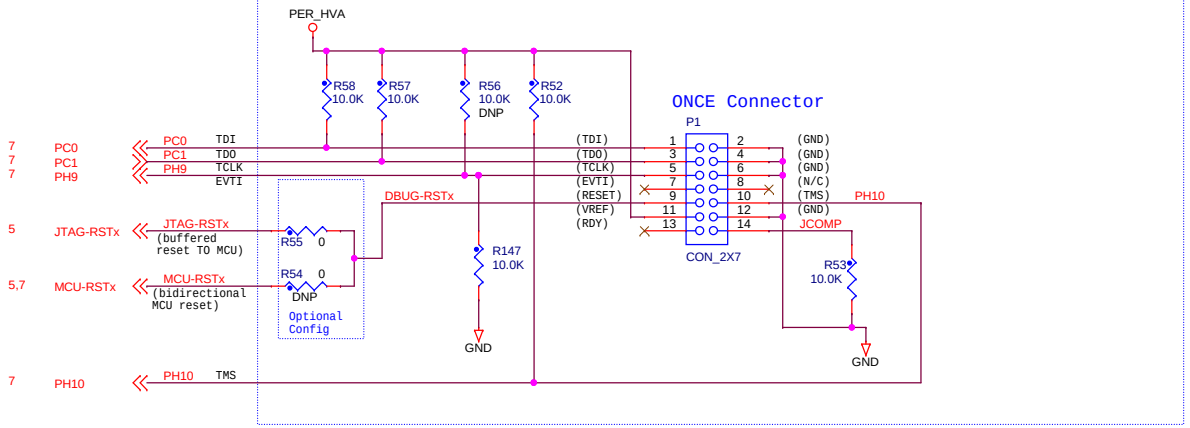


Table 13-3. Functional terminal state during power-up and reset

TERMINAL TYPE[1]	POWERUP pad state[2]	RESET pad state	DEFAULT pad state[3]	Comments
RESET	strong pull-down	strong pull-down	weak pull-up	functional reset pad.
PORST[4]	Weak pull down	Weak pull up	weak pull-up	power on reset pad.
GPIO	high impedance	high impedance	high impedance	by default, but configurable for STANDBY exit
ANALOG	high impedance	high impedance	high impedance	-
EOUT0, EOUT1	high impedance	high impedance	high impedance	
TCK	high impedance	weak pull-up	weak pull-up	-
TMS	high impedance	weak pull-up	weak pull-up	-
TDI	high impedance	weak pull-up	weak pull-up	-
TDO	high impedance	high impedance	high impedance	-
TCK_ALT	high impedance	weak pull-up	weak pull-up	-
TMS_ALT	high impedance	weak pull-up	weak pull-up	-
TDI_ALT	high impedance	weak pull-up	weak pull-up	-
TDO_ALT	high impedance	high impedance	high impedance	-

Note TCLK needs to be pulled down to allow exit from STANDBY in some corner cases

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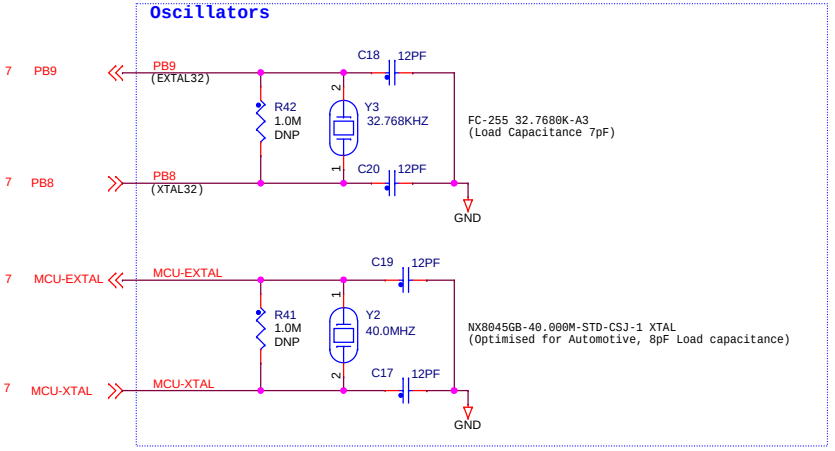
Clocks



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U20A

MPC5748G 176QFP

Package 1of3 GPIO Pins1

Key to text colours:

- Purple - Comms Physical Interfaces
- Orange - Other Peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- Black - Clock, Reset and Control
- RED - I/O Matrix and other functions (eg LED)
- Green - I/O Matrix (dedicated)

PA 12..15 has SPI

PD has ADC0 and ADC1

Sheet	Net	Function	Pin	Port
15	PA0	(GPIO)	24	PA0
14,15	PA1 (WKPU2 / NMI0)	(SW1 & GPIO**)	19	PA1
14,15	PA2 (WKPU3)	(SW2 & GPIO)	17	PA2
12	PA3	(MII_RXCLK)	114	PA3
15	PA4	(GPIO)	51	PA4
15	PA5	(GPIO)	146	PA5
15	PA6	(GPIO)	147	PA6
12	PA7	(MII_RXD2)	128	PA7
12	PA8	(RMII_RXD1)	129	PA8
12	PA9	(RMII_RXD0)	130	PA9
12	PA10	(MII_COL)	131	PA10
12	PA11	(RMII_RXER)	132	PA11
15	PA12	(GPIO)	53	PA12
15	PA13	(GPIO)	52	PA13
15	PA14	(GPIO)	50	PA14
15	PA15	(GPIO)	48	PA15
9	PB0	(CAN0_TX)	39	PB0
9	PB1	(CAN0_RX)	40	PB1
9	PB2	(LIN0_TX)	176	PB2
9	PB3	(LIN0_RX)	1	PB3
14	PB4	(ADC_POT)	88	PB4
15	PB5	(GPIO)	91	PB5
15	PB6	(GPIO)	92	PB6
15	PB7	(GPIO)	93	PB7
6	PB8	(XTAL32)	61	PB8
6	PB9	(EXTAL32)	60	PB9
15	PB10	(GPIO)	62	PB10
15	PB11	(GPIO)	96	PB11
15	PB12	(GPIO)	101	PB12
15	PB13	(GPIO)	103	PB13
15	PB14	(GPIO)	105	PB14
15	PB15	(GPIO)	107	PB15
5	PC0	(TDI)	154	PC0
5	PC1	(TDO)	149	PC1
11	PC2	(USB1_CLK)	145	PC2
11	PC3	(USB1_DIR)	144	PC3
13	PC4	(FR_B_TX_EN)	159	PC4
13	PC5	(FR_A_TX)	158	PC5
9	PC6	(LIN1_TX)	44	PC6
9	PC7	(LIN1_RX)	45	PC7
10	PC8	(RS232_TX)	175	PC8
10	PC9	(RS232_RX)	2	PC9
9	PC10	(CAN1_TX)	36	PC10
9	PC11	(CAN1_RX)	35	PC11
13	PC12	(FR_DBG0)	173	PC12
13	PC13	(FR_DBG1)	174	PC13
13	PC14	(FR_DBG2)	3	PC14
13	PC15	(FR_DBG3)	4	PC15
14,15	PD0	(HEX1 & GPIO)	77	PD0
14,15	PD1	(HEX2 & GPIO)	78	PD1
14,15	PD2	(HEX3 & GPIO)	79	PD2
14,15	PD3	(HEX4 & GPIO)	80	PD3
15	PD4	(GPIO)	81	PD4
15	PD5	(GPIO)	82	PD5
15	PD6	(GPIO)	83	PD6
15	PD7	(GPIO)	84	PD7
15	PD8	(GPIO)	87	PD8
15	PD9	(GPIO)	94	PD9
15	PD10	(GPIO)	95	PD10
15	PD12	(GPIO)	100	PD12
15	PD13	(GPIO)	102	PD13
15	PD14	(GPIO)	104	PD14
15	PD15	(GPIO)	106	PD15
5	MCU-RSTx	MCU-RSTx	29	RESET
5	PORSTx	PORSTx	153	PORST
6	MCU-XTAL	MCU-XTAL	56	XTAL
6	MCU-EXTAL	MCU-EXTAL	58	EXTAL

Port	Pin	Net	Function	Sheet
PE0	18			
PE1	20			
PE2	156	PE2	(FR_A_TX_EN)	13
PE3	157	PE3	(FR_A_RX)	13
PE4	160	PE4	(FR_B_TX)	13
PE5	161	PE5	(FR_B_RX)	13
PE6	167			
PE7	168			
PE8	21			
PE9	22			
PE10	23			
PE11	25			
PE12	133	PE12	(MII_CRS)	12
PE13	127	PE13	(MII_RXD3)	12
PE14	136	PE14	(USB1_D2)	11
PE15	137	PE15	(USB1_D3)	11
PF0	63	PF0	(GPIO)	15
PF1	64	PF1	(GPIO)	15
PF2	65	PF2	(GPIO)	15
PF3	66	PF3	(GPIO)	15
PF4	67	PF4	(GPIO)	15
PF5	68	PF5	(GPIO)	15
PF6	69	PF6	(GPIO)	15
PF7	70	PF7	(GPIO)	15
PF8	42	PF8	(GPIO)	15
PF9	41	PF9	(GPIO)	15
PF10	46	PF10	(GPIO)	15
PF11	47	PF11	(GPIO)	15
PF12	43	PF12	(GPIO)	15
PF13	49	PF13	(GPIO)	15
PF14	126	PF14	(RMII_MDIO)	12
PF15	125	PF15	(RMII_RXDV)	12
PG0	122	PG0	(RMII_MDC)	12
PG1	121	PG1	(RMII_TXCLK)	12
PG2	16	PG2	(LED1 & GPIO)	14 (eMIOS E1UC_11_H)
PG3	15	PG3	(LED2 & GPIO)	14 (eMIOS E1UC_12_H)
PG4	14	PG4	(LED3 & GPIO)	14 (eMIOS E1UC_13_H)
PG5	13	PG5	(LED4 & GPIO)	14 (eMIOS E1UC_14_H)
PG6	38	PG6	(CLKOUT1 GPIO)	PG6 (1)
PG7	37	PG7	(CLKOUT0 GPIO)	PG7 (1)
PG8	34			
PG9	33			
PG10	138	PG10	(USB1_D4)	11
PG11	139	PG11	(USB1_D5)	11
PG12	116	PG12	(MII_TXD2)	12
PG13	115	PG13	(MII_TXD3)	12
PG14	134	PG14	(USB1_D0)	11
PG15	135	PG15	(USB1_D1)	11
PH0	117	PH0	(RMII_TXD1)	12
PH1	118	PH1	(RMII_TXD0)	12
PH2	119	PH2	(RMII_TXEN)	12
PH3	120			
PH4	162			
PH5	163			
PH6	164			
PH7	165			
PH8	166			
PH9	155	PH9	(TCK)	5
PH10	148	PH10	(TMS)	5
PH11	140	PH11	(USB1_D6)	11
PH12	141	PH12	(USB1_D7)	11
PH13	9			
PH14	10			
PH15	8			

PPC5748GSK0MKU6

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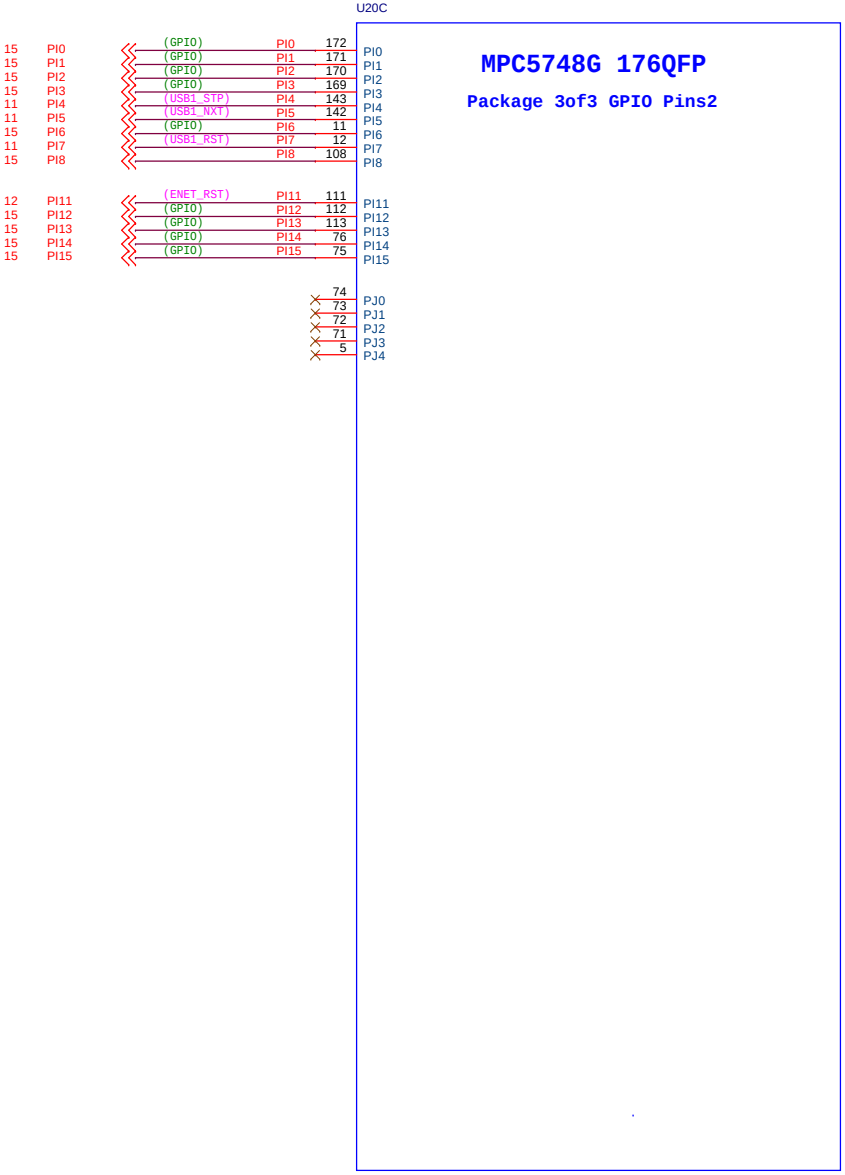
Key to text colours:
Purple - Comms Physical Interfaces
Orange - Other Peripherals and I/O
Blue - Debug (JTAG & Nexus)
Black - Clock, Reset and Control
RED - I/O Matrix and other functions (eg LED)
Green - I/O Matrix (dedicated)



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CAN & LIN Physical

All CAN and LIN signals are in power domain VDD_HV_A.

All interfaces will work at 3.3V or 5.0V (PER_HVA)

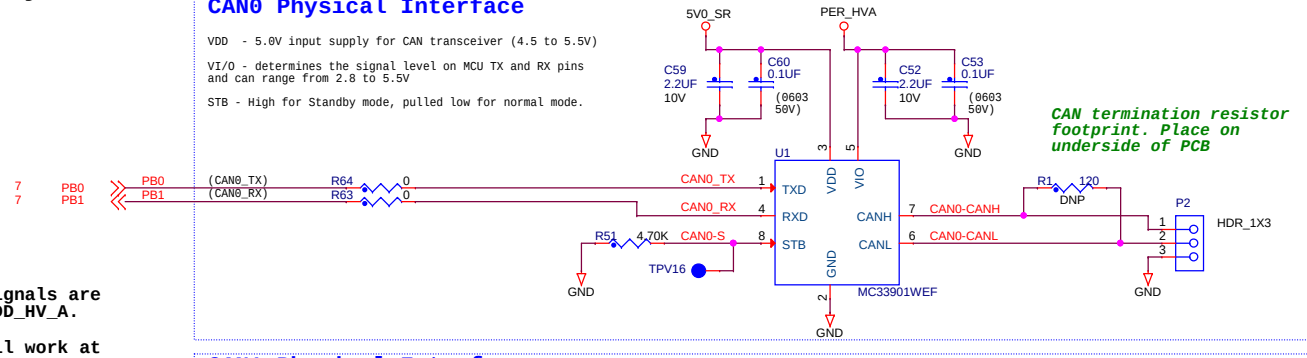
CAN0 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)

VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V

STB - High for Standby mode, pulled low for normal mode.

CAN termination resistor footprint. Place on underside of PCB



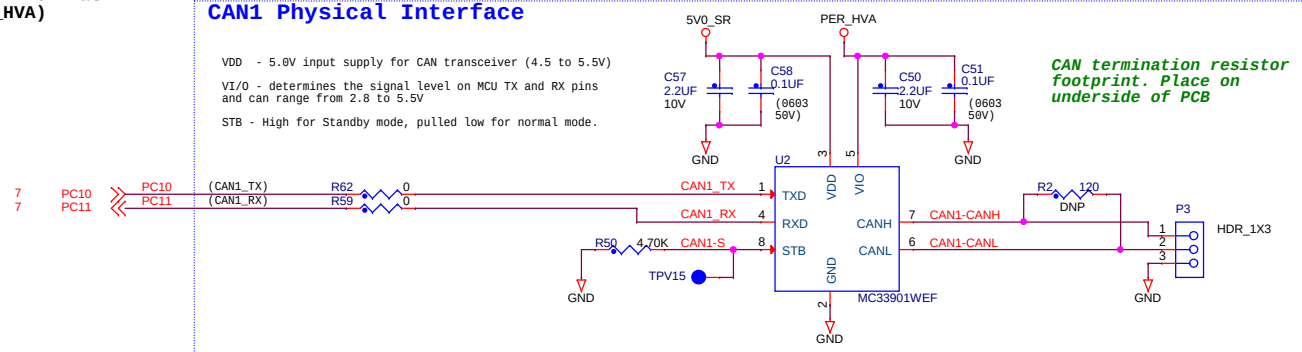
CAN1 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)

VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V

STB - High for Standby mode, pulled low for normal mode.

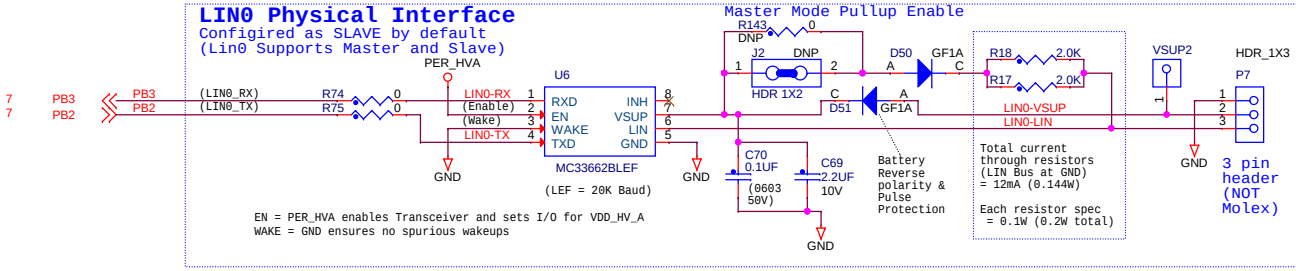
CAN termination resistor footprint. Place on underside of PCB



LIN0 Physical Interface

Configired as SLAVE by default
(Lin0 Supports Master and Slave)

Master Mode Pullup Enable

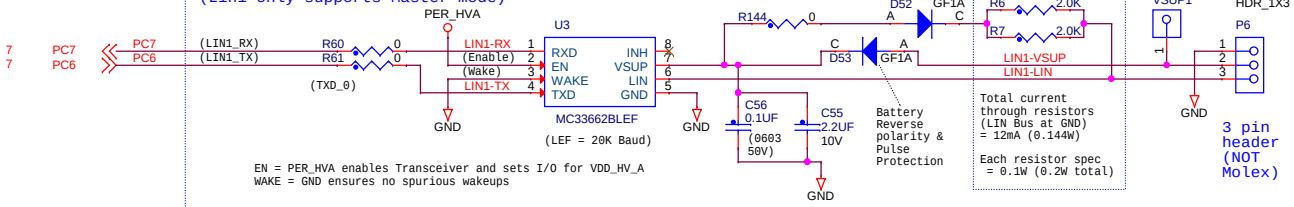


EN = PER_HVA enables Transceiver and sets I/O for VDD_HV_A
WAKE = GND ensures no spurious wakeups

LIN1 Physical Interface

Configired as MASTER by default
(Lin1 only supports Master mode)

Master Mode Pullup Enable



EN = PER_HVA enables Transceiver and sets I/O for VDD_HV_A
WAKE = GND ensures no spurious wakeups

MC33662LEF LIN transceiver is newer version of 33661 offering:

- Full LIN compliance (33661 no longer compliant)
- Improved ESD protection on LIN pin up to 15KV
- Improved ESD on Wake and VSUP Pins
- Other EMC and performance improvements

See freescale.com for more details

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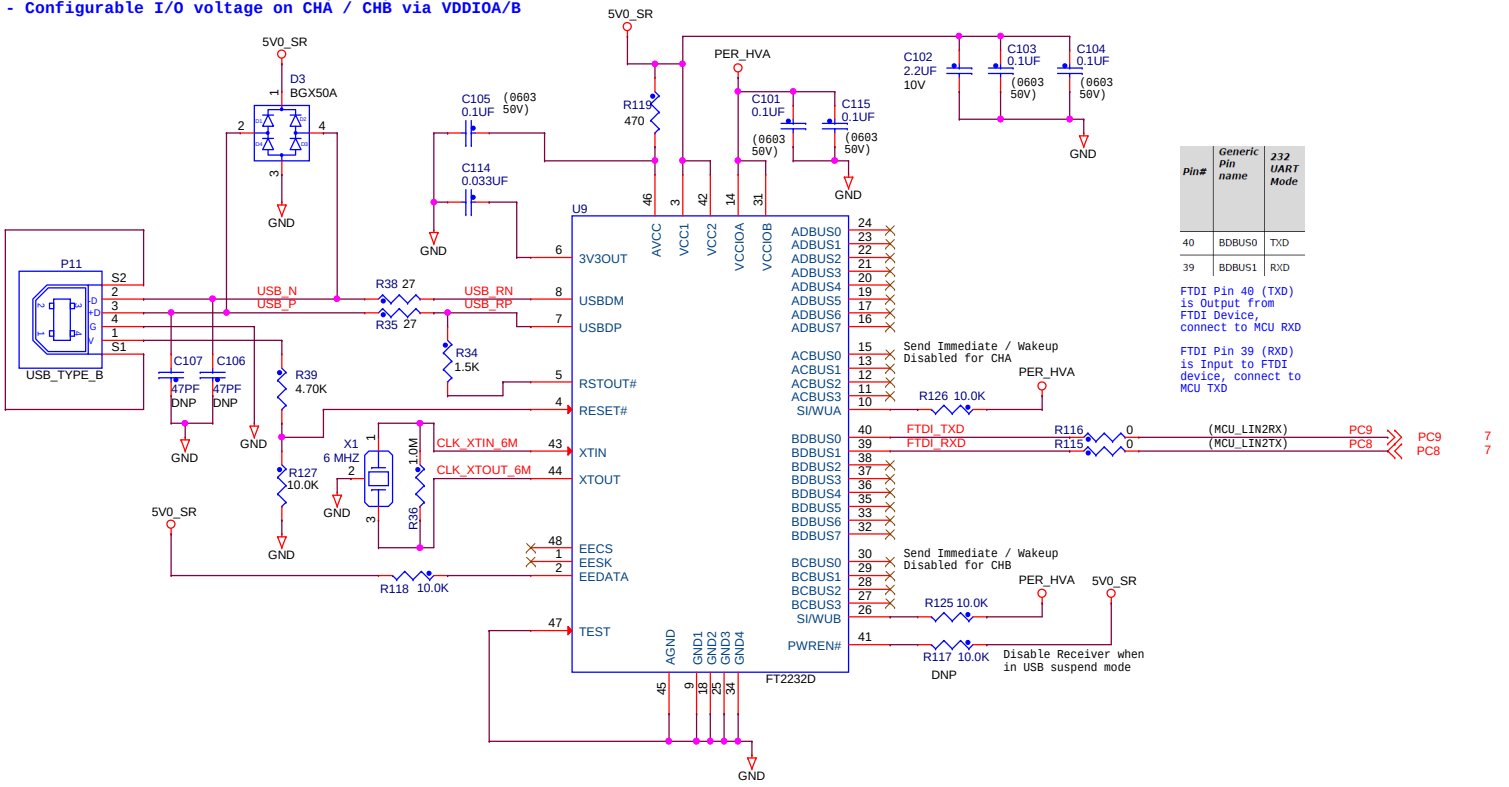
USB RS232 (serial) Interface

All Signals are in power domain VDD_HV_A.

FTDI interface will work at 3.3V or 5.0V (PER_HVA)

FTDI USB <-> Serial Interface

- Self Powered mode. No power is taken from USB
- Device efaults to Dual serial (RS232) mode ie RS232 on both A and B
- Configurable I/O voltage on CHA / CHB via VDDIOA/B



Pin#	Generic Pin name	232 UART Mode
40	BDBUS0	TXD
39	BDBUS1	RXD

FTDI Pin 40 (TXD) is Output from FTDI Device, connect to MCU RXD

FTDI Pin 39 (RXD) is Input to FTDI device, connect to MCU TXD

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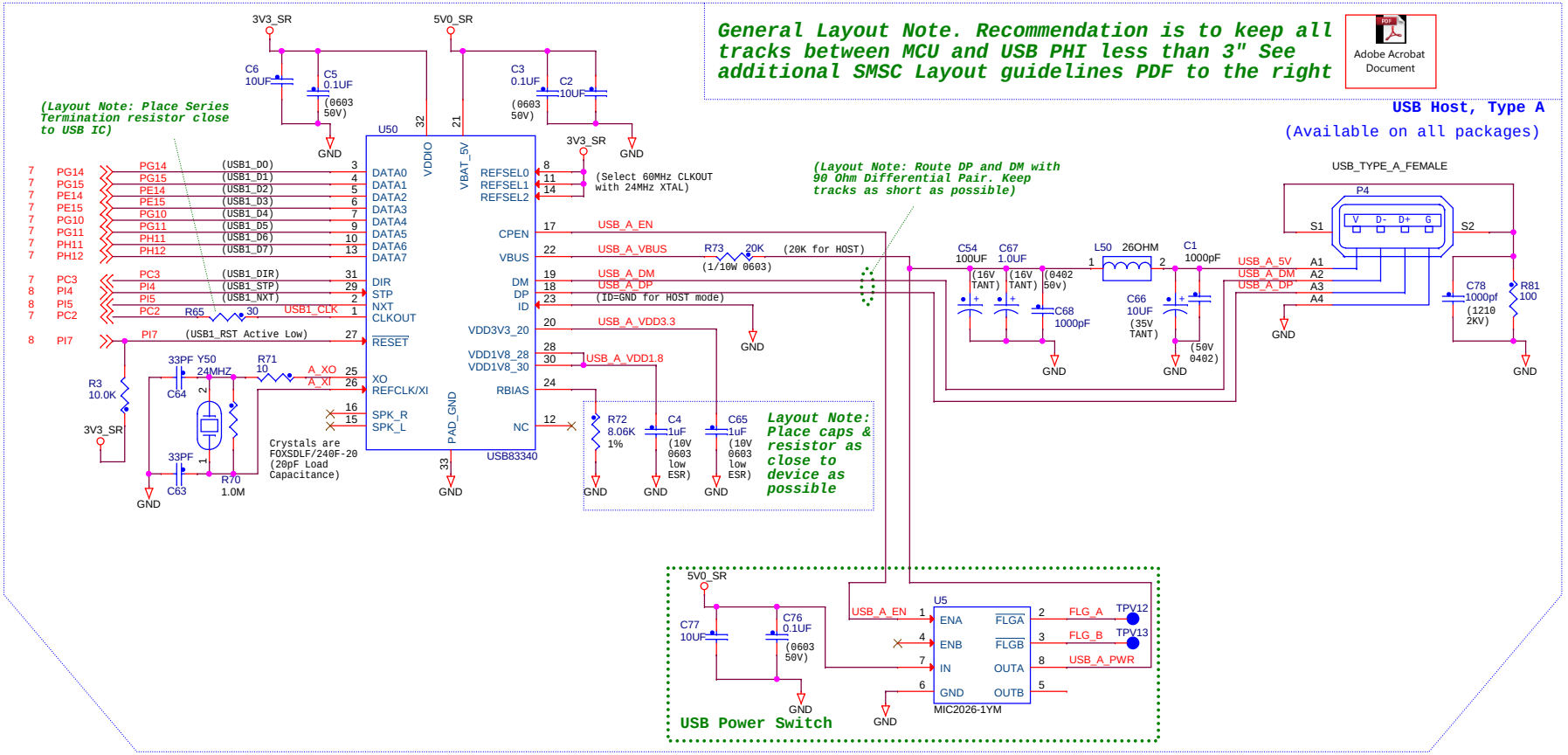
USB (Type A Host and Type AB OTG)

USB Signals are in power domain VDD_HV_A

The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, USB MCU pads must be left as tri-state with no pullups.



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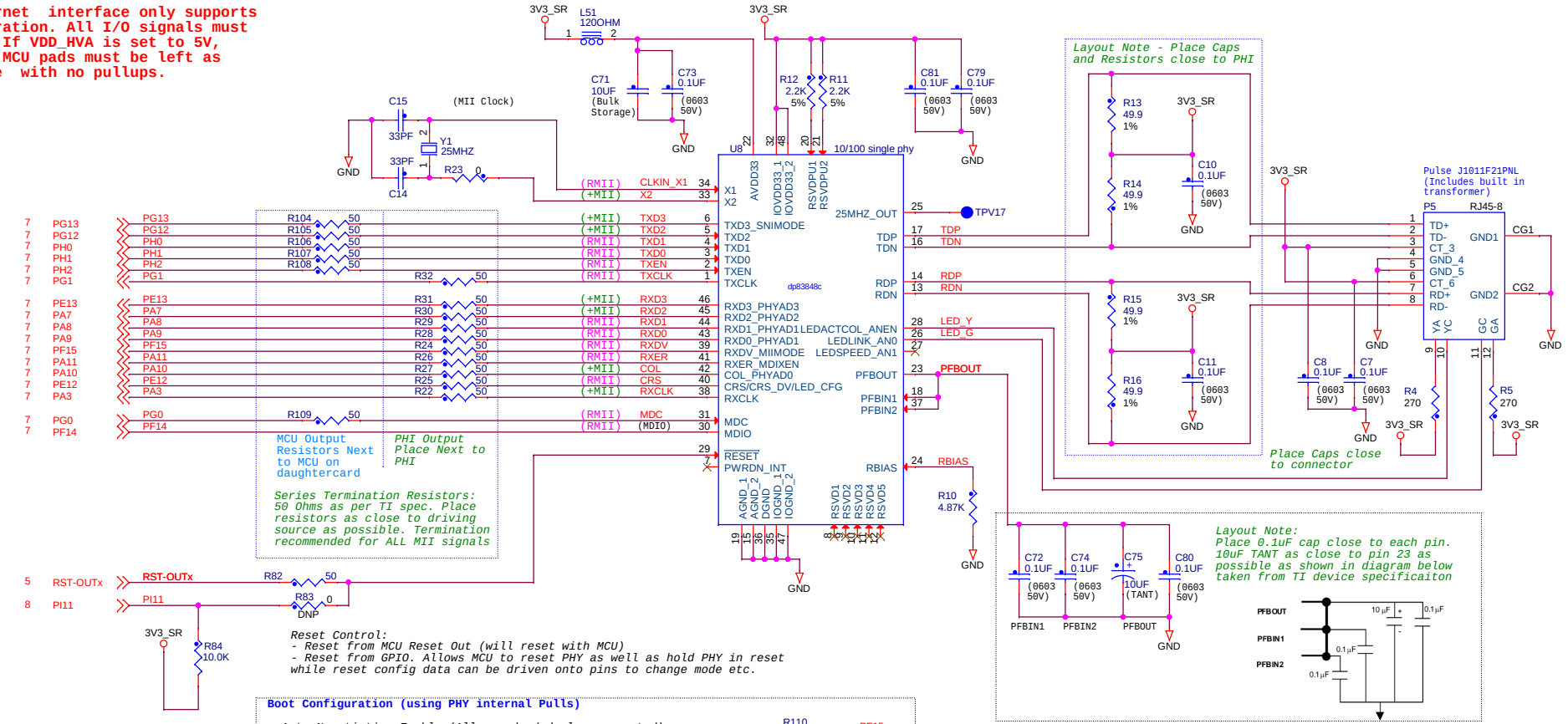
Ethernet (Configured for MII Mode)

All Ethernet Signals are in power domain VDD_HV_B

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.



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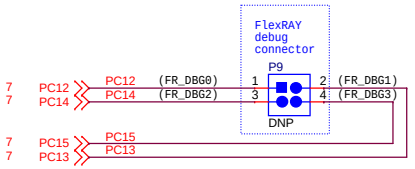
FlexRAY Physical Interface

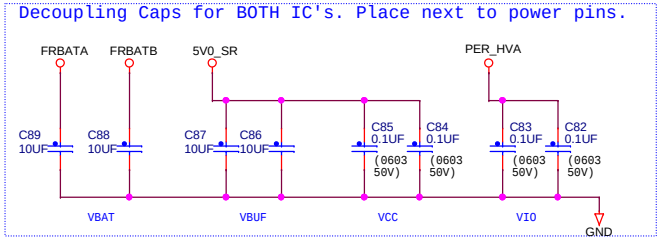
All Signals are in power domain VDD_HV_A.

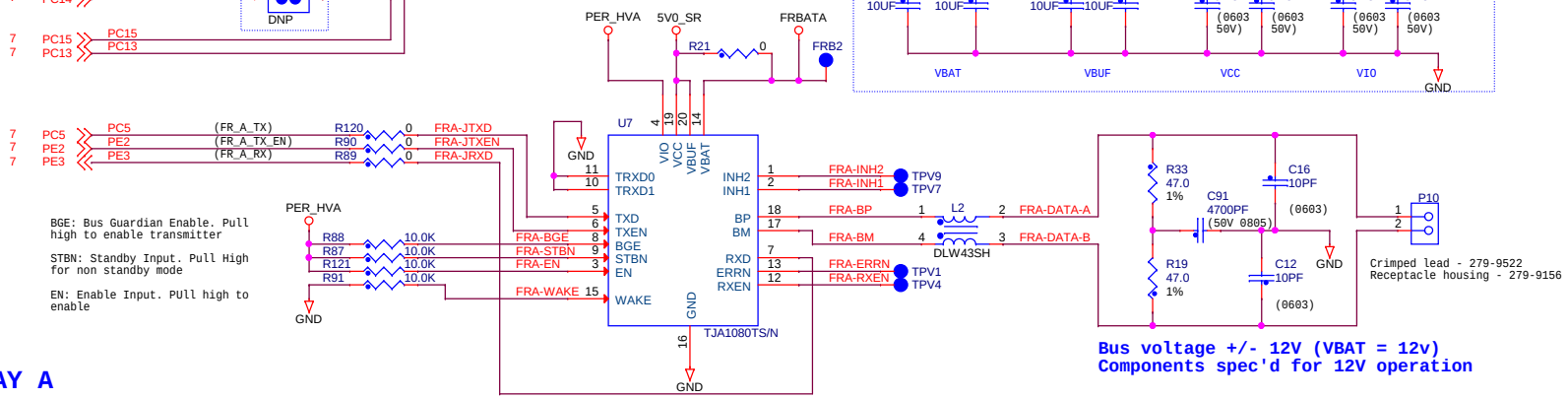
FlexRAY interface will work at 3.3V or 5.0V (PER_HVA)



Note on VBAT:
- Operational range is 6.5v to 60V
- Undervoltage detection is max 4.5v

On EVB this is supplied from 5v, In theory this should be to battery with 60uS delay between applying Vbat and I/O voltages. If necessary, 12V can be externally supplied by removing the resistor and connecting pad to 12v





BGE: Bus Guardian Enable. Pull high to enable transmitter

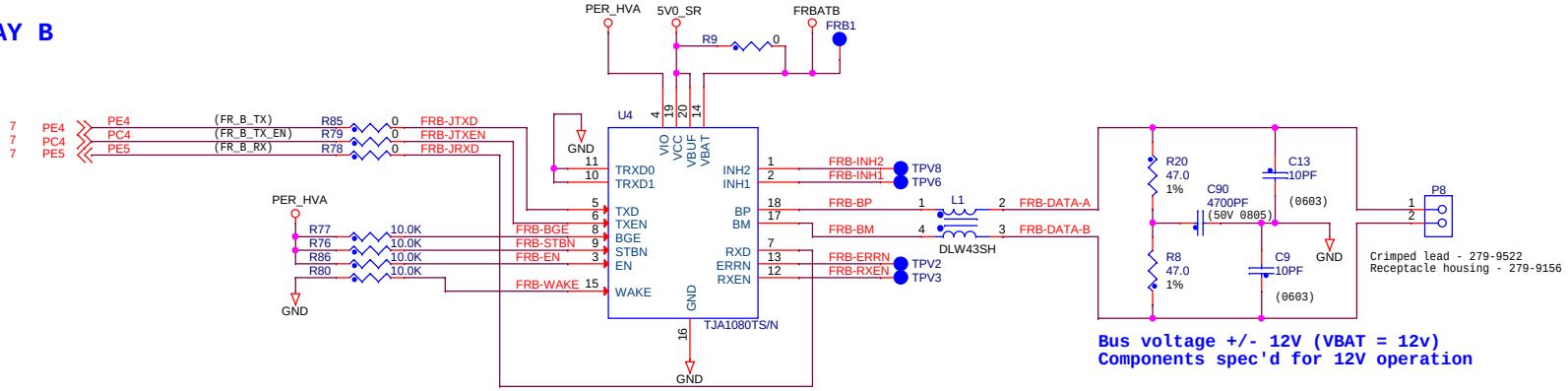
STBN: Standby Input. Pull High for non standby mode

EN: Enable Input. PUll high to enable

FlexRAY A

Bus voltage +/- 12V (VBAT = 12v)
Components spec'd for 12V operation

FlexRAY B



Bus voltage +/- 12V (VBAT = 12v)
Components spec'd for 12V operation

MODE	EN	STBN
Normal	1	1
Rec Only	0	1
Go to Sleep	1	0
Sleep	0	0

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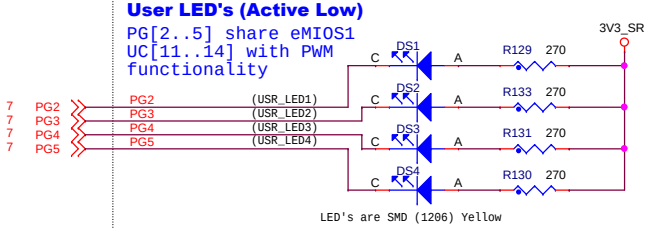
User Peripheralls (Led's, Switches and ADC Pot)

Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage)
Similarly, the LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains
The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage

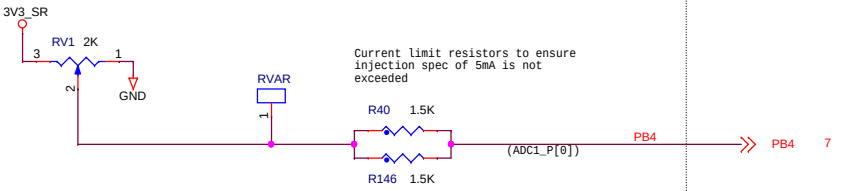
User LED's (Active Low)

PG[2..5] share eMIOS1 UC[11..14] with PWM functionality

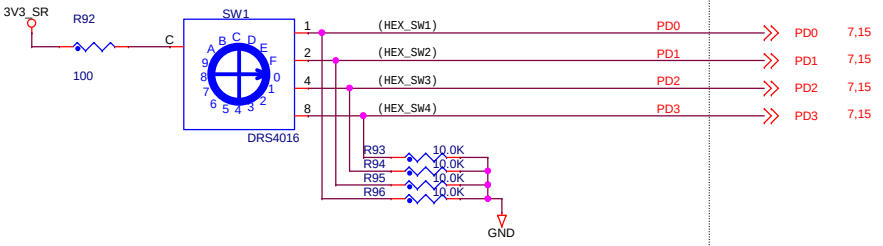


Note that LED2 and LED4 (PG3 and PG5) can be controlled in LPU_RUN mode (and also have pad keepers in LPU_STANDBY)

ADC Input Pot and Test Point

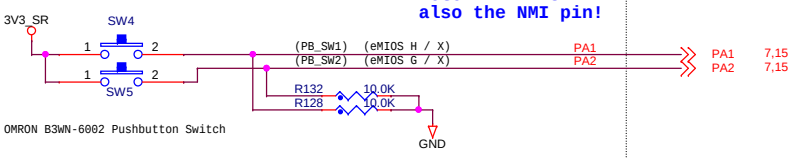


Hex Encoded Switch (Active High)



User Pushbutton Switches (Active High)

Note - PA1 is also the NMI pin!



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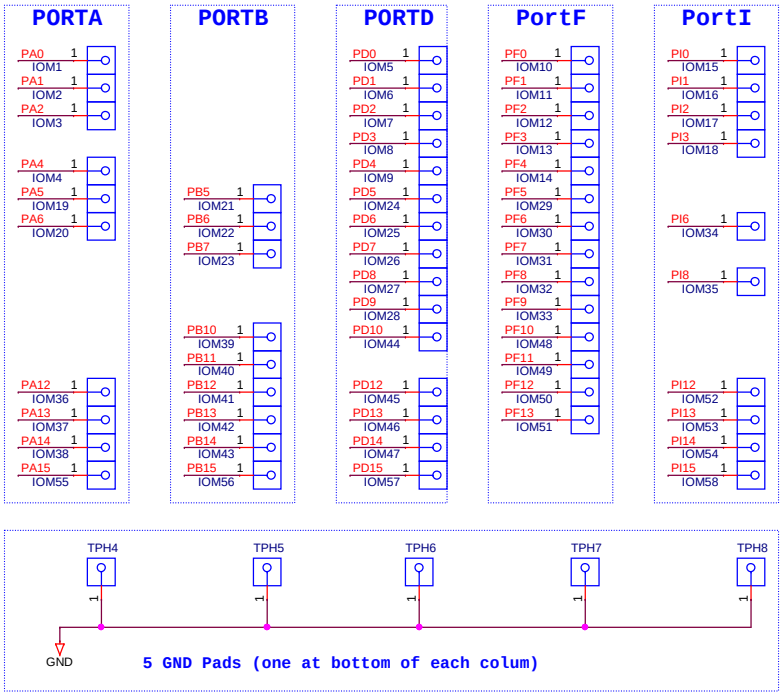
GPIO Pin Matrix

All pads are DNP (Do Not Populate) 0.1" pitch headers placed on a 0.1" grid

PA[1,2] shared with user switches

PD[0..3] shared with Hex Switch

7	PA0	PA0
7,14	PA1	PA1
7,14	PA2	PA2
7	PA4	PA4
7	PA5	PA5
7	PA6	PA6
7	PA12	PA12
7	PA13	PA13
7	PA14	PA14
7	PA15	PA15
7	PB5	PB5
7	PB6	PB6
7	PB7	PB7
7	PB10	PB10
7	PB11	PB11
7	PB12	PB12
7	PB13	PB13
7	PB14	PB14
7	PB15	PB15
7,14	PD0	PD0
7,14	PD1	PD1
7,14	PD2	PD2
7,14	PD3	PD3
7	PD4	PD4
7	PD5	PD5
7	PD6	PD6
7	PD7	PD7
7	PD8	PD8
7	PD9	PD9
7	PD10	PD10
7	PD12	PD12
7	PD13	PD13
7	PD14	PD14
7	PD15	PD15
7	PF0	PF0
7	PF1	PF1
7	PF2	PF2
7	PF3	PF3
7	PF4	PF4
7	PF5	PF5
7	PF6	PF6
7	PF7	PF7
7	PF8	PF8
7	PF9	PF9
7	PF10	PF10
7	PF11	PF11
7	PF12	PF12
7	PF13	PF13
8	PI0	PI0
8	PI1	PI1
8	PI2	PI2
8	PI3	PI3
8	PI6	PI6
8	PI8	PI8
8	PI12	PI12
8	PI13	PI13
8	PI14	PI14
8	PI15	PI15



Layout Notes:

Pads must be placed in a 5 (W) x 16(H) matrix pattern, 2.54 mm pitch
- *one column for each port*
- *16 tall (1 row for each port number from 0 to 15).*
- *GND pad at bottom of each colum*
- *After production, pads should be through hole (not solder filled)*

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