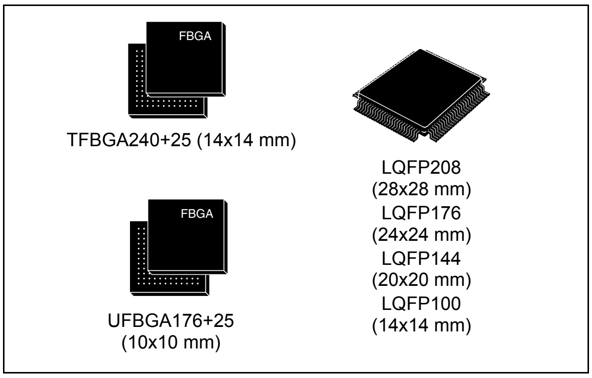
STM32H743xI

32-bit ARM Cortex-M7 400MHz MCUs, up to 2MB Flash, 1MB RAM, 46 com. and analog interfaces

Datasheet - preliminary data

Features



Core

- 32-bit ARM® Cortex®-M7 core with double-precision FPU and L1 cache: 16 Kbytes of data and 16 Kbytes of instruction cache allowing one cache line to be filled in a single access from the 256-bit embedded Flash memory; frequency up to 400 MHz, MPU, 856 DMIPS/ 2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

- Up to 2 Mbytes of Flash memory with read-while-write support
- ~1 Mbyte of RAM: 192 Kbytes of TCM RAM (inc. 64 Kbytes of ITCM RAM + 128 Kbytes of DTCM RAM for time critical routines), 864 Kbytes of user SRAM, and 4 Kbytes of SRAM in Backup domain
- Dual mode Quad-SPI memory interface
- Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND Flash
- CRC calculation unit

Security

- ROP, PC-ROP, active tamper, secure firmware upgrade support

General-purpose input/outputs

- Up to 168 I/O ports with interrupt capability
  - Fast I/Os capable of up to 133 MHz
  - Up to 164 5 V-tolerant I/Os

Reset and power management

- 3 separate power domains which can be independently clock gated or switched off to maximize power efficiency:
  - D1: high-performance capabilities for high bandwidth peripherals
  - D2: communication peripherals and timers
  - D3: reset/clock control/power management
- 1.62 to 3.6 V application supply and I/Os
- POR, PDR, PVD and BOR
- Dedicated USB power embedding a 3.3 V internal regulator to supply the internal PHYs
- Embedded regulator (LDO) with configurable scalable output to supply the digital circuitry
- Voltage scaling in Run and Stop mode
- Backup regulator (~0.9 V)
- Voltage reference for analog peripheral and V_{REF+}
- Low-power modes: Sleep, Stop and Standby

Low-power consumption

- Total current consumption down to 7 µA

Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 40 kHz LSI
- External oscillators: 4-48 MHz HSE, 32.768 kHz LSE
- 3× PLLs (1 for the system clock, 2 for kernel clocks) with fractional mode

Interconnect matrix

- 3 bus matrices (1 AXI and 2 AHB)
- Bridges (5× AHB2-APB, 2× AXI2-AHB)

4 DMA controllers to unload the CPU

- 1× high-speed general-purpose master direct memory access controller (MDMA)
- 2× dual-port DMAs with FIFO and request router capabilities
- 1× basic DMA with request router capabilities

Up to 35 communication peripherals

- 4× I2C FM+ interfaces (SMBus/PMBus)
- 4× USART/4x UARTs (ISO7816 interface, LIN, IrDA, modem control) and 1x LPUART
- 6× SPIs, including 3 with muxed duplex I2S audio class accuracy via internal audio PLL or external clock and 1 x I2S in LP domain
- 4x SAIs (serial audio interface)
- SPDIFRX interface
- SWPMI single-wire protocol master I/F
- MDIO Slave interface
- 2× SD/SDIO/MMC interfaces
- 2× CAN controllers: 2 with CAN FD, 1 with time-triggered CAN (TT-CAN)
- 2× USB OTG interfaces (1FS, 1HS/FS)
- Ethernet MAC interface with DMA controller
- HDMI-CEC
- 8- to 14-bit camera interface up to 80 MHz

11 analog peripherals

- 3× ADCs with 16-bit max. resolution (14 bits 2.7 MSPS, 16 bits 168 kSPS)
- 1× temperature sensor
- 2× 12-bit D/A converters (1 MHz)
- 2× ultra-low-power comparators
- 2× operational amplifiers (8 MHz bandwidth)
- 1× digital filters for sigma delta modulator (DFSDM) with 8 channels/4 filters

Graphics

- LCD-TFT controller up to XGA resolution
- Chrom-ART graphical hardware Accelerator™ (DMA2D) to reduce CPU load
- Hardware JPEG Codec

Up to 22 timers and watchdogs

- 1× high-resolution timer (2.5 ns max resolution)
- 2× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- 2× 16-bit advanced motor control timers
- 10× 16-bit general-purpose timers
- 5× 16-bit low-power timers
- 2× watchdogs (independent and window)
- 1× SysTick timer
- RTC with sub-second accuracy & HW calendar

Debug mode

- SWD & JTAG interfaces
- 4 Kbyte Embedded Trace Buffer

True random number generators (3 oscillators each)

96-bit unique ID

All packages are ECOPACK®2 compliant

Table 1. Device summary

Reference	Part number
STM32H743xI	STM32H743VI, STM32H743ZI, STM32H743II, STM32H743BI, STM32H743XI

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List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the Root part number 1 microcontrollers.

This document should be read in conjunction with the Root part number 2 reference manual (RM0433). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M7 core, please refer to the Cortex®-M7 Technical Reference Manual, available from the www.arm.com website.

2 Description

STM32H743xI devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 400 MHz. The Cortex® -M7 core features a floating point unit (FPU) which supports ARM® double-precision (IEEE 754 compliant) and single-precision data-processing instructions and data types. STM32H743xI devices support a full set of DSP instructions and a memory protection unit (MPU) to enhance application security.

STM32H743xI devices incorporate high-speed embedded memories with a dual-bank Flash memory up to 2 Mbytes, around 1 Mbyte of RAM (including 192 Kbytes of TCM RAM, 864 Kbytes of user SRAM and 4 Kbytes of backup SRAM), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, 2x32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memory access.

All the devices offer three ADCs, two DACs, two ultra-low power comparators, a low-power RTC, a high-resolution timer, 12 general-purpose 16-bit timers, two PWM timers for motor control, five low-power timers, a true random number generator (RNG). The devices support four digital filters for external sigma-delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Four I²Cs
  - Four USARTs, four UARTs and one LPUART
  - Six SPIs, three I²Ss in half-duplex mode. To achieve audio class accuracy, the I²S peripherals can be clocked by a dedicated internal audio PLL or by an external clock to allow synchronization.
  - Four SAI serial audio interfaces
  - One SPDIFRX interface
  - One SWPMI (Single Wire Protocol Master Interface)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces
  - A USB OTG full-speed and a USB OTG high-speed interface with full-speed capability (with the ULPI)
  - One FDCAN plus one TT-CAN interface
  - An Ethernet interface
  - Chrom-ART Accelerator™
  - HDMI-CEC
- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - A Quad-SPI Flash memory interface
  - A camera interface for CMOS sensors
  - An LCD-TFT display controller
  - A JPEG hardware compressor/decompressor

Refer to *Table 2: STM32H743xI features and peripheral counts* for the list of peripherals available on each part number.

STM32H743xI devices operate in the –40 to +85 °C temperature range from a 1.62 to 3.6 V power supply. The supply voltage can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor)* and connecting the PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Dedicated supply inputs for USB (OTG_FS and OTG_HS) are available on all packages except LQFP100 to allow a greater power supply choice.

A comprehensive set of power-saving modes allows the design of low-power applications.

STM32H743xI devices are offered in 6 packages ranging from 100 pins to 240 pins/balls. The set of included peripherals changes with the device chosen.

These features make STM32H743xI microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smart watches.

Figure 1 shows the general block diagram of the device family.

Table 2. STM32H743xI features and peripheral counts

Peripherals		STM32H 743VI	STM32H 743ZI	STM32H 743II	STM32H 743BI	STM32H 743XI
Flash memory in Kbytes		2048				
SRAM in Kbytes	SRAM mapped onto AXI bus	512				
	SRAM1 (D2 domain)	128				
	SRAM2 (D2 domain)	128				
	SRAM3 (D2 domain)	32				
	SRAM4 (D3 domain)	64				
TCM RAM in Kbytes	ITCM RAM (instruction)	64				
	DTCM RAM (data)	128				
Backup SRAM (Kbytes)		4				
FMC		Yes				
Quad-SPI		Yes				
Ethernet		Yes				

Table 2. STM32H743xI features and peripheral counts (continued)

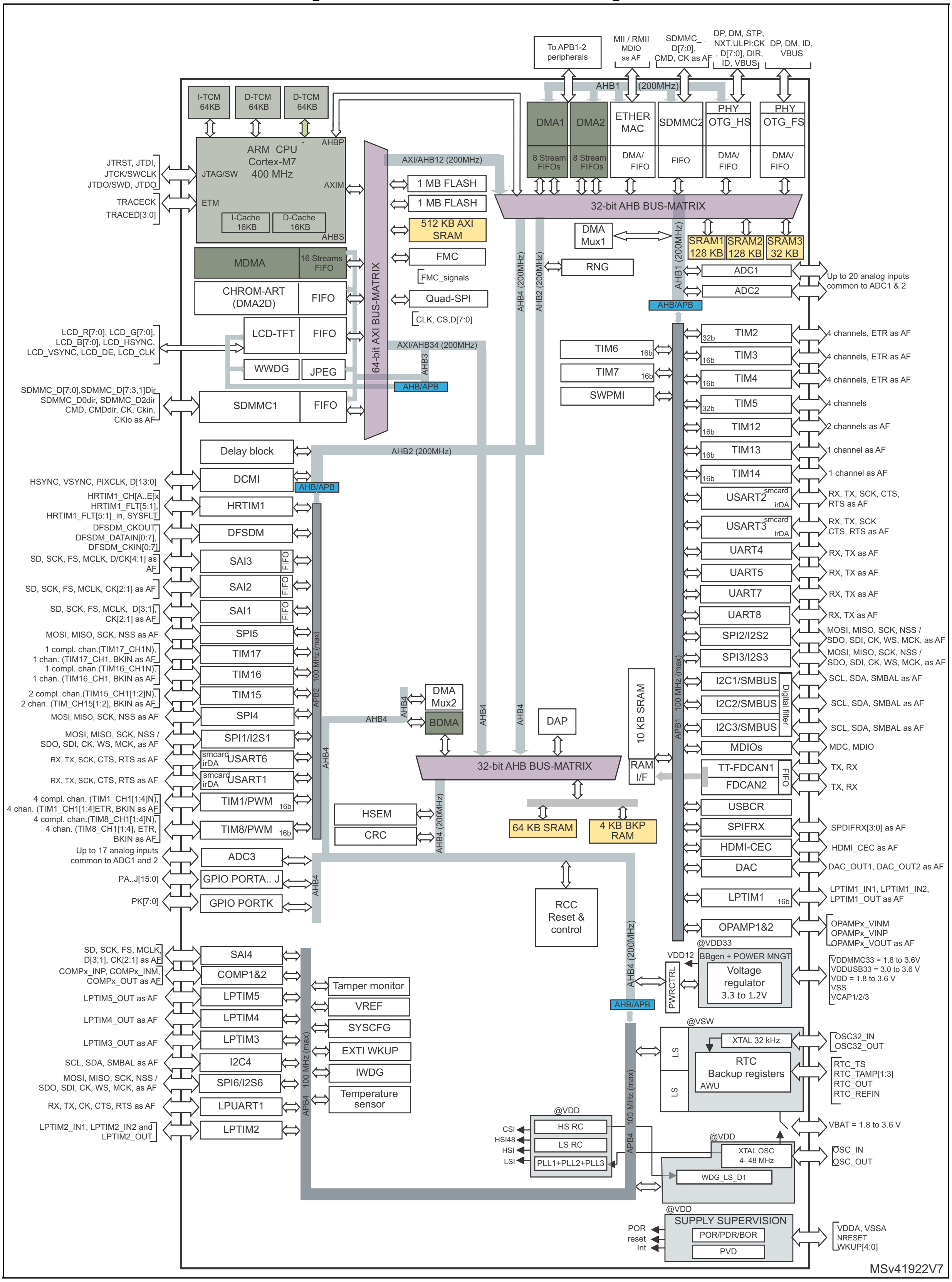
Peripherals		STM32H 743VI	STM32H 743ZI	STM32H 743II	STM32H 743BI	STM32H 743XI
Timers	High-resolution	1				
	General-purpose	10				
	Advanced-control (PWM)	2				
	Basic	2				
	Low-power	5				
Random number generator		Yes				
Communication interfaces	SPI / I^2S	6/3(1)				
	I^2C	4				
	USART/UART/ LPUART	4/4 /1				
	SAI	4				
	SPDIFRX	4 inputs				
	SWPMI	Yes				
	MDIO	Yes				
	SDMMC	2				
	FDCAN/TT-CAN	1/1				
	USB OTG_FS	Yes				
	USB OTG_HS	Yes				
Ethernet and camera interface		Yes				
LCD-TFT		Yes				
JPEG Codec		Yes				
Chrom-ART Accelerator™ (DMA2D)		Yes				
GPIOs		Up to 168				
8 to 16-bit ADCs		3				
Number of channels		20				
12-bit DAC Number of channels		Yes 2				
Comparators		2				
Operational amplifiers		2				
DFSDM		Yes				
Maximum CPU frequency		400 MHz				
Operating voltage		1.71 to 3.6 V(2)	1.62 to 3.6 V(3)			

Table 2. STM32H743xI features and peripheral counts (continued)

Peripherals	STM32H 743VI	STM32H 743ZI	STM32H 743II	STM32H 743BI	STM32H 743XI
Operating temperatures	Ambient temperatures: –40 up to +85 °C(4)				
	Junction temperature: –40 to + 125 °C				
Package	LQFP100	LQFP144	LQFP 176 UFBGA 176+25	LQFP 208	TFBGA 240+25

1. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. Since the LQFP100 package does not feature the PDR_ON pin (tied internally to V_{DD}), the minimum V_{DD} value for this package is 1.71 V.
3. V_{DD}/V_{DDA} can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor*) and connecting PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.
4. The product junction temperature must be kept within the –40 to +125 °C temperature range.

Figure 1. STM32H743xI block diagram



3 Functional overview

3.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with double-precision FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 1 shows the general block diagram of the STM32H743xI family.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

3.3 Memories

3.3.1 Embedded Flash memory

The STM32H743xI devices embed up to 2 Mbytes of Flash memory that can be used for storing programs and data.

The Flash memory is organized as 266-bit Flash words memory that can be used for storing both code and data constants. Each word consists of:

- One Flash word (8 words, 32 bytes or 256 bits)
- 10 ECC bits.

The Flash memory is divided into two independent banks. Each bank is organized as follows:

- A 1 Mbyte user Flash memory block containing eight user sectors of 128 Kbytes(4 K Flash words)
- 128 Kbytes of System Flash memory from which the device can boot
- 2 Kbytes (64 Flash words) of user option bytes for user configuration

3.3.2 Embedded SRAM

All devices feature:

- 512 Kbytes of AXI-SRAM mapped onto AXI bus on D1 domain.
- SRAM1 mapped on D2 domain: 128 Kbytes
- SRAM2 mapped on D2 domain: 128 Kbytes
- SRAM3 mapped on D2 domain: 32 Kbytes
- SRAM4 mapped on D3 domain: 64 Kbytes
- 4 Kbytes of backup SRAM

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.
- RAM mapped to TCM interface (ITCM and DTCM):

  Both ITCM and DTCM RAMs are 0 wait state memories that are accessible from the CPU or the MDMA (even in Sleep mode) through a specific AHB slave of the CPU(AHBP).
  - 64 Kbytes of ITCM-RAM (instruction RAM)

    This RAM is connected to ITCM 64-bit interface designed for execution of critical real-times routines by the CPU.
  - 128 Kbytes of DTCM-RAM (2x 64 Kbyte DTCM-RAMs on 2x32-bit DTCM ports)

    The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex®-M7 dual issue capability.

Error code correction (ECC)

SRAM data are protected by ECC:

- 7 ECC bits are added per 32-bit word.
- 8 ECC bits are added per 64-bit word for AXI-SRAM and ITCM-RAM.

The ECC mechanism is based on the SECDED algorithm. It supports single- and double-error correction.

3.4 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space
- All RAM address space: ITCM, DTCM RAMs and SRAMs
- The System memory bootloader

The boot loader is located in non-user System memory. It is used to reprogram the Flash memory through a serial interface (USART, I2C, SPI, USB-DFU). Refer to *STM32 microcontroller System memory boot mode* application note (AN2606) for details.

3.5 Power supply management

3.5.1 Power supply scheme

- V_{DD} = 1.62 to 3.6 V: external power supply for I/Os, provided externally through V_{DD} pins.
- V_{DDLDO} = 1.62 to 3.6 V: supply voltage for the internal regulator supplying V_{CORE}
- V_{DDA} = 1.62 to 3.6 V: external analog power supplies for ADC, DAC, COMP and OPAMP.
- $V_{DD33USB}$ and $V_{DD50USB}$:

  $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via the USB internal regulator. This allows supporting a V_{DD} supply different from 3.3 V.

  The USB regulator can be bypassed to supply directly $V_{DD33USB}$ if V_{DD} = 3.3 V.
- V_{BAT} = 1.2 to 3.6 V: power supply for the V_{SW} domain when V_{DD} is not present.
- V_{CAP1}/V_{CAP2}/V_{CAP3}: V_{CORE} supplies, which values depend on voltage scaling (0.7 V, 0.9 V, 1.0 V, 1.1 V or 1.2 V). They are configured through VOS bits in PWR_CR3 register. The V_{CORE} domain is split into the following power domains that can be independently switch off.
  - D1 domain containing some peripherals and the Cortex®-M7 core.
  - D2 domain containing a large part of the peripherals.
  - D3 domain containing some peripherals and the system control.

3.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in reset mode when V_{DD} is below this threshold,
- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.
- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.

3.5.3 Voltage regulator

The same voltage regulator supplies the 3 power domains (D1, D2 and D3). D1 and D2 can be independently switched off.

Voltage regulator output can be adjusted according to application needs through 5 power supply levels:

- Run mode (VOS1 to VOS3)
  - Scale 1: high performance
  - Scale 2: medium performance and consumption
  - Scale 3: optimized performance and low-power consumption
- Stop mode (SVOS3 to SVOS5)
  - Scale 3: peripheral with wakeup from stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  - Scale 4 and 5 where the peripheral with wakeup from Stop mode is disabled

    The peripheral functionality is disabled but wakeup from Stop mode is possible through GPIO or asynchronous interrupt.

3.6 Low-power strategy

There are several ways to reduce power consumption on STM32H743xI:

- Decrease dynamic power consumption by slowing down the system clocks even in Run mode and individually clock gating the peripherals that are not used.
- Save power consumption when the CPU is idle, by selecting among the available low-power mode according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wakeup sources.

The devices feature several low-power modes:

- CSleep (CPU clock stopped)
- CStop (CPU sub-system clock stopped)
- DStop (Domain bus matrix clock stopped)
- Stop (System clock stopped)
- DStandby (Domain powered down)
- Standby (System powered down)

CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex®-Mx core is set after returning from an interrupt service routine.

A domain can enter low-power mode (DStop or DStandby) when the processor, its subsystem and the peripherals allocated in the domain enter low-power mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared and the power domains are in DStop or DStandby mode.

Table 3. System vs domain low-power mode

System power mode	D1 domain power mode	D2 domain power mode	D3 domain power mode
Run	DRun/DStop/DStandby	DRun/DStop/DStandby	DRun
Stop	DStop/DStandby	DStop/DStandby	DStop
Standby	DStandby	DStandby	DStandby

3.7 Reset and clock controller (RCC)

The clock and reset controller is located in D3 domain. The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baudrate.

3.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock (1% accuracy)
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - 4-48 MHz HSE clock
  - 32.768 kHz LSE clock

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

3.7.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Window watchdog
- Independent watchdog
- Software reset
- Low-power mode security reset
- Exit from Standby

3.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

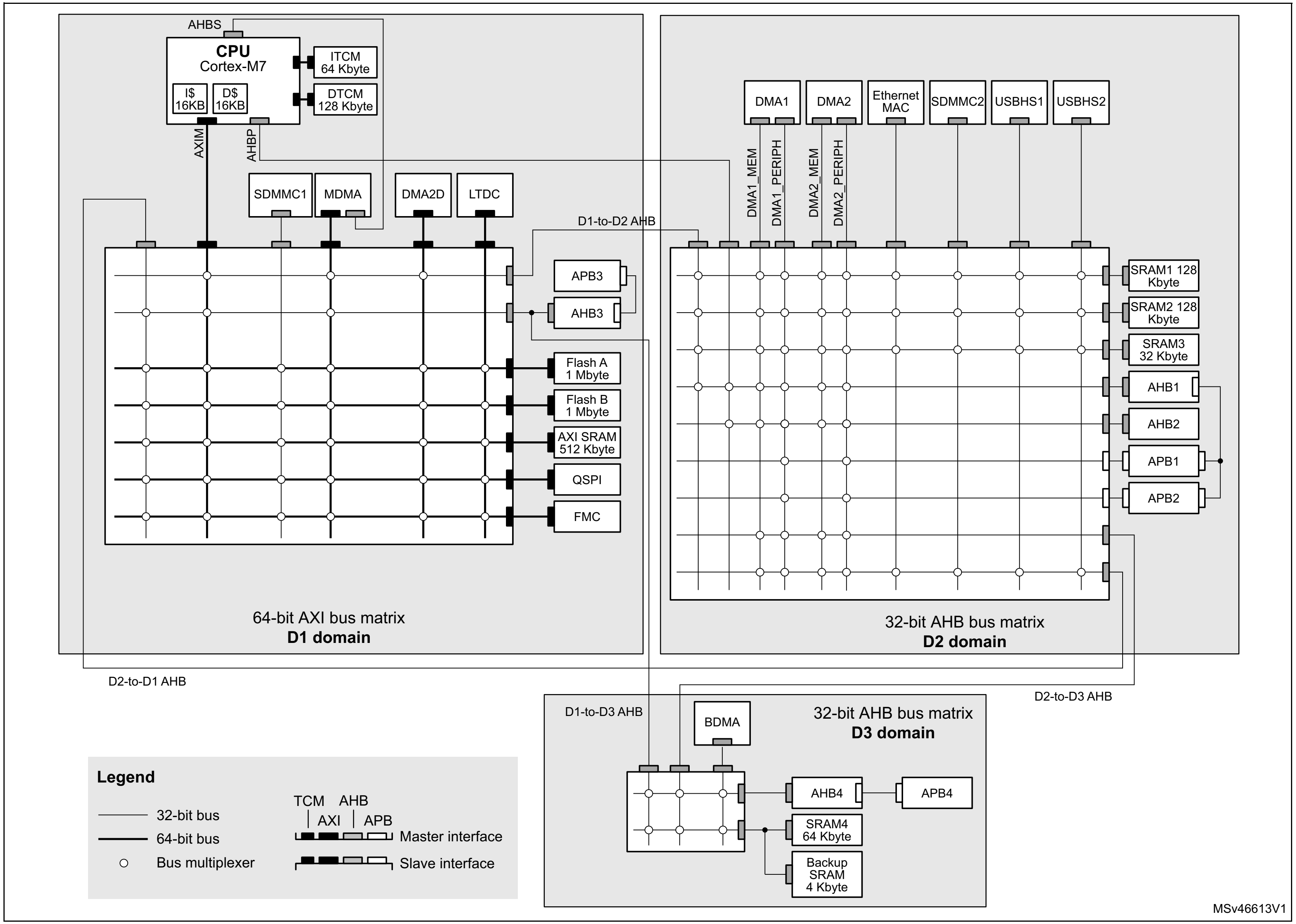
After reset, all GPIOs are in Analog mode to reduce power consumption.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, two AHB bus matrices and bus bridges that allow interconnecting bus masters with bus slaves (see *Figure 2*).

Figure 2. STM32H743xI bus matrix



3.10 DMA controllers

The devices feature four DMA instances to unload CPU activity:

- A master direct memory access (MDMA)

  The MDMA is a high-speed DMA controller, which is in charge of all types of memory transfers (peripheral to memory, memory to memory, memory to peripheral), without any CPU action. It features a master AXI interface and a dedicated AHB interface to access Cortex®-M7 TCM memories.

  The MDMA is located in D1 domain. It is able to interface with the other DMA controllers located in D2 domain to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

  Each of the 16 channels can perform single block transfers, repeated block transfers and linked list transfers.
- Two dual-port DMAs (DMA1, DMA2) located in D2 domain, with FIFO and request router capabilities.
- One basic DMA (BDMA) located in D3 domain, with request router capabilities.

The DMA request router could be considered as an extension of the DMA controller. It routes the DMA peripheral requests to the DMA controller itself. This allowing managing the DMA requests with a high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output trigger or DMA event.

3.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphical accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables. The DMA2D also supports block based YCbCr to handle JPEG decoder output.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and handle up to 150 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.13 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processor, power domains and/or D3 domain from Stop mode.

The EXTI handles up to 89 independent event/interrupt lines split as 28 configurable events and 61 direct events .

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

3.14 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.15 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by 2.

3.16 Quad-SPI memory interface (QUADSPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad-SPI Flash memories. It supports both single and double datarate operations.

It can operate in any of the following modes:

- Direct mode through registers
- External Flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes of external Flash memory can be mapped, and 8-, 16- and 32-bit data accesses are supported as well as code execution.

The opcode and the frame format are fully programmable.

3.17 Analog-to-digital converters (ADCs)

The STM32H743xI devices embed three analog-to-digital converters, which resolution can be configured to 16, 14, 12, 10 or 8 bits. Each ADC shares up to 20 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, thus allowing to automatically transfer ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, HRTIM1 and LPTIM1 timer.

3.18 Temperature sensor

STM32H743xI devices embeds a temperature sensor that generates a voltage (V_{TS}) that varies linearly with the temperature. This temperature sensor is internally connected to ADC3_IN18. The conversion range is between 1.7 V and 3.6 V. It can measure the device ambient temperature ranging from − 40 to +125 °C with a precision of +-2%.

The temperature sensor have a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the System memory area, which is accessible in read-only mode.

3.19 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers and the backup SRAM.

To optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by V_{DD}, in which case, the V_{DD} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to VDD.

3.20 Digital-to-analog converters (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- external triggers for conversion
- input voltage reference V_{REF+} or internal VREFBUF reference.

The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.21 Ultra-low-power comparators (COMP)

STM32H743xI devices embed two rail-to-rail comparators (COMP1 and COMP2). They feature programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) as well as selectable output polarity.

The reference voltage can be one of the following:

- An external I/O
- A DAC output channel
- An internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers, and be combined into a window comparator.

3.22 Operational amplifiers (OPAMP)

STM32H743xI devices embed two rail-to-rail operational amplifiers (OPAMP1 and OPAMP2) with external or internal follower routing and PGA capability.

The operational amplifier main features are:

- PGA with a non-inverting gain ranging of 2, 4, 8 or 16 or inverting gain ranging of -1, -3, -7 or -15
- One positive input connected to DAC
- Output connected to internal ADC
- Low input bias current down to 1 nA
- Low input offset voltage down to 1.5 mV
- Gain bandwidth up to 8 MHz

The devices embeds two operational amplifiers (OPAMP1 and OPAMP2) with two inputs and one output each. These three I/Os can be connected to the external pins, thus enabling any type of external interconnections. The operational amplifiers can be configured internally as a follower, as an amplifier with a non-inverting gain ranging from 2 to 16 or with inverting gain ranging from -1 to -15.

3.23 Digital filter for sigma-delta modulators (DFSDM)

The devices embed one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from internal ADC peripherals or microcontroller memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0..20 MHz
- alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: ADC data or memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion

- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0’s or 1’s on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “regular” or “injected” conversions:
  - “regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
  - “injected” conversions for precise timing and with high conversion priority

3.24 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can achieve a data transfer rate up to 140 Mbyte/s using a 80 MHz pixel clock. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.25 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

3.26 JPEG Codec (JPEG)

The JPEG Codec can encode and decode a JPEG stream as defined in the ***ISO/IEC 10918-1*** specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Support for single greyscale component
- Ability to enable/disable header processing
- Fully synchronous design
- Configuration for high-speed decode mode

3.27 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.28 Timers and watchdogs

The devices include one high-resolution timer, two advanced-control timers, ten general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
High-resolution timer	HRTIM1	16-bit	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	10	Yes	400	400
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	100	200
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	100	200
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	100	200
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	100	200
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	100	200
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	100	200
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	100	200

Table 4. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	100	200
Low-power timer	LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	100	200

1. The maximum timer clock is up to 400 MHz depending on TIMPRE bit in the RCC_CFGR register and D2PRE1/2 bits in RCC_D2CFGR register.

3.28.1 High-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

The HRTIM1 timer is made of a digital kernel clocked at 400 MHz The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull and resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

3.28.2 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.28.3 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32H743xI devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The devices include 4 full-featured general-purpose timers: TIM2, TIM3, TIM4 and TIM5. TIM2 and TIM5 are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4 and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

3.28.4 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.28.5 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

The low-power timers have an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.28.6 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.28.7 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.28.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.29 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, Wakeup Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.30 Inter-integrated circuit interface (I2C)

STM32H743xI devices embed four I^2C interfaces.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.31 Universal synchronous/asynchronous receiver transmitter (USART)

STM32H743xI devices have four embedded universal synchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8). Refer to *Table 5* for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2, USART3 and USART6 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

The USARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode.The wakeup from Stop mode are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

All USART interfaces can be served by the DMA controller.

Table 5. USART features

USART modes/features(1)	USART1/2/3/6	UART4/5/7/8
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (Master/Slave)	X	-
Smartcard mode	X	-
Single-wire Half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wakeup from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	16	

1. X = supported.

3.32 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wakeup from Stop mode are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.33 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

The devices feature up to six SPIs (SPI2S1, SPI2S2, SPI2S3, SPI4, SPI5 and SPI6) that allow communicating up to 50 Mbits/s in master and slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. All SPI interfaces support NSS pulse mode, TI mode, Hardware CRC calculation and 8x 8-bit embedded Rx and Tx FIFOs with DMA capability.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I^2S interfaces support 16x 8-bit embedded Rx and Tx FIFOs with DMA capability.

3.34 Serial audio interfaces (SAI)

The devices embed 4 SAIs (SAI1, SAI2, SAI3 and SAI4) that allow designing many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC’97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.
Audio sampling frequencies up to 192 kHz are supported.
In addition, up to 8 microphones can be supported thanks to an embedded PDM interface.
The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.35 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

3.36 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.37 Management Data Input/Output (MDIO) slaves

The devices embed an MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO Register write
  - MDIO Register read
  - MDIO protocol error
- Able to operate in and wake up from STOP mode

3.38 SD/SDIO/MMC card host interfaces (SDMMC)

Two SDMMCD host interfaces are available. They support *MultiMediaCard System Specification Version 4.51* in three different databus modes: 1 bit (default), 4 bits and 8 bits.

Both interfaces support the *SD memory card specifications version 4.1.* and the *SDIO card specification version 4.0.* in two different databus modes: 1 bit (default) and 4 bits.

Each SDMMC host interface supports only one SD/SDIO/MMC card at any one time and a stack of MMC Version 4.51 or previous.

The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.

3.39 Controller area network (FDCAN1, FDCAN2)

The controller area network (CAN) subsystem consists of two CAN modules, a shared message RAM memory and a clock calibration unit.

Both CAN modules (FDCAN1 and FDCAN2) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TTCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10 Kbytes message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TTCAN). This message RAM is shared between the two FDCAN1 and FDCAN2 modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for both FDCAN1 and FDCAN2 from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

3.40 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed two USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG-HS1 supports both full-speed and high-speed operations, while OTG-HS2 supports only full-speed operations. They both integrate the transceivers for full-speed operation (12 Mbit/s). OTG-HS1 features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG-HS1 in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripherals are compliant with the USB 2.0 specification and with the OTG 2.0 specification. They have software-configurable endpoint setting and supports suspend/resume. The USB OTG controllers require a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode (OTG_HS1 only)

  The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.41 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.42 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

3.43 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- ARM® CoreSight™ debug and trace components

The debug can be controlled via a JTAG/Serial-wire debug access port, using industry standard debugging tools.

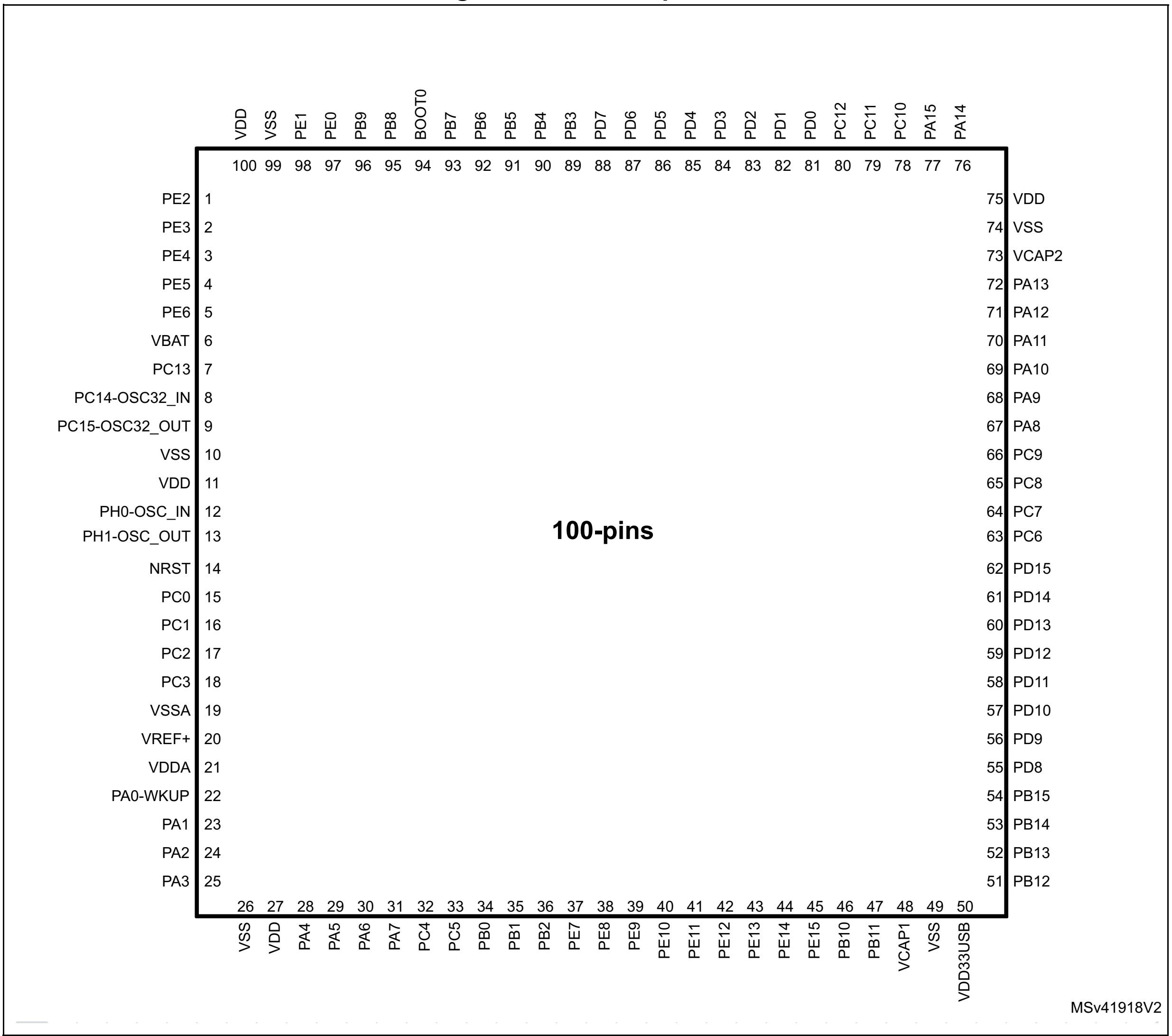
The trace port performs data capture for logging and analysis.

4 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

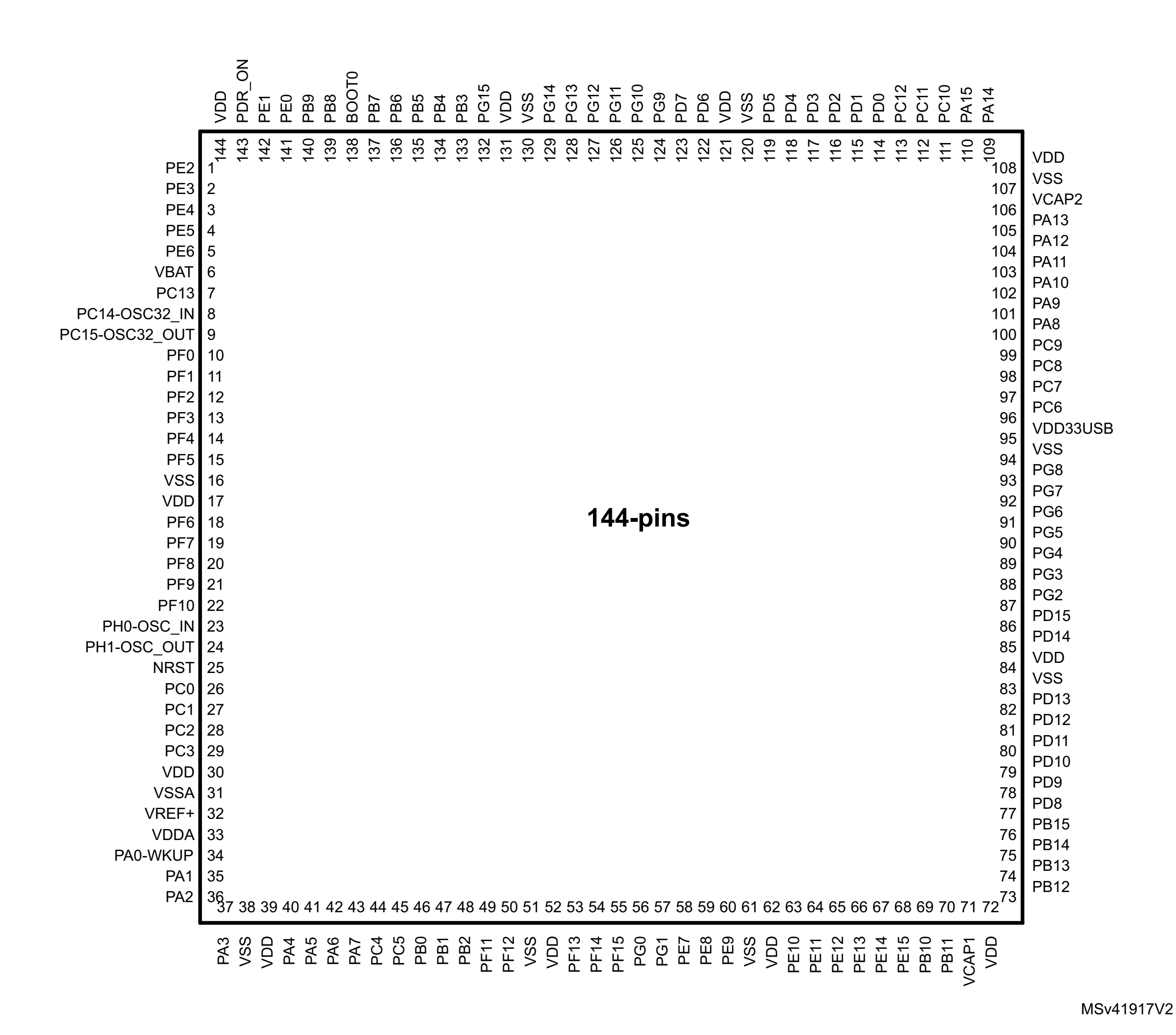
5 Pin descriptions

Figure 3. LQFP100 pinout



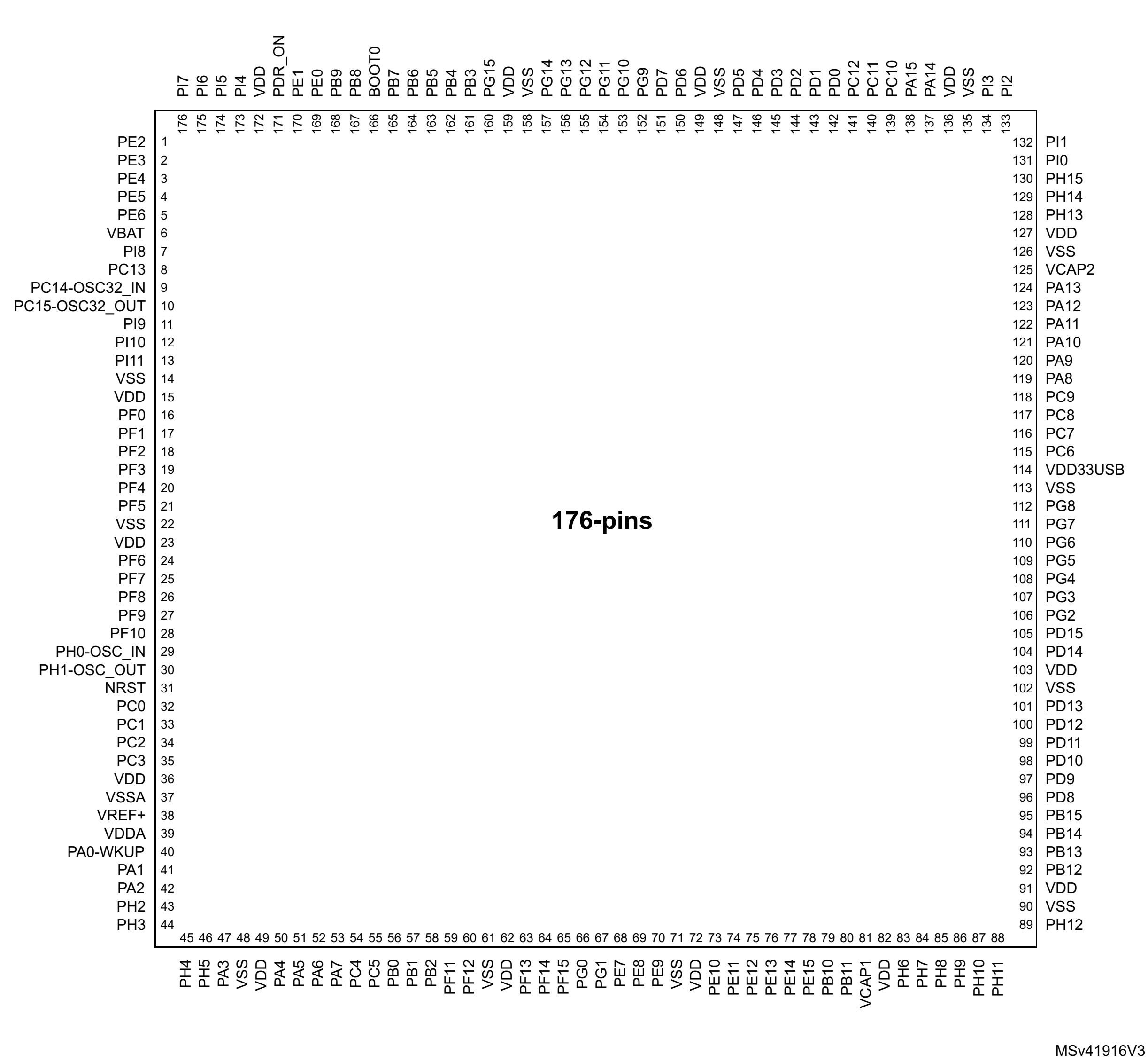
1. The above figure shows the package top view.

Figure 4. LQFP144 pinout



1. The above figure shows the package top view.

Figure 5. LQFP176 pinout



1. The above figure shows the package top view.

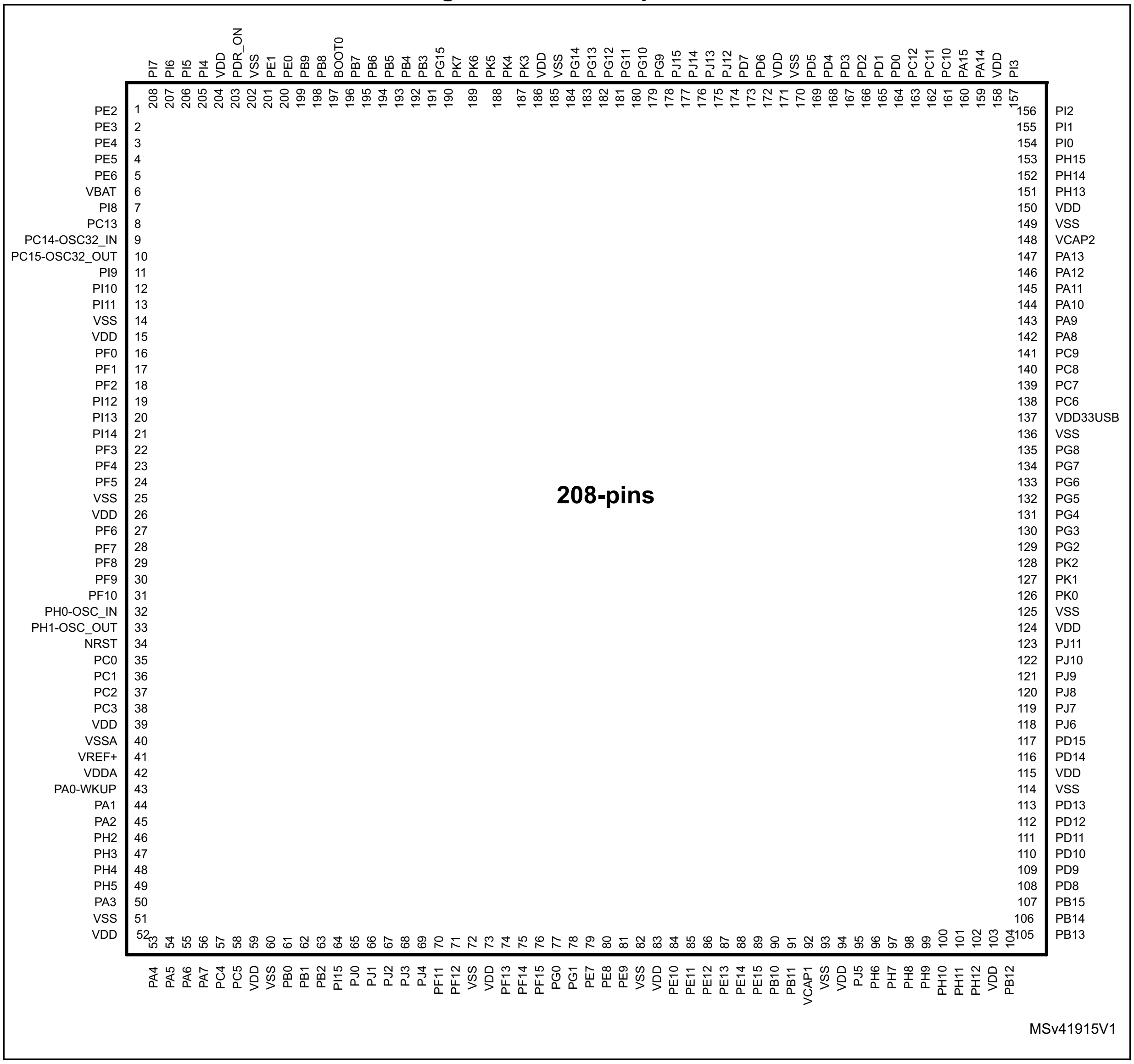
Figure 6. UFBGA176+25 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	PDR_ON	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13	PI8	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14-OSC32_IN	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15-OSC32_OUT	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP2	PC9	PA8
G	PH0-OSC_IN	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1-OSC_OUT	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD 33USB	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	VSS								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2_C	PC3_C	PB2	PG1	VSS	VSS	VCAP1	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

MSv41912V3

1. The above figure shows the package top view.

Figure 7. LQFP208 pinout



1. The above figure shows the package top view.

Figure 8. TFBGA240+25 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	PI6	PI5	PI4	PB5	VDD LDO3	VCAP3	PK5	PG10	PG9	PD5	PD4	PC10	PA15	PI1	PI0	VSS
B	VBAT	VSS	PI7	PE1	PB6	VSS	PB4	PK4	PG11	PJ15	PD6	PD3	PC11	PA14	PI2	PH15	PH14
C	PC15-OSC32_OUT	PC14-OSC32_IN	PE2	PE0	PB7	PB3	PK6	PK3	PG12	VSS	PD7	PC12	VSS	PI3	PA13	VSS	VDD LDO2
D	PE5	PE4	PE3	PB9	PB8	PG15	PK7	PG14	PG13	PJ14	PJ12	PD2	PD0	PA10	PA9	PH13	VCAP2
E	NC	PI9	PC13	PI8	PE6	VDD	PDR_ON	BOOT0	VDD	PJ13	VDD	PD1	PC8	PC9	PA8	PA12	PA11
F	NC	NC	PI10	PI11	VDD								PC7	PC6	PG8	PG7	VDD33 USB
G	PF2	NC	PF1	PF0	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG5	PG6	VSS	VDD50 USB
H	PI12	PI13	PI14	PF3	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG4	PG3	PG2	PK2
J	PH0-OSC_OUT	PH0-OSC_IN	VSS	PF5	PF4		VSS	VSS	VSS	VSS	VSS		VDD	PK0	PK1	VSS	VSS
K	NRST	PF6	PF7	PF8	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ11	VSS	NC	NC
L	VDDA	PC0	PF10	PF9	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ10	VSS	NC	NC
M	VREF+	PC1	PC2	PC3	VDD								VDD	PJ9	VSS	NC	NC
N	VREF-	PH2	PA2	PA1	PA0	PJ0	VDD	VDD	PE10	VDD	VDD	VDD	PJ8	PJ7	PJ6	VSS	NC
P	VSSA	PH3	PH4	PH5	PI15	PJ1	PF13	PF14	PE9	PE11	PB10	PB11	PH10	PH11	PD15	PD14	VDD
R	PC2_C	PC3_C	PA6	VSS	PA7	PB2	PF12	VSS	PF15	PE12	PE15	PJ5	PH9	PH12	PD11	PD12	PD13
T	PA0_C	PA1_C	PA5	PC4	PB1	PJ2	PF11	PG0	PE8	PE13	PH6	VSS	PH8	PB12	PB15	PD10	PD9
U	VSS	PA3	PA4	PC5	PB0	PJ3	PJ4	PG1	PE7	PE14	VCAP1	VDD LDO1	PH7	PB13	PB14	PD8	VSS

MSv41911V1

1. The above figure shows the package top view.

Table 6. Legend/abbreviations used in the pinout table

<table>
<tr><th colspan="2">Name</th><th>Abbreviation</th><th>Definition</th></tr>
<tr><td colspan="2">Pin name</td><td colspan="2">Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name</td></tr>
<tr><td colspan="2" rowspan="4">Pin type</td><td>S</td><td>Supply pin</td></tr>
<tr><td>I</td><td>Input only pin</td></tr>
<tr><td>I/O</td><td>Input / output pin</td></tr>
<tr><td>ANA</td><td>Analog-only Input</td></tr>
<tr><td colspan="2" rowspan="9">I/O structure</td><td>FT</td><td>5 V tolerant I/O</td></tr>
<tr><td>TT</td><td>3.3 V tolerant I/O</td></tr>
<tr><td>B</td><td>Dedicated BOOT0 pin</td></tr>
<tr><td>RST</td><td>Bidirectional reset pin with embedded weak pull-up resistor</td></tr>
<tr><td colspan="2">Option for TT and FT I/Os</td></tr>
<tr><td>_f</td><td>I2C FM+ option</td></tr>
<tr><td>_a</td><td>analog option (supplied by V_{DDA})</td></tr>
<tr><td>_u</td><td>USB option (supplied by $V_{DD33USB}$)</td></tr>
<tr><td>_h</td><td>High Speed Low Voltage</td></tr>
<tr><td colspan="2">Notes</td><td colspan="2">Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.</td></tr>
<tr><td rowspan="2">Pin functions</td><td>Alternate functions</td><td colspan="2">Functions selected through GPIOx_AFR registers</td></tr>
<tr><td>Additional functions</td><td colspan="2">Functions directly selected/enabled through peripheral registers</td></tr>
</table>

Table 7. STM32H743xI pin/ball definition

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
1	1	A2	1	1	C3	PE2	I/O	FT_h	-	TRACECLK, SAI1_CK1, SPI4_SCK, SAI1_MCLK_A, SAI4_MCLK_A, QUADSPI_BK1_IO2, SAI4_CK1, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	A1	2	2	D3	PE3	I/O	FT_h	-	TRACED0, TIM15_BKIN, SAI1_SD_B, SAI4_SD_B, FMC_A19, EVENTOUT	-
3	3	B1	3	3	D2	PE4	I/O	FT_h	-	TRACED1, SAI1_D2, DFSDM_DATIN3, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, SAI4_FS_A, SAI4_D2, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-
4	4	B2	4	4	D1	PE5	I/O	FT_h	-	TRACED2, SAI1_CK2, DFSDM_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, SAI4_SCK_A, SAI4_CK2, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	5	B3	5	5	E5	PE6	I/O	FT_h	-	TRACED3, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SAI4_SD_A, SAI4_D1, SAI2_MCK_B, TIM1_BKIN2_COMP12, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	H10	-	-	A1	VSS	S	-	-	-	-
-	-	-	-	-	F1	VDD	S	-	-	-	-
6	6	C1	6	6	B1	VBAT	S	-	-	-	-
-	-	J6	-	-	B2	VSS	S	-	-	-	-
-	-	D2	7	7	E4	PI8	I/O	FT	-	EVENTOUT	RTC_TAMP_2/RTC_TS/WKUP3

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
7	7	D1	8	8	E3	PC13	I/O	FT	-	EVENTOUT	RTC_TAMP_1/RTC_TS/ WKUP2
-	-	J7	-	-	B6	VSS	S	-	-	-	-
8	8	E1	9	9	C2	PC14-OSC32_IN (PC14)	I/O	FT	-	EVENTOUT	OSC32_IN
9	9	F1	10	10	C1	PC15-OSC32_OUT (PC15)	I/O	FT	-	EVENTOUT	OSC32_OUT
-	-	D3	11	11	E2	PI9	I/O	FT_h	-	UART4_RX, CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	12	12	F3	PI10	I/O	FT_h	-	CAN1_RXFD, ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	E4	13	13	F4	PI11	I/O	FT	-	LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT	WKUP4
-	-	F2	14	14	A17	VSS	S	-	-	-	-
-	-	F3	15	15	E6	VDD	S	-	-	-	-
-	-	-	-	-	F2	NC	-	-	-	-	-
-	-	-	-	-	E1	NC	-	-	-	-	-
-	-	-	-	-	F1	NC	-	-	-	-	-
-	-	-	-	-	G2	NC	-	-	-	-	-
-	10	E2	16	16	G4	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	11	H3	17	17	G3	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	12	H2	18	18	G1	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	19	H1	PI12	I/O	FT	-	ETH_TX_ER, LCD_HSYNC, EVENTOUT	-
-	-	-	-	20	H2	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	21	H3	PI14	I/O	FT_h	-	LCD_CLK, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	13	J2	19	22	H4	PF3	I/O	FT_ha	-	FMC_A3, EVENTOUT	ADC3_INP5
-	14	J3	20	23	J5	PF4	I/O	FT_ha	-	FMC_A4, EVENTOUT	ADC3_INN5, ADC3_INP9
-	15	K3	21	24	J4	PF5	I/O	FT_ha	-	FMC_A5, EVENTOUT	ADC3_INP4
10	16	G2	22	25	C10	VSS	S	-	-	-	-
11	17	G3	23	26	E9	VDD	S	-	-	-	-
-	18	K2	24	27	K2	PF6	I/O	FT_ha	-	TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, SAI4_SD_B, QUADSPI_BK1_IO3, EVENTOUT	ADC3_INN4, ADC3_INP8
-	19	K1	25	28	K3	PF7	I/O	FT_ha	-	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, SAI4_MCLK_B, QUADSPI_BK1_IO2, EVENTOUT	ADC3_INP3
-	20	L3	26	29	K4	PF8	I/O	FT_ha	-	TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS, SAI4_SCK_B, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_INN3, ADC3_INP7
-	21	L2	27	30	L4	PF9	I/O	FT_ha	-	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, SAI4_FS_B, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_INP2
-	22	L1	28	31	L3	PF10	I/O	FT_ha	-	TIM16_BKIN, SAI1_D3, QUADSPI_CLK, SAI4_D3, DCMI_D11, LCD_DE, EVENTOUT	ADC3_INN2, ADC3_INP6
12	23	G1	29	32	J2	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
13	24	H1	30	33	J1	PH1-OSC_OUT (PH1)	I/O	FT		EVENTOUT	OSC_OUT

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
14	25	J1	31	34	K1	NRST	I/O	RST	-	-	-
15	26	M2	32	35	L2	PC0	I/O	FT_a	-	DFSDM_CKIN0, DFSDM_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC123_ INP10
16	27	M3	33	36	M2	PC1	I/O	FT_ha	-	TRACED0, SAI1_D1, DFSDM_DATIN0, DFSDM_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SAI4_SD_A, SDMMC2_CK, SAI4_D1, ETH_MDC, MDIOS_MDC, EVENTOUT	ADC123_ INN10, ADC123_ INP11, RTC_TAMP_ 3/WKUP5
-	-	-	-	-	M3 (1)	PC2	I/O	FT_a	-	DFSDM_CKIN1, SPI2_MISO/I2S2_SDI, DFSDM_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_ INN11, ADC123_ INP12
17 (2)	28(2)	M4 (2)	34(2)	37(2)	R1 (1)	PC2_C	ANA	TT_a	-	-	ADC3_INN2, ADC3_INP0
-	-	-	-	-	M4 (1)	PC3	I/O	FT_a	-	DFSDM_DATIN1, SPI2_MOSI/I2S2_SDO, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC12_ INN12, ADC12_ INP13
18 (2)	29(2)	M5 (2)	35(2)	38(2)	R2 (1)	PC3_C	ANA	TT_a	-		ADC3_INP1
-	30	G3	36	39	E11	VDD	S	-	-	-	-
-	-	J10	-	-	C13	VSS	S	-	-	-	-
19	31	M1	37	40	P1	VSSA	S	-	-	-	-
-	-	N1	-	-	N1	VREF-	S	-	-	-	-
20	32	P1	38	41	M1	VREF+	S	-	-	-	-
21	33	R1	39	42	L1	VDDA	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
22	34	N3	40	43	N5 (1)	PA0-WKUP(PA0)	I/O	FT_a	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, USART2_CTS_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_INP16, WKUP0
-	-	-	-	-	T1(1)	PA0_C	ANA	TT_a	-	-	ADC12_INN1, ADC12_INP0
23	35	N2	41	44	N4 (1)	PA1	I/O	FT_ha	-	TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_INN16, ADC1_INP17
-	-	-	-	-	T2(1)	PA1_C	ANA	TT_a	-	-	ADC12_INP1
24	36	P2	42	45	N3	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC12_INP14, WKUP1
-	-	F4	43	46	N2	PH2	I/O	FT_ha	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	ADC3_INP13
-	-	-	-	-	F5	VDD	S	-	-	-	-
-	-	J8	-	-	C16	VSS	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	G4	44	47	P2	PH3	I/O	FT_ha	-	QUADSPI_BK2_IO1, SAI2_MCK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	ADC3_ INN13, ADC3_ INP14
-	-	H4	45	48	P3	PH4	I/O	FT_fa	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	ADC3_ INN14, ADC3_ INP15
-	-	J4	46	49	P4	PH5	I/O	FT_fa	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	ADC3_INN1 5, ADC3_INP1 6
25	37	R2	47	50	U2	PA3	I/O	FT_ha	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC12_ INP15
26	38	K6	-	51	F2	VSS	S	-	-	-	-
-	-	L4	48	-	-	VSS	S	-	-	-	-
27	39	K4	49	52	G5	VDD	S	-	-	-	-
28	40	N4	50	53	U3	PA4	I/O	TT_a	-	TIM5_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_ INP18, DAC_OUT1
29	41	P4	51	54	T3	PA5	I/O	TT_ha	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_ INN18, ADC12_ INP19, DAC_OUT2

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
30	42	P3	52	55	R3	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, SPI6_MISO, TIM13_CH1, TIM8_BKIN_COMP12, MDIOS_MDC, TIM1_BKIN_COMP12, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_ INP3
31	43	R3	53	56	R5	PA7	I/O	FT_a	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SDO, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_ INN3, ADC12_ INP7, OPAMP1_ VINM
32	44	N5	54	57	T4	PC4	I/O	FT_a	-	DFSDM_CKIN2, I2S1_MCK, SPDIFRX_IN2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC12_ INP4, OPAMP1_ VOUT, COMP_1_ INM
33	45	P5	55	58	U4	PC5	I/O	FT_a	-	SAI1_D3, DFSDM_DATIN2, SPDIFRX_IN3, SAI4_D3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, COMP_1_OUT, EVENTOUT	ADC12_ INN4, ADC12_ INP8, OPAMP1_ VINM
-	-	-	-	59	G13	VDD	S	-	-	-	-
-	-	J9	-	60	G16	VSS	S	-	-	-	-
34	46	R5	56	61	U5	PB0	I/O	FT_a	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC12_ INN5, ADC12_ INP9, OPAMP1_ VINP, COMP_1_ INP

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
35	47	R4	57	62	T5	PB1	I/O	FT_u	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC12_ INP5, COMP_1_ INM
36	48	M6	58	63	R6	PB2	I/O	FT_ha	-	SAI1_D1, DFSDM_CKIN1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, SAI4_SD_A, QUADSPI_CLK, SAI4_D1, ETH_TX_ER, EVENTOUT	COMP_1_IN P, RTC_OUT
-	-	-	-	64	P5	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	
-	-	-	-	65	N6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	
-	-	-	-	66	P6	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	
-	-	-	-	67	T6	PJ2	I/O	FT	-	LCD_R3, EVENTOUT	-
-	-	-	-	68	U6	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	69	U7	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	R6	59	70	T7	PF11	I/O	FT_a	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	ADC1_INP2
-	50	P6	60	71	R7	PF12	I/O	FT_ha	-	FMC_A6, EVENTOUT	ADC1_INN2, ADC1_INP6
-	51	M8	61	72	J3	VSS	S	-	-	-	-
-	52	N8	62	73	H5	VDD	S	-	-	-	-
-	53	N6	63	74	P7	PF13	I/O	FT_ha	-	DFSDM_DATIN6, I2C4_SMBA, FMC_A7, EVENTOUT	ADC2_INP2
-	54	R7	64	75	P8	PF14	I/O	FT_ fha	-	DFSDM_CKIN6, I2C4_SCL, FMC_A8, EVENTOUT	ADC2_INN2, ADC2_INP6
-	55	P7	65	76	R9	PF15	I/O	FT_fh	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	56	N7	66	77	T8	PG0	I/O	FT_h	-	FMC_A10, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	F6	-	-	J16	VSS	S	-	-	-	-
-	-	-	-	-	H13	VDD	S	-	-	-	-
-	57	M7	67	78	U8	PG1	I/O	FT_h	-	FMC_A11, EVENTOUT	OPAMP2_ VINM
37	58	R8	68	79	U9	PE7	I/O	FT_ha	-	TIM1_ETR, DFSDM_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4/FMC_DA4, EVENTOUT	OPAMP2_ VOUT, COMP_2_ INM
38	59	P8	69	80	T9	PE8	I/O	FT_ha	-	TIM1_CH1N, DFSDM_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5/FMC_DA5, COMP_2_OUT, EVENTOUT	OPAMP2_ VINM
39	60	P9	70	81	P9	PE9	I/O	FT_ha	-	TIM1_CH1, DFSDM_CKOUT, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6/FMC_DA6, EVENTOUT	OPAMP2_ VINP, COMP_2_ INP
-	61	M9	71	82	J17	VSS	S	-	-	-	-
-	62	N9	72	83	J13	VDD	S	-	-	-	-
40	63	R9	73	84	N9	PE10	I/O	FT_ha	-	TIM1_CH2N, DFSDM_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7/FMC_DA7, EVENTOUT	COMP_2_ INM
41	64	P10	74	85	P10	PE11	I/O	FT_ha	-	TIM1_CH2, DFSDM_CKIN4, SPI4_NSS, SAI2_SD_B, FMC_D8/FMC_DA8, LCD_G3, EVENTOUT	COMP_2_ INP

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
42	65	R10	75	86	R10	PE12	I/O	FT_h	-	TIM1_CH3N, DFSDM_DATIN5, SPI4_SCK, SAI2_SCK_B, FMC_D9/FMC_DA9, COMP_1_OUT, LCD_B4, EVENTOUT	-
43	66	N11	76	87	T10	PE13	I/O	FT_h	-	TIM1_CH3, DFSDM_CKIN5, SPI4_MISO, SAI2_FS_B, FMC_D10/FMC_DA10, COMP_2_OUT, LCD_DE, EVENTOUT	-
-	-	F7	-	-	K15	VSS	S	-	-	-	-
-	-	-	-	-	K13	VDD	S	-	-	-	-
44	67	P11	77	88	U10	PE14	I/O	FT_h	-	TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11/FMC_DA11, LCD_CLK, EVENTOUT	-
45	68	R11	78	89	R11	PE15	I/O	FT_h	-	TIM1_BKIN, HDMI__TIM1_BKIN, FMC_D12/FMC_DA12, TIM1_BKIN_COMP12, LCD_R7, EVENTOUT	-
46	69	R12	79	90	P11	PB10	I/O	FT_f	-	TIM2_CH3, HRTIM_SCOUT, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
47	70	R13	80	91	P12	PB11	I/O	FT_f	-	TIM2_CH4, HRTIM_SCIN, LPTIM2_ETR, I2C2_SDA, DFSDM_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
48	71	M10	81	92	U11	VCAP1	S	-	-	-	-
49	-	K7	-	93	L15	VSS	S	-	-	-	-
-	-	-	-	-	U12	VDDLDO1	S	-	-	-	-
50	72	N10	82	94	L13	VDD	S	-	-	-	-
-	-	-	-	95	R12	PJ5	I/O	FT		LCD_R6, EVENTOUT	-
-	-	M11	83	96	T11	PH6	I/O	FT	-	TIM12_CH1, I2C2_SMBA, SPI5_SCK, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	N12	84	97	U13	PH7	I/O	FT_fa	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	M12	85	98	T13	PH8	I/O	FT_ fha	-	TIM5_ETR, I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	F8	-	-	M15	VSS	S	-	-	-	-
-	-	-	-	-	M13	VDD	S	-	-	-	-
-	-	M13	86	99	R13	PH9	I/O	FT_h	-	TIM12_CH2, I2C3_SMBA, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	L13	87	100	P13	PH10	I/O	FT_h	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	L12	88	101	P14	PH11	I/O	FT_fh	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	K12	89	102	R14	PH12	I/O	FT_fh	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	H12	90	-	N16	VSS	S	-	-	-	-
-	-	J12	91	103	P17	VDD	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
51	73	P12	92	104	T14	PB12	I/O	FT_u	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM_DATIN1, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, TIM1_BKIN_COMP12, UART5_RX, EVENTOUT	-
52	74	P13	93	105	U14	PB13	I/O	FT_u	-	TIM1_CH1N, LPTIM2_OUT, SPI2_SCK/I2S2_CK, DFSDM_CKIN1, USART3_CTS_NSS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, UART5_TX, EVENTOUT	OTG_HS_VBUS
53	75	R14	94	106	U15	PB14	I/O	FT_u	-	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, DFSDM_DATIN2, USART3_RTS, UART4_RTS, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
54	76	R15	95	107	T15	PB15	I/O	FT_u	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, DFSDM_CKIN2, UART4_CTS, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-
55	77	P15	96	108	U16	PD8	I/O	FT_h	-	DFSDM_CKIN3, SAI3_SCK_B, USART3_TX, SPDIFRX_IN1, FMC_D13/FMC_DA13, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
56	78	P14	97	109	T17	PD9	I/O	FT_h	-	DFSDM_DATIN3, SAI3_SD_B, USART3_RX, CAN2_RXFD, FMC_D14/FMC_DA14, EVENTOUT	-
57	79	N15	98	110	T16	PD10	I/O	FT_h	-	DFSDM_CKOUT, SAI3_FS_B, USART3_CK, CAN2_TXFD, FMC_D15/FMC_DA15, LCD_B3, EVENTOUT	-
-	-	-	-	-	N12	VDD	S	-	-	-	-
-	-	F9	-	-	U17	VSS	S	-	-	-	-
58	80	N14	99	111	R15	PD11	I/O	FT_h	-	LPTIM2_IN2, I2C4_SMBA, USART3_CTS_NSS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16, EVENTOUT	-
59	81	N13	100	112	R16	PD12	I/O	FT_fh	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17, EVENTOUT	-
60	82	M15	101	113	R17	PD13	I/O	FT_fh	-	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	83	K8	102	114	T12	VSS	S		-		-
-	84	J13	103	115	N11	VDD	S		-		-
61	85	M14	104	116	P16	PD14	I/O	FT_h	-	TIM4_CH3, SAI3_MCLK_B, UART8_CTS, FMC_D0/FMC_DA0, EVENTOUT	-
62	86	L14	105	117	P15	PD15	I/O	FT_h	-	TIM4_CH4, SAI3_MCLK_A, UART8_RTS, FMC_D1/FMC_DA1, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	118	N15	PJ6	I/O	FT	-	TIM8_CH2, LCD_R7, EVENTOUT	-
-	-	-	-	119	N14	PJ7	I/O	FT	-	TRGIN, TIM8_CH2N, LCD_G0, EVENTOUT	-
-	-	-	-	-	N10	VDD	S	-	-	-	-
-	-	F10	-	-	R8	VSS	S	-	-	-	-
-	-	-	-	120	N13	PJ8	I/O	FT	-	TIM1_CH3N, TIM8_CH1, UART8_TX, LCD_G1, EVENTOUT	-
-	-	-	-	121	M14	PJ9	I/O	FT	-	TIM1_CH3, TIM8_CH1N, UART8_RX, LCD_G2, EVENTOUT	-
-	-	-	-	122	L14	PJ10	I/O	FT	-	TIM1_CH2N, TIM8_CH2, SPI5_MOSI, LCD_G3, EVENTOUT	-
-	-	-	-	123	K14	PJ11	I/O	FT	-	TIM1_CH2, TIM8_CH2N, SPI5_MISO, LCD_G4, EVENTOUT	-
-	-	-	-	124	N8	VDD	S	-	-	-	-
-	-	-	-	-	P17	VDD	S	-	-	-	-
-	-	G6	-	125	U1	VSS	S	-	-	-	-
-	-	-	-	-	N17	NC	-	-	-	-	-
-	-	-	-	-	M16	NC	-	-	-	-	-
-	-	-	-	-	M17	NC	-	-	-	-	-
-	-	-	-	-	L7	VSS	S	-	-	-	-
-	-	-	-	-	L16	NC	-	-	-	-	-
-	-	-	-	-	L17	NC	-	-	-	-	-
-	-	-	-	-	K16	NC	-	-	-	-	-
-	-	-	-	-	K17	NC	-	-	-	-	-
-	-	-	-	-	L8	VSS	S	-	-	-	-
-	-	-	-	126	J14	PK0	I/O	FT	-	TIM1_CH1N, TIM8_CH3, SPI5_SCK, LCD_G5, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	127	J15	PK1	I/O	FT	-	TIM1_CH1, TIM8_CH3N, SPI5_NSS, LCD_G6, EVENTOUT	-
-	-	-	-	128	H17	PK2	I/O	FT	-	TIM1_BKIN, TIM8_BKIN, TIM8_BKIN_COMP12, TIM1_BKIN_COMP12, LCD_G7, EVENTOUT	-
-	87	L15	106	129	H16	PG2	I/O	FT_h	-	TIM8_BKIN, TIM8_BKIN_COMP12, FMC_A12, EVENTOUT	-
-	88	K15	107	130	H15	PG3	I/O	FT_h	-	TIM8_BKIN2, TIM8_BKIN2_COMP12, FMC_A13, EVENTOUT	-
-	-	G7	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	N7	VDD	S	-	-	-	-
-	89	K14	108	131	H14	PG4	I/O	FT_h	-	TIM1_BKIN2, TIM1_BKIN2_COMP12, FMC_A14/FMC_BA0, EVENTOUT	-
-	90	K13	109	132	G14	PG5	I/O	FT_h	-	TIM1_ETR, FMC_A15/FMC_BA1, EVENTOUT	-
-	91	J15	110	133	G15	PG6	I/O	FT_h	-	TIM17_BKIN, HRTIM_CHE1, QUADSPI_BK1_NCS, FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT	-
-	92	J14	111	134	F16	PG7	I/O	FT_h	-	HRTIM_CHE2, SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-
-	93	H14	112	135	F15	PG8	I/O	FT_h	-	TIM8_ETR, SPI6_NSS, USART6_RTS, SPDIFRX_IN2, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	94	G12	113	136	-	VSS	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	-	G17	VDD50USB	S	-	-	-	-
-	95	H13	114	137	F17	VDD33USB	S	-	-	-	-
-	-	-	-	-	M5	VDD	S	-	-	-	-
63	96	H15	115	138	F14	PC6	I/O	FT_h	-	HRTIM_CHA1, TIM3_CH1, TIM8_CH1, DFSDM_CKIN3, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	SWPMI_IO
64	97	G15	116	139	F13	PC7	I/O	FT_h	-	TRGIO, HRTIM_CHA2, TIM3_CH2, TIM8_CH2, DFSDM_DATIN3, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, FMC_NE1, SDMMC2_D7, SWPMI_TX, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-
65	98	G14	117	140	E13	PC8	I/O	FT_h	-	TRACED1, HRTIM_CHB1, TIM3_CH3, TIM8_CH3, USART6_CK, UART5_RTS, FMC_NE2/FMC_NCE, SWPMI_RX, SDMMC1_D0, DCMI_D2, EVENTOUT	-
66	99	F14	118	141	E14	PC9	I/O	FT_fh	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SWPMI_SUSPEND, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT	-
-	-	G8	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	L5	VDD	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
67	100	F15	119	142	E15	PA8	I/O	FT_ fha	-	MCO1, TIM1_CH1, HRTIM_CHB2, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, UART7_RX, TIM8_BKIN2_COMP12, LCD_B3, LCD_R6, EVENTOUT	-
68	101	E15	120	143	D15	PA9	I/O	FT_u	-	TIM1_CH2, HRTIM_CHC1, LPUART1_TX, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, CAN1_RXFD, ETH_TX_ER, DCMI_D0, LCD_R5, EVENTOUT	OTG_FS_ VBUS
69	102	D15	121	144	D14	PA10	I/O	FT_u	-	TIM1_CH3, HRTIM_CHC2, LPUART1_RX, USART1_RX, CAN1_TXFD, OTG_FS_ID, MDIOS_MDIO, LCD_B4, DCMI_D1, LCD_B1, EVENTOUT	-
70	103	C15	122	145	E17	PA11	I/O	FT_u	-	TIM1_CH4, HRTIM_CHD1, LPUART1_CTS, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS_NSS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
71	104	B15	123	146	E16	PA12	I/O	FT_u	-	TIM1_ETR, HRTIM_CHD2, LPUART1_RTS, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	105	A15	124	147	C15	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	106	F13	125	148	D17	VCAP2	S	-	-	-	-
74	107	F12	126	149	-	VSS	S	-	-	-	-
-	-	-	-	-	C17	VDDLDO2	-	-	-	-	-
75	108	G13	127	150	K5	VDD	S	-	-	-	-
-	-	E12	128	151	D16	PH13	I/O	FT_h	-	TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	E13	129	152	B17	PH14	I/O	FT_h	-	TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	D13	130	153	B16	PH15	I/O	FT_h	-	TIM8_CH3N, CAN1_TXFD, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	E14	131	154	A16	PI0	I/O	FT_h	-	TIM5_CH4, SPI2_NSS/I2S2_WS, CAN1_RXFD, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	G9	-	-	-	VSS	S	-	-	-	-
-	-	D14	132	155	A15	PI1	I/O	FT_h	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, TIM8_BKIN2_COMP12, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	C14	133	156	B15	PI2	I/O	FT_h	-	TIM8_CH4, SPI2_MISO/I2S2_SDI, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	C13	134	157	C14	PI3	I/O	FT_h	-	TIM8_ETR, SPI2_MOSI/I2S2_SDO, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	D9	135	-	-	VSS	S	-	-	-	-
-	-	C9	136	158	-	VDD	S	-	-	-	-
76	109	A14	137	159	B14	PA14(JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
77	110	A13	138	160	A14	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HRTIM_FLT1, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, UART7_TX, EVENTOUT	-
78	111	B14	139	161	A13	PC10	I/O	FT_ha	-	HRTIM_EEV1, DFSDM_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	112	B13	140	162	B13	PC11	I/O	FT_h	-	HRTIM_FLT2, DFSDM_DATIN5, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT	-
80	113	A12	141	163	C12	PC12	I/O	FT_h	-	TRACED3, HRTIM_EEV2, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-
-	-	G10	-	-	-	VDD	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
81	114	B12	142	164	D13	PD0	I/O	FT_h	-	DFSDM_CKIN6, SAI3_SCK_A, UART4_RX, CAN1_RX, FMC_D2/FMC_DA2, EVENTOUT	-
82	115	C12	143	165	E12	PD1	I/O	FT_h	-	DFSDM_DATIN6, SAI3_SD_A, UART4_TX, CAN1_TX, FMC_D3/FMC_DA3, EVENTOUT	-
83	116	D12	144	166	D12	PD2	I/O	FT_h	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT	-
84	117	D11	145	167	B12	PD3	I/O	FT_h	-	DFSDM_CKOUT, SPI2_SCK/I2S2_CK, USART2_CTS_NSS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
85	118	D10	146	168	A12	PD4	I/O	FT_h	-	HRTIM_FLT3, SAI3_FS_A, USART2_RTS, CAN1_RXFD, FMC_NOE, EVENTOUT	-
86	119	C11	147	169	A11	PD5	I/O	FT_h	-	HRTIM_EEV3, USART2_TX, CAN1_TXFD, FMC_NWE, EVENTOUT	-
-	120	D8	148	170	R4	VSS	S	-	-	-	-
-	121	C8	149	171	-	VDD	S	-	-	-	-
87	122	B11	150	172	B11	PD6	I/O	FT_h	-	SAI1_D1, DFSDM_CKIN4, DFSDM_DATIN1, SPI3_MOSI/I2S3_SDO, SAI1_SD_A, USART2_RX, SAI4_SD_A, CAN2_RXFD, SAI4_D1, SDMMC2_CK, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
88	123	A11	151	173	C11	PD7	I/O	FT_h	-	DFSDM_DATIN4, SPI1_MOSI/I2S1_SDO, DFSDM_CKIN1, USART2_CK, SPDIFRX_IN0, SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	-	-	174	D11	PJ12	I/O	FT	-	TRGOUT, LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	-	175	E10	PJ13	I/O	FT	-	LCD_B4, LCD_B1, EVENTOUT	-
-	-	-	-	176	D10	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	177	B10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	-	H6	-	-	-	VSS	S	-	-	-	-
-	124	C10	152	178	A10	PG9	I/O	FT_h	-	SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX_IN3, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	125	B10	153	179	A9	PG10	I/O	FT_h	-	HRTIM_FLT5, SPI1_NSS/I2S1_WS, LCD_G3, SAI2_SD_B, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	126	B9	154	180	B9	PG11	I/O	FT_h	-	HRTIM_EEV4, SPI1_SCK/I2S1_CK, SPDIFRX_IN0, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	127	B8	155	181	C9	PG12	I/O	FT_h	-	LPTIM1_IN1, HRTIM_EEV5, SPI6_MISO, USART6_RTS, SPDIFRX_IN1, LCD_B4, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_NE4, LCD_B1, EVENTOUT	-
-	128	A8	156	182	D9	PG13	I/O	FT_h	-	TRACED0, LPTIM1_OUT, HRTIM_EEV10, SPI6_SCK, USART6_CTS_NSS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT	-
-	129	A7	157	183	D8	PG14	I/O	FT_h	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT	-
-	130	D7	158	184	-	VSS	S	-	-		-
-	131	C7	159	185	-	VDD	S	-	-	-	-
-	-	-	-	186	C8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	187	B8	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	188	A8	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	189	C7	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	190	D7	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	-	H7	-	-	-	VSS	S	-	-	-	-
-	132	B7	160	191	D6	PG15	I/O	FT_h	-	USART6_CTS_NSS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
89	133	A10	161	192	C6	PB3(JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, HRTIM_FLT4, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK, SDMMC2_D2, UART7_RX, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
90	134	A9	162	193	B7	PB4(NJTRST)	I/O	FT	-	NJTRST, TIM16_BKIN, TIM3_CH1, HRTIM_EEV6, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, UART7_TX, EVENTOUT	-
91	135	A6	163	194	A5	PB5	I/O	FT	-	TIM17_BKIN, TIM3_CH2, HRTIM_EEV7, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, SPI3_MOSI/I2S3_SDO, SPI6_MOSI, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, UART5_RX, EVENTOUT	-
-	-	H8	-	-	-	VSS	S	-	-	-	-
92	136	B6	164	195	B5	PB6	I/O	FT_f	-	TIM16_CH1N, TIM4_CH1, HRTIM_EEV8, I2C1_SCL, HDMI_CEC, I2C4_SCL, USART1_TX, LPUART1_TX, CAN2_TX, QUADSPI_BK1_NCS, DFSDM_DATIN5, FMC_SDNE1, DCMI_D5, UART5_TX, EVENTOUT	-
93	137	B5	165	196	C5	PB7	I/O	FT_fa	-	TIM17_CH1N, TIM4_CH2, HRTIM_EEV9, I2C1_SDA, I2C4_SDA, USART1_RX, LPUART1_RX, CAN2_TXFD, DFSDM_CKIN5, FMC_NL, DCMI_VSYNC, EVENTOUT	PVD_IN
94	138	D6	166	197	E8	BOOT0	I	B	-	-	VPP

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
95	139	A5	167	198	D5	PB8	I/O	FT_fh	-	TIM16_CH1, TIM4_CH3, DFSDM_CKIN7, I2C1_SCL, I2C4_SCL, SDMMC1_CKIN, UART4_RX, CAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-
96	140	B4	168	199	D4	PB9	I/O	FT_fh	-	TIM17_CH1, TIM4_CH4, DFSDM_DATIN7, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C4_SDA, SDMMC1_CDIR, UART4_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	A4	169	200	C4	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, HRTIM_SCIN, LPTIM2_ETR, UART8_RX, CAN1_RXFD, SAI2_MCK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A3	170	201	B4	PE1	I/O	FT_h	-	LPTIM1_IN2, HRTIM_SCOUT, UART8_TX, CAN1_TXFD, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	A7	VCAP3	S	-	-	-	-
99	-	D5	-	202	-	VSS	S	-	-	-	-
-	143	C6	171	203	E7	PDR_ON	S	FT			-
-	-	-	-	-	A6	VDDLDO3	S	-	-	-	-
100	144	C5	172	204	-	VDD	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	D4	173	205	A4	PI4	I/O	FT_h	-	TIM8_BKIN, SAI2_MCK_A, TIM8_BKIN_COMP12, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	C4	174	206	A3	PI5	I/O	FT_h	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	C3	175	207	A2	PI6	I/O	FT_h	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	C2	176	208	B3	PI7	I/O	FT_h	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-
-	-	H9	-	-	-	VSS	S	-	-	-	-
-	-	K9	-	-	-	VSS	S	-	-	-	-
-	-	K10	-	-	-	VSS	S	-	-	-	-

1. Pxy_C and Pxy pins/balls are two separate pads (analog switch open). The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.

2. There is a direct path between Pxy_C and Pxy pins/balls, through an analog switch. Pxy alternate functions are available on Pxy_C when the analog switch is closed. The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.

Table 8. Port A alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	TIM15_BKIN	-	-	USART2_CTS_NSS	UART4_TX	SDMMC2_CMD	SAI2_SD_B	ETH_MII_CRS	-	-	-	EVENT-OUT
Port A	PA1	-	TIM2_CH2	TIM5_CH2	LPTIM3_OUT	TIM15_CH1N	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	SAI2_MCK_B	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	LCD_R2	EVENT-OUT
Port A	PA2	-	TIM2_CH3	TIM5_CH3	LPTIM4_OUT	TIM15_CH1	-	-	USART2_TX	SAI2_SCK_B	-	-	ETH_MDIO	MDIOS_MDIO	-	LCD_R1	EVENT-OUT
Port A	PA3	-	TIM2_CH4	TIM5_CH4	LPTIM5_OUT	TIM15_CH2	-	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENT-OUT
Port A	PA4	-	-	TIM5_ETR	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	SPI6_NSS	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENT-OUT
Port A	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	SPI6_SCK	-	OTG_HS_ULPI_CK	-	-	-	LCD_R4	EVENT-OUT
Port A	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO/I2S1_SDI	-	-	SPI6_MISO	TIM13_CH1	TIM8_BKIN_COMP12	MDIOS_MDC	TIM1_BKIN_COMP12	DCMI_PIXCLK	LCD_G2	EVENT-OUT
Port A	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SDO	-	-	SPI6_MOSI	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	-	EVENT-OUT
Port A	PA8	MCO1	TIM1_CH1	HRTIM_CHB2	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	UART7_RX	TIM8_BKIN2_COMP12	LCD_B3	LCD_R6	EVENT-OUT
Port A	PA9	-	TIM1_CH2	HRTIM_CHC1	LPUART1_TX	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	CAN1_RXFD	-	ETH_TX_ER	-	DCMI_D0	LCD_R5	EVENT-OUT
Port A	PA10	-	TIM1_CH3	HRTIM_CHC2	LPUART1_RX	-	-	-	USART1_RX	-	CAN1_TXFD	OTG_FS_ID	MDIOS_MDIO	LCD_B4	DCMI_D1	LCD_B1	EVENT-OUT
Port A	PA11	-	TIM1_CH4	HRTIM_CHD1	LPUART1_CTS	-	SPI2_NSS/I2S2_WS	UART4_RX	USART1_CTS_NSS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENT-OUT
Port A	PA12	-	TIM1_ETR	HRTIM_CHD2	LPUART1_RTS	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENT-OUT
Port A	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT

Table 8. Port A alternate functions (continued)

	Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port A	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	HRTIM_FLT1	-	HDMI_CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS	UART4_RTS	-	-	UART7_TX	-	-	-	EVENT-OUT

Table 9. Port B alternate functions

	Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENT-OUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENT-OUT
	PB2	-	-	SAI1_D1	-	DFSDM_CKIN1	-	SAI1_SD_A	SPI3_MOSI/I2S3_SDO	SAI4_SD_A	QUADSPI_CLK	SAI4_D1	ETH_TX_ER	-	-	-	EVENT-OUT
	PB3	JTDO/TRACESWO	TIM2_CH2	HRTIM_FLT4	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	SDMMC2_D2	-	UART7_RX	-	-	-	EVENT-OUT
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	HRTIM_EEV6	-	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/I2S2_WS	SPI6_MISO	SDMMC2_D3	-	UART7_TX	-	-	-	EVENT-OUT
	PB5	-	TIM17_BKIN	TIM3_CH2	HRTIM_EEV7	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	I2C4_SMBA	SPI3_MOSI/I2S3_SDO	SPI6_MOSI	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	UART5_RX	EVENT-OUT
	PB6	-	TIM16_CH1N	TIM4_CH1	HRTIM_EEV8	I2C1_SCL	HDMI_CEC	I2C4_SCL	USART1_TX	LPUART1_TX	CAN2_TX	QUADSPI_BK1_NCS	DFSDM_DATIN5	FMC_SDNE1	DCMI_D5	UART5_TX	EVENT-OUT
	PB7	-	TIM17_CH1N	TIM4_CH2	HRTIM_EEV9	I2C1_SDA	-	I2C4_SDA	USART1_RX	LPUART1_RX	CAN2_TXFD	-	DFSDM_CKIN5	FMC_NL	DCMI_VSYNC	-	EVENT-OUT
	PB8	-	TIM16_CH1	TIM4_CH3	DFSDM_CKIN7	I2C1_SCL	-	I2C4_SCL	SDMMC1_CKIN	UART4_RX	CAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6	LCD_B6	EVENT-OUT

Table 9. Port B alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port B	PB9	-	TIM17_CH1	TIM4_CH4	DFSDM_DATIN7	I2C1_SDA	SPI2_NSS/I2S2_WS	I2C4_SDA	SDMMC1_CDIR	UART4_TX	CAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC1_D5	DCMI_D7	LCD_B7	EVENT-OUT
Port B	PB10	-	TIM2_CH3	HRTIM_SCOUT	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM_DATIN7	USART3_TX	-	QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENT-OUT
Port B	PB11	-	TIM2_CH4	HRTIM_SCIN	LPTIM2_ETR	I2C2_SDA	-	DFSDM_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	-	LCD_G5	EVENT-OUT
Port B	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	DFSDM_DATIN1	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	TIM1_BKIN_COMP12	UART5_RX	EVENT-OUT
Port B	PB13	-	TIM1_CH1N	-	LPTIM2_OUT	-	SPI2_SCK/I2S2_CK	DFSDM_CKIN1	USART3_CTS_NSS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	UART5_TX	EVENT-OUT
Port B	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/I2S2_SDI	DFSDM_DATIN2	USART3_RTS	UART4_RTS	SDMMC2_D0	-	-	OTG_HS_DM	-	-	EVENT-OUT
Port B	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SDO	DFSDM_CKIN2	-	UART4_CTS	SDMMC2_D1	-	-	OTG_HS_DP	-	-	EVENT-OUT

Table 10. Port C alternate functions

	Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port C	PC0	-	-	-	DFSDM_CKIN0	-	-	DFSDM_DATIN4	-	SAI2_FS_B	-	OTG_HS_ULPI_STP	-	FMC_SDNWE	-	LCD_R5	EVENT-OUT
	PC1	TRACED0	-	SAI1_D1	DFSDM_DATIN0	DFSDM_CKIN4	SPI2_MOSI/I2S2_SDO	SAI1_SD_A	-	SAI4_SD_A	SDMMC2_CK	SAI4_D1	ETH_MDC	MDIOS_MDC	-	-	EVENT-OUT
	PC2	-	-	-	DFSDM_CKIN1	-	SPI2_MISO/I2S2_SDI	DFSDM_CKOUT	-	-	-	OTG_HS_ULPI_DIR	ETH_MII_TXD2	FMC_SDNE0	-	-	EVENT-OUT
	PC3	-	-	-	DFSDM_DATIN1	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	OTG_HS_ULPI_NXT	ETH_MII_TX_CLK	FMC_SDCKE0	-	-	EVENT-OUT
	PC4	-	-	-	DFSDM_CKIN2	-	I2S1_MCK	-	-	-	SPDIFRX_IN2	-	ETH_MII_RXD0/ETH_RMII_RXD0	FMC_SDNE0	-	-	EVENT-OUT
	PC5	-	-	SAI1_D3	DFSDM_DATIN2	-	-	-	-		SPDIFRX_IN3	SAI4_D3	ETH_MII_RXD1/ETH_RMII_RXD1	FMC_SDCKE0	COMP_1_OUT	-	EVENT-OUT
	PC6	-	HRTIM_CHA1	TIM3_CH1	TIM8_CH1	DFSDM_CKIN3	I2S2_MCK	-	USART6_TX	SDMMC1_D0DIR	FMC_NWAIT	SDMMC2_D6	-	SDMMC1_D6	DCMI_D0	LCD_HSYNC	EVENT-OUT
	PC7	TRGIO	HRTIM_CHA2	TIM3_CH2	TIM8_CH2	DFSDM_DATIN3	-	I2S3_MCK	USART6_RX	SDMMC1_D123DIR	FMC_NE1	SDMMC2_D7	SWPMI_TX	SDMMC1_D7	DCMI_D1	LCD_G6	EVENT-OUT
	PC8	TRACED1	HRTIM_CHB1	TIM3_CH3	TIM8_CH3	-	-	-	USART6_CK	UART5_RTS	FMC_NE2/FMC_NCE	-	SWPMI_RX	SDMMC1_D0	DCMI_D2	-	EVENT-OUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	UART5_CTS	QUADSPI_BK1_IO0	LCD_G3	SWPMI_SUSPEND	SDMMC1_D1	DCMI_D3	LCD_B2	EVENT-OUT
	PC10	-	-	HRTIM_EEV1	DFSDM_CKIN5	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	QUADSPI_BK1_IO1	-	-	SDMMC1_D2	DCMI_D8	LCD_R2	EVENT-OUT
	PC11	-	-	HRTIM_FLT2	DFSDM_DATIN5	-	-	SPI3_MISO/I2S3_SDI	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	-	-	SDMMC1_D3	DCMI_D4	-	EVENT-OUT
	PC12	TRACED3	-	HRTIM_EEV2	-	-	-	SPI3_MOSI/I2S3_SDO	USART3_CK	UART5_TX	-	-	-	SDMMC1_CK	DCMI_D9	-	EVENT-OUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT

Table 10. Port C alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port C	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT

Table 11. Port D alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port D	PD0	-	-	-	DFSDM_CKIN6	-	-	SAI3_SCK_A	-	UART4_RX	CAN1_RX	-	-	FMC_D2/FMC_DA2	-	-	EVENT-OUT
	PD1	-	-	-	DFSDM_DATIN6	-	-	SAI3_SD_A	-	UART4_TX	CAN1_TX	-	-	FMC_D3/FMC_DA3	-	-	EVENT-OUT
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDMMC1_CMD	DCMI_D11	-	EVENT-OUT
	PD3	-	-	-	DFSDM_CKOUT	-	SPI2_SCK/I2S2_CK	-	USART2_CTS_NSS	-	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVENT-OUT
	PD4	-	-	HRTIM_FLT3	-	-	-	SAI3_FS_A	USART2_RTS	-	CAN1_RXFD	-	-	FMC_NOE	-	-	EVENT-OUT
	PD5	-	-	HRTIM_EEV3	-	-	-	-	USART2_TX	-	CAN1_TXFD	-	-	FMC_NWE	-	-	EVENT-OUT
	PD6	-	-	SAI1_D1	DFSDM_CKIN4	DFSDM_DATIN1	SPI3_MOSI/I2S3_SDO	SAI1_SD_A	USART2_RX	SAI4_SD_A	CAN2_RXFD	SAI4_D1	SDMMC2_CK	FMC_NWAIT	DCMI_D10	LCD_B2	EVENT-OUT
	PD7	-	-	-	DFSDM_DATIN4	-	SPI1_MOSI/I2S1_SDO	DFSDM_CKIN1	USART2_CK	-	SPDIFRX_IN0	-	SDMMC2_CMD	FMC_NE1	-	-	EVENT-OUT
	PD8	-	-	-	DFSDM_CKIN3	-	-	SAI3_SCK_B	USART3_TX	-	SPDIFRX_IN1	-	-	FMC_D13/FMC_DA13	-	-	EVENT-OUT
	PD9	-	-	-	DFSDM_DATIN3	-	-	SAI3_SD_B	USART3_RX	-	CAN2_RXFD	-	-	FMC_D14/FMC_DA14	-	-	EVENT-OUT
	PD10	-	-	-	DFSDM_CKOUT	-	-	SAI3_FS_B	USART3_CK	-	CAN2_TXFD	-	-	FMC_D15/FMC_DA15	-	LCD_B3	EVENT-OUT
	PD11	-	-	-	LPTIM2_IN2	I2C4_SMBA	-	-	USART3_CTS_NSS	-	QUADSPI_BK1_IO0	SAI2_SD_A	-	FMC_A16	-	-	EVENT-OUT
	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	I2C4_SCL	-	-	USART3_RTS	-	QUADSPI_BK1_IO1	SAI2_FS_A	-	FMC_A17	-	-	EVENT-OUT
	PD13	-	LPTIM1_OUT	TIM4_CH2	-	I2C4_SDA	-	-		-	QUADSPI_BK1_IO3	SAI2_SCK_A	-	FMC_A18	-	-	EVENT-OUT
	PD14	-	-	TIM4_CH3	-	-	-	SAI3_MCLK_B	-	UART8_CTS	-	-	-	FMC_D0/FMC_DA0	-	-	EVENT-OUT
	PD15	-	-	TIM4_CH4	-	-	-	SAI3_MCLK_A	-	UART8_RTS	-	-	-	FMC_D1/FMC_DA1	-	-	EVENT-OUT

Table 12. Port E alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port E	PE0	-	LPTIM1_ETR	TIM4_ETR	HRTIM_SCIN	LPTIM2_ETR	-	-	-	UART8_RX	CAN1_RXFD	SAI2_MCK_A	-	FMC_NBL0	DCMI_D2	-	EVENT-OUT
Port E	PE1	-	LPTIM1_IN2	-	HRTIM_SCOUT	-	-	-	-	UART8_TX	CAN1_TXFD	-	-	FMC_NBL1	DCMI_D3	-	EVENT-OUT
Port E	PE2	TRACECLK	-	SAI1_CK1	-	-	SPI4_SCK	SAI1_MCLK_A	-	SAI4_MCLK_A	QUADSPI_BK1_IO2	SAI4_CK1	ETH_MII_TXD3	FMC_A23	-	-	EVENT-OUT
Port E	PE3	TRACED0	-	-	-	TIM15_BKIN	-	SAI1_SD_B	-	SAI4_SD_B	-	-	-	FMC_A19	-	-	EVENT-OUT
Port E	PE4	TRACED1	-	SAI1_D2	DFSDM_DATIN3	TIM15_CH1N	SPI4_NSS	SAI1_FS_A	-	SAI4_FS_A	-	SAI4_D2	-	FMC_A20	DCMI_D4	LCD_B0	EVENT-OUT
Port E	PE5	TRACED2	-	SAI1_CK2	DFSDM_CKIN3	TIM15_CH1	SPI4_MISO	SAI1_SCK_A	-	SAI4_SCK_A	-	SAI4_CK2	-	FMC_A21	DCMI_D6	LCD_G0	EVENT-OUT
Port E	PE6	TRACED3	TIM1_BKIN2	SAI1_D1	-	TIM15_CH2	SPI4_MOSI	SAI1_SD_A	-	SAI4_SD_A	SAI4_D1	SAI2_MCK_B	TIM1_BKIN2_COMP12	FMC_A22	DCMI_D7	LCD_G1	EVENT-OUT
Port E	PE7	-	TIM1_ETR	-	DFSDM_DATIN2	-	-	-	UART7_RX	-	-	QUADSPI_BK2_IO0	-	FMC_D4/FMC_DA4	-	-	EVENT-OUT
Port E	PE8	-	TIM1_CH1N	-	DFSDM_CKIN2	-	-	-	UART7_TX	-	-	QUADSPI_BK2_IO1	-	FMC_D5/FMC_DA5	COMP_2_OUT	-	EVENT-OUT
Port E	PE9	-	TIM1_CH1	-	DFSDM_CKOUT	-	-	-	UART7_RTS	-	-	QUADSPI_BK2_IO2	-	FMC_D6/FMC_DA6	-	-	EVENT-OUT
Port E	PE10	-	TIM1_CH2N	-	DFSDM_DATIN4	-	-	-	UART7_CTS	-	-	QUADSPI_BK2_IO3	-	FMC_D7/FMC_DA7	-	-	EVENT-OUT
Port E	PE11	-	TIM1_CH2	-	DFSDM_CKIN4	-	SPI4_NSS	-	-	-	-	SAI2_SD_B	-	FMC_D8/FMC_DA8	-	LCD_G3	EVENT-OUT
Port E	PE12	-	TIM1_CH3N	-	DFSDM_DATIN5	-	SPI4_SCK	-	-	-	-	SAI2_SCK_B	-	FMC_D9/FMC_DA9	COMP_1_OUT	LCD_B4	EVENT-OUT
Port E	PE13	-	TIM1_CH3	-	DFSDM_CKIN5	-	SPI4_MISO	-	-	-	-	SAI2_FS_B	-	FMC_D10/FMC_DA10	COMP_2_OUT	LCD_DE	EVENT-OUT
Port E	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	SAI2_MCK_B	-	FMC_D11/FMC_DA11	-	LCD_CLK	EVENT-OUT
Port E	PE15	-	TIM1_BKIN	-	-	-	HDMI__TIM1_BKIN	-	-	-	-		-	FMC_D12/FMC_DA12	TIM1_BKIN_COMP12	LCD_R7	EVENT-OUT

Table 13. Port F alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVENT-OUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVENT-OUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENT-OUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVENT-OUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVENT-OUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENT-OUT
	PF6	-	TIM16_CH1	-	-	-	SPI5_NSS	SAI1_SD_B	UART7_RX	SAI4_SD_B	QUADSPI_BK1_IO3	-	-	-	-	-	EVENT-OUT
	PF7	-	TIM17_CH1	-	-	-	SPI5_SCK	SAI1_MCLK_B	UART7_TX	SAI4_MCLK_B	QUADSPI_BK1_IO2	-	-	-	-	-	EVENT-OUT
	PF8	-	TIM16_CH1N	-	-	-	SPI5_MISO	SAI1_SCK_B	UART7_RTS	SAI4_SCK_B	TIM13_CH1	QUADSPI_BK1_IO0	-	-	-	-	EVENT-OUT
	PF9	-	TIM17_CH1N	-	-	-	SPI5_MOSI	SAI1_FS_B	UART7_CTS	SAI4_FS_B	TIM14_CH1	QUADSPI_BK1_IO1	-	-	-	-	EVENT-OUT
	PF10	-	TIM16_BKIN	SAI1_D3	-	-	-	-	-	-	QUADSPI_CLK	SAI4_D3	-	-	DCMI_D11	LCD_DE	EVENT-OUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	SAI2_SD_B	-	FMC_SDNRAS	DCMI_D12	-	EVENT-OUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENT-OUT
	PF13	-	-	-	DFSDM_DATIN6	I2C4_SMBA	-	-	-	-	-	-	-	FMC_A7	-	-	EVENT-OUT
	PF14	-	-	-	DFSDM_CKIN6	I2C4_SCL	-	-	-	-	-	-	-	FMC_A8	-	-	EVENT-OUT
	PF15	-	-	-	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENT-OUT

Table 14. Port G alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENT-OUT
Port G	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENT-OUT
Port G	PG2	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	TIM8_BKIN_COMP12	FMC_A12	-	-	EVENT-OUT
Port G	PG3	-	-	-	TIM8_BKIN2	-	-	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_A13	-	-	EVENT-OUT
Port G	PG4	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-	TIM1_BKIN2_COMP12	FMC_A14/FMC_BA0	-	-	EVENT-OUT
Port G	PG5	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	-	-	EVENT-OUT
Port G	PG6	-	TIM17_BKIN	HRTIM_CHE1	-	-	-	-	-	-	-	QUADSPI_BK1_NCS	-	FMC_NE3	DCMI_D12	LCD_R7	EVENT-OUT
Port G	PG7	-	-	HRTIM_CHE2	-	-	-	SAI1_MCLK_A	USART6_CK	-	-	-	-	FMC_INT	DCMI_D13	LCD_CLK	EVENT-OUT
Port G	PG8	-	-	-	TIM8_ETR	-	SPI6_NSS	-	USART6_RTS	SPDIFRX_IN2	-	-	ETH_PPS_OUT	FMC_SDCLK	-	LCD_G7	EVENT-OUT
Port G	PG9	-	-	-	-	-	SPI1_MISO/I2S1_SDI	-	USART6_RX	SPDIFRX_IN3	QUADSPI_BK2_IO2	SAI2_FS_B	-	FMC_NE2/FMC_NCE	DCMI_VSYNC	-	EVENT-OUT
Port G	PG10	-	-	HRTIM_FLT5	-	-	SPI1_NSS/I2S1_WS	-	-	-	LCD_G3	SAI2_SD_B	-	FMC_NE3	DCMI_D2	LCD_B2	EVENT-OUT
Port G	PG11	-	-	HRTIM_EEV4	-	-	SPI1_SCK/I2S1_CK	-	-	SPDIFRX_IN0	-	SDMMC2_D2	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	DCMI_D3	LCD_B3	EVENT-OUT
Port G	PG12	-	LPTIM1_IN1	HRTIM_EEV5	-	-	SPI6_MISO		USART6_RTS	SPDIFRX_IN1	LCD_B4	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_NE4	-	LCD_B1	EVENT-OUT
Port G	PG13	TRACED0	LPTIM1_OUT	HRTIM_EEV10	-	-	SPI6_SCK	-	USART6_CTS_NSS	-	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	-	LCD_R0	EVENT-OUT

Table 14. Port G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port G	PG14	TRACED1	LPTIM1_ETR	-	-	-	SPI6_MOSI	-	USART6_TX		QUADSPI_BK2_IO3	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	-	LCD_B0	EVENT-OUT
Port G	PG15	-	-	-	-	-	-	-	USART6_CTS_NSS	-	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENT-OUT

Table 15. Port H alternate functions

	Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
Port H	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
Port H	PH2	-	LPTIM1_IN2	-	-	-	-	-	-	-	QUADSPI_BK2_IO0	SAI2_SCK_B	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVENT-OUT
Port H	PH3	-	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO1	SAI2_MCK_B	ETH_MII_COL	FMC_SDNE0	-	LCD_R1	EVENT-OUT
Port H	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	LCD_G5	OTG_HS_ULPI_NXT	-	-	-	LCD_G4	EVENT-OUT
Port H	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENT-OUT
Port H	PH6	-	-	TIM12_CH1	-	I2C2_SMBA	SPI5_SCK	-	-	-	-	-	ETH_MII_RXD2	FMC_SDNE1	DCMI_D8	-	EVENT-OUT
Port H	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	ETH_MII_RXD3	FMC_SDCKE1	DCMI_D9	-	EVENT-OUT
Port H	PH8	-	-	TIM5_ETR	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC	LCD_R2	EVENT-OUT
Port H	PH9	-	-	TIM12_CH2	-	I2C3_SMBA	-	-	-	-	-	-	-	FMC_D17	DCMI_D0	LCD_R3	EVENT-OUT
Port H	PH10	-	-	TIM5_CH1	-	I2C4_SMBA	-	-	-	-	-	-	-	FMC_D18	DCMI_D1	LCD_R4	EVENT-OUT
Port H	PH11	-	-	TIM5_CH2	-	I2C4_SCL	-	-	-	-	-	-	-	FMC_D19	DCMI_D2	LCD_R5	EVENT-OUT
Port H	PH12	-	-	TIM5_CH3	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_D20	DCMI_D3	LCD_R6	EVENT-OUT
Port H	PH13	-	-	-	TIM8_CH1N	-	-	-	-	UART4_TX	CAN1_TX	-	-	FMC_D21	-	LCD_G2	EVENT-OUT
Port H	PH14	-	-	-	TIM8_µCH2N	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D22	DCMI_D4	LCD_G3	EVENT-OUT
Port H	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	CAN1_TXFD	-	-	FMC_D23	DCMI_D11	LCD_G4	EVENT-OUT

Table 16. Port I alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	CAN1_RXFD	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENT-OUT
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_D25	DCMI_D8	LCD_G6	EVENT-OUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO/I2S2_SDI	-	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENT-OUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	-	-	FMC_D27	DCMI_D10	-	EVENT-OUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK_A	TIM8_BKIN_COMP12	FMC_NBL2	DCMI_D5	LCD_B4	EVENT-OUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENT-OUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6	LCD_B6	EVENT-OUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	DCMI_D7	LCD_B7	EVENT-OUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PI9	-	-	-	-	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVENT-OUT
	PI10	-	-	-	-	-	-	-	-	-	CAN1_RXFD	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVENT-OUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	-	EVENT-OUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	ETH_TX_ER	-	-	LCD_HSYNC	EVENT-OUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENT-OUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENT-OUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENT-OUT

Table 17. Port J alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port J	PJ0	-	-	-	-	-	-	-	-	-	LCD_R7	-	-	-	-	LCD_R1	EVENT-OUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVENT-OUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R3	EVENT-OUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVENT-OUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVENT-OUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVENT-OUT
	PJ6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVENT-OUT
	PJ7	TRGIN	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVENT-OUT
	PJ8	-	TIM1_CH3N	-	TIM8_CH1	-	-	-	-	UART8_TX	-	-	-	-	-	LCD_G1	EVENT-OUT
	PJ9	-	TIM1_CH3	-	TIM8_CH1N	-	-	-	-	UART8_RX	-	-	-	-	-	LCD_G2	EVENT-OUT
	PJ10	-	TIM1_CH2N	-	TIM8_CH2	-	SPI5_MOSI	-	-	-	-	-	-	-	-	LCD_G3	EVENT-OUT
	PJ11	-	TIM1_CH2	-	TIM8_CH2N	-	SPI5_MISO	-	-	-	-	-	-	-	-	LCD_G4	EVENT-OUT
	PJ12	TRGOUT	-	-	-	-	-	-	-	-	LCD_G3	-	-	-	-	LCD_B0	EVENT-OUT
	PJ13	-	-	-	-	-	-	-	-	-	LCD_B4	-	-	-	-	LCD_B1	EVENT-OUT
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVENT-OUT
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVENT-OUT

Table 18. Port K alternate functions

	Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port K	PK0	-	TIM1_CH1N	-	TIM8_CH3	-	SPI5_SCK	-	-	-	-	-	-	-	-	LCD_G5	EVENT-OUT
Port K	PK1	-	TIM1_CH1	-	TIM8_CH3N	-	SPI5_NSS	-	-	-	-	-	-	-	-	LCD_G6	EVENT-OUT
Port K	PK2	-	TIM1_BKIN	-	TIM8_BKIN	-	-	-	-	-	-	TIM8_BKIN_COMP12	TIM1_BKIN_COMP12	-	-	LCD_G7	EVENT-OUT
Port K	PK3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVENT-OUT
Port K	PK4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVENT-OUT
Port K	PK5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVENT-OUT
Port K	PK6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVENT-OUT
Port K	PK7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE	EVENT-OUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 °C and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

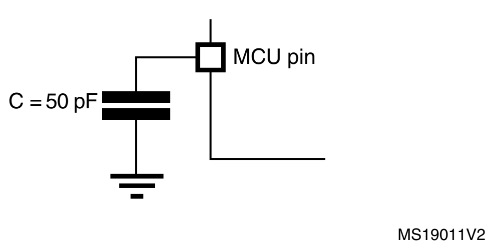
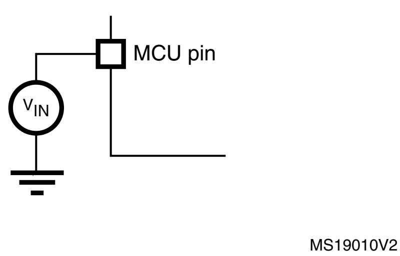
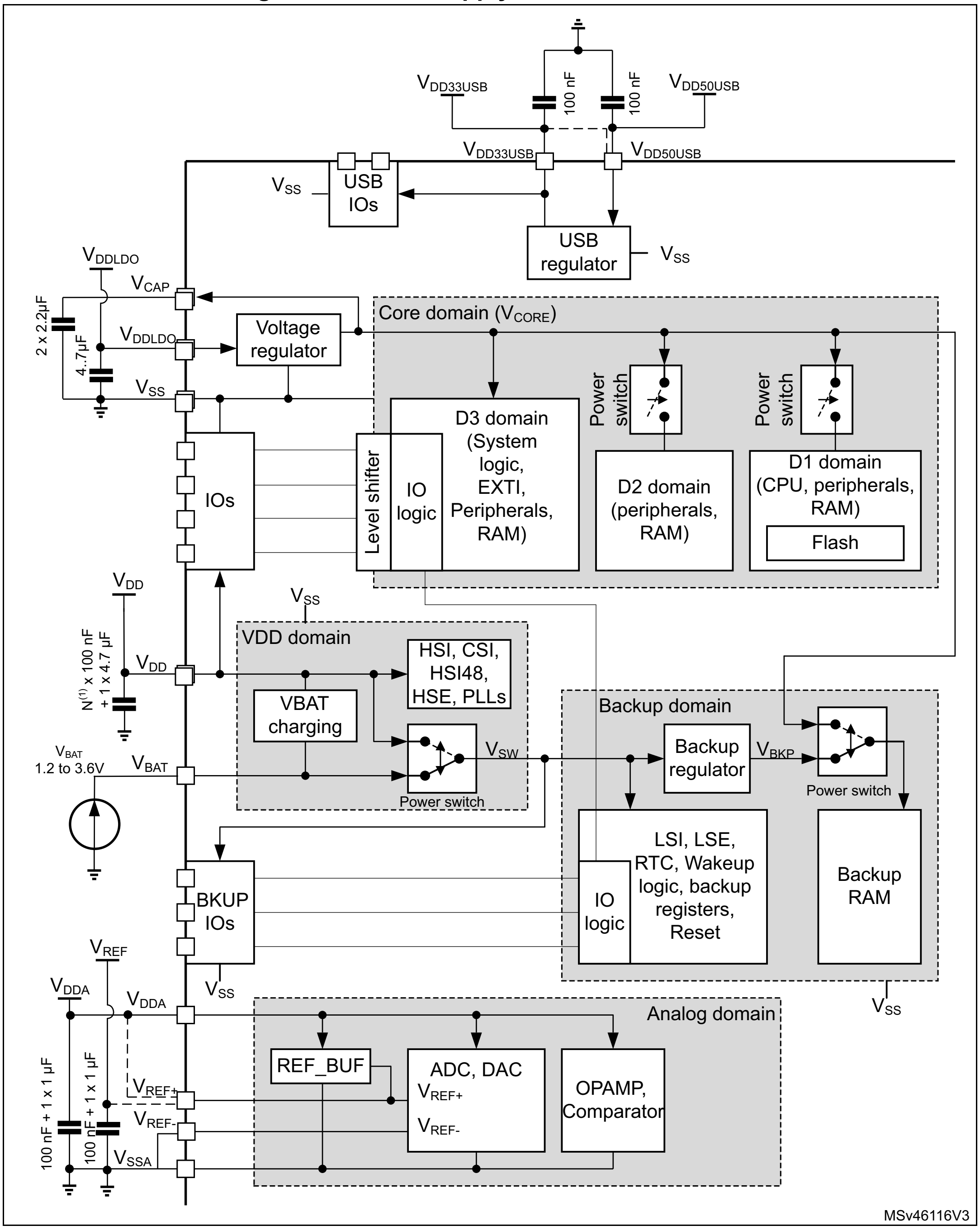


Figure 10. Pin input voltage



6.1.6 Power supply scheme

Figure 11. Power supply scheme

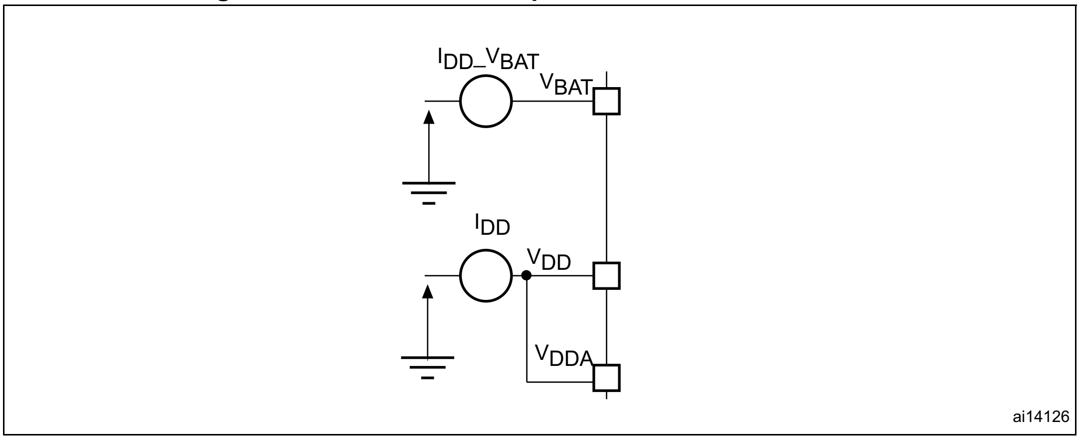


1. N corresponds to the number of VDD pins available on the package..

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics (1)

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDLDO}, V_{DDA}, $V_{DD33USB}$, V_{BAT})	−0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) +4.0(3)(4)	V
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	V
	Input voltage on BOOT0 pin	V_{SS}	9.0	V
	Input voltage on any other pins	V_{SS}-0.3	4.0	V
$\lvert\Delta V_{DDX}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 56* for the maximum allowed injected current values.
3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
4. To sustain a voltage higher than 4V the internal pull-up/pull-down resistors must be disabled.

Table 20. Current characteristics

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	620	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	620	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST and B pins except PA4, PA5	−5/+0	
	Injected current on PA4, PA5	−0/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by V_{IN}>V_{DD} while a negative injection is induced by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	– 65 to +150	°C
T_J	Maximum junction temperature	125	

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

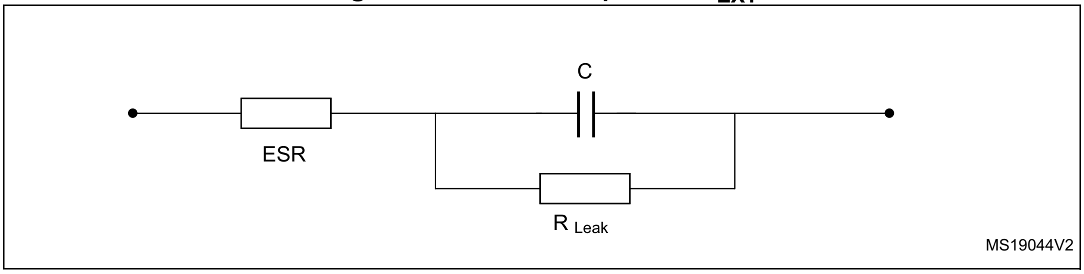
Symbol	Parameter		Operating conditions	Min	Max	Unit
V_{DD}	Standard operating voltage		-	1.62(1)	3.6	V
V_{DDLDO}	Supply voltage for the internal regulator		$V_{DDLDO} \leq V_{DD}$	1.62(1)	3.6	
$V_{DD33USB}$	Standard operating voltage, USB domain		USB used	3.0	3.6	
			USB not used	0	3.6	
V_{DDA}	Analog operating voltage		ADC or COMP used	1.62	3.6	
			DAC used	1.8		
			OPAMP used	2.0		
			VREFBUF used	1.8		
			ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{IN}	I/O Input voltage		TT_xx I/O	−0.3	V_{DD}+0.3	
			BOOT0	0	9	
			All I/O except BOOT0 and TT_xx	−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$)+3.6V < 5.5V(2)(3)	
P_D	Power dissipation at T_A = 85 °C for suffix 6(4)	TFBGA240+25	-	-	978	mW
		LQFP208	-	-	943	
		LQFP176	-	-	930	
		UFBGA176+25	-	-	1070	
		LQFP144	-	-	915	
		LQFP100	-	-	889	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(5)		–40	105	
T_J	Junction temperature range	Suffix 6 version		–40	125	°C

1. When RESET is released functionality is guaranteed down to V_{BOR0} min
2. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).

6.3.2 VCAP1/VCAP2/VCAP3 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP1/VCAP2/VCAP3 pins. C_{EXT} is specified in *Table 23*. Two external capacitors can be connected to VCAPx pins.

Figure 13. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 23. VCAP1/VCAP2/VCAP3 operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 100 mΩ

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

6.3.3 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 24. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	0	∞	
	V_{DDUSB} fall time rate	10	∞	

6.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 25* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 25. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after BOR0 released	-	-	377	-	µs
V_{BOR0}	Brown-out reset threshold 0	Rising edge(1)	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge in Run mode	2.69	2.76	2.83	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BOR (unless BOR0) and PVD	Hysteresis in Run mode	-	100	-	mV
$I_{DD\_BOR\_PVD}$(1)	BOR(2) (unless BOR0) and PVD consumption from V_{DD}	-	-		0.630	µA

Table 25. Reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVM_0}	Analog voltage detector for V_{DDA} threshold 0	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVM_1}	Analog voltage detector for V_{DDA} threshold 1	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVM_2}	Analog voltage detector for V_{DDA} threshold 2	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVM_3}	Analog voltage detector for V_{DDA} threshold 3	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{hyst_VDDA}	Hysteresis of V_{DDA} voltage detector	-	-	100	-	mV
I_{DD_PVM}	PVM consumption from $V_{DD(1)}$	-	-	-	0.25	µA
I_{DD_VDDA}	Voltage detector consumption on V_{DDA}(1)	Resistor bridge	-	-	2.5	µA

1. Guaranteed by design.
2. BOR0 is enabled in all modes (except Shutdown) and its consumption is therefore included in the supply current characteristics tables (refer to *Section 6.3.6: Supply current characteristics*).

6.3.5 Embedded reference voltage

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 26. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltages	-40°C < TJ < 105°C	1.180	1.216	1.255	V
$t_{S\_vrefint}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}(1)	VBAT sampling time when reading the internal VBAT reference voltage	-	9	-	-	
I_{refbuf}(2)	Reference Buffer consumption for ADC	V_{DDA}=3.3 V	9	13.5	23	µA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	-40°C < T_J < 105°C	-	5	15	mV
T_{coeff}	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$	Average Voltage coefficient	3.0V < V_{DD} < 3.6V	-	10	1370	ppm/V

Table 26. Embedded reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT_DIV1}	1/4 reference voltage	-	-	25	-	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage	-	-	50	-	
V_{REFINT_DIV3}	3/4 reference voltage	-	-	75	-	

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.

Table 27. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = 3.3 V	1FF1E860 - 1FF1E861

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 12: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{ACLK} frequency (refer to the table “Number of wait states according to CPU clock (ACLK) frequency and V_{CORE} range” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.

The parameters given in *Table 28* to *Table 36* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 28. Typical and maximum current consumption in Run mode, code with data processing running from ITCM, regulator ON(1)

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Typ	Max(2)			unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS1	400	71	110	210	290	mA
				300	56	-	-	-	
			VOS2	300	50	72	170	230	
				216	37	58	150	210	
				200	35.5	-	-	-	
			VOS3	200	33	50	130	190	
				180	30	47	130	180	
				168	28	45	130	180	
				144	25	41	120	180	
				60	13	28	110	160	
				25	10	24	99	160	
		All peripherals enabled	VOS1	400	165	220	400	500(3)	
				300	130	-	-	-	
			VOS2	300	120	170	300	390	
				200	83	-	-	-	
			VOS3	200	78	110	220	300	

1. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
2. Guaranteed by characterization results unless otherwise specified.
3. Guaranteed by test in production.

Table 29. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, cache ON, regulator ON

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Typ	Max[(1)] T_J = 25°C	Max[(1)] T_J = 85°C	Max[(1)] T_J = 105°C	unit
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS1	400	105	160	310	420	mA
				300	55	-	-	-	
			VOS2	300	50	72	160	230	
				216	38	-	-	-	
				200	36	-	-	-	
			VOS3	200	33	50	130	190	
				180	30	-	-	-	
				168	29	-	-	-	
				144	26	-	-	-	
				60	14	-	-	-	
				25	14	-	-	-	
		All peripherals enabled	VOS1	400	160	220	400	500[(2)]	
				300	130	-	-	-	
			VOS2	300	120	160	300	390	
				200	81	-	-	-	
			VOS3	200	77	110	220	300	

1. Guaranteed by characterization results unless otherwise specified.
2. Guaranteed by by test in production.

Table 30. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, cache OFF, regulator ON

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Typ	Max[(1)] T_J = 25°C	Max[(1)] T_J = 85°C	Max[(1)] T_J = 105°C	unit
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS1	400	73	110	220	290	mA
			VOS2	300	52	75	170	230	
			VOS3	200	34	52	130	190	
		All peripherals enabled	VOS1	400	135	190	360	470	
			VOS2	300	100	150	270	370	
			VOS3	200	70	100	210	300	

1. Guaranteed by characterization results.

Table 31. Typical consumption in Run mode and corresponding performance versus code position

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Coremark	Typ	Unit	IDD/ Coremark	Unit
		Peripheral	Code						
I_{DD}	Supply current in Run mode	All peripherals disabled, cache ON	ITCM	400	2012	71	mA	35	µA/ Coremark
			FLASH A	400	2012	105		52	
			AXI SRAM	400	2012	105		52	
			SRAM1	400	2012	105		52	
			SRAM4	400	2012	105		52	
		All peripherals disabled cache OFF	ITCM	400	2012	71		35	
			FLASH A	400	593	70.5		119	
			AXI SRAM	400	344	70.5		205	
			SRAM1	400	472	74.5		158	
			SRAM4	400	432	72		167	

Table 32. Typical current consumption batch acquisition mode

Symbol	Parameter	Conditions		$f_{rcc\_ahb\_ck(AHB4)}$ (MHz)	Typ	unit
I_{DD}	Supply current in batch acquisition mode	D1Standby, D2Standby, D3Run	VOS3	64	6.5	mA
		D1Stop, D2Stop, D3Run	VOS3	64	12	

Table 33. Typical and maximum current consumption in Sleep mode, regulator ON

Symbol	Parameter	Conditions		$f_{rcc\_c\_ck}$ (MHz)	Typ	Max[1]			unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	All peripherals disabled	VOS1	400	31.0	64	220	330	mA
				300	24.5	57	210	330	
			VOS2	300	22.0	48	180	270	
				200	17.0	42	170	270	
			VOS3	200	15.5	37	150	230	

1. Guaranteed by characterization results.

Table 34. Typical and maximum current consumption in Stop mode, regulator ON

Symbol	Parameter	Conditions		Typ	Max(1)			unit
					T_J = 25°C	T_J = 85°C	T_J = 105°C	
$I_{DD(Stop)}$	D1Stop, D2Stop, D3Stop	Flash memory OFF, no IWDG	SVOS5	1.4	7.2	49	75	mA
			SVOS4	1.95	11	66	110	
			SVOS3	2.85	16	91	150	
		Flash memory ON, no IWDG	SVOS5	1.65	7.2	49	75	
			SVOS4	2.2	11	66	110	
			SVOS3	3.15	16	91	150	
	D1Stop, D2Standby, D3Stop	Flash memory OFF, no IWDG	SVOS5	0.99	5.1	35	60	
			SVOS4	1.4	7.5	47	79	
			SVOS3	2.05	12	64	110	
		Flash memory ON, no IWDG	SVOS5	1.25	5.5	35	61	
			SVOS4	1.65	7.8	47	80	
			SVOS3	2.3	12	65	110	
	D1Standby, D2Stop, D3Stop	Flash OFF, no IWDG	SVOS5	0.57	3	21	36	
			SVOS4	0.805	4.5	27	47	
			SVOS3	1.2	6.7	37	63	
	D1Standby, D2Standby, D3Stop		SVOS5	0.17	1.1	8	13	
			SVOS4	0.245	1.5	11	17	
			SVOS3	0.405	2.4	15	23	

1. Guaranteed by characterization results.

Table 35. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions		Typ				Max (3 V)(1)			Unit
		Backup SRAM	RTC & LSE	1.62 V	2.4 V	3 V	3.3 V	T_J = 25°C	T_J = 85°C	T_J = 105°C	
I_{DD} (Standby)	Supply current in Standby mode	OFF	OFF	1.8	1.9	1.95	2.05	3	9.1	19	µA
		ON	OFF	3.4	3.4	3.5	3.7	6.8	27	64	
		OFF	ON	2	2.1	2.2	2.3	-	-	-	
		ON	ON	3.55	3.7	3.8	4.15	-	-	-	

1. Guaranteed by characterization results.

Table 36. Typical and maximum current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ				Max (3 V)[1]			Unit
		Backup SRAM	RTC & LSE	1.2 V	2 V	3 V	3.4 V	T_J = 25°C	T_J = 85°C	T_J = 105°C	
IDD (VBAT)	Supply current in standby mode	OFF	OFF	0.024	0.035	0.062	0.096	0.074	1.5	4.1	µA
		ON	OFF	1.4	1.6	1.8	1.8	3.2	19	42	
		OFF	ON	0.225	0.23	0.25	0.31	-	-	-	
		ON	ON	1.95	2.15	2.2	2.35	-	-	-	

1. Guaranteed by characterization results.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 57: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 37: Peripheral current consumption in Run mode*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- f_{ACLK} is the system clock. f_{PCLK} = f_{ACLK}/4, and f_{HCLK} = f_{ACLK}/2.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - f_{ACLK} = 400 MHz (Scale 1), f_{ACLK} = 300 MHz (Scale 2), f_{ACLK} = 200 MHz (Scale 3)
- The ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 37. Peripheral current consumption in Run mode

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
AHB3	MDMA	8.3	7.6	7	µA/MHz
	DMA2D	21	20	18	
	JPEG	24	23	21	
	FLASH	9.9	9	8.3	
	FMC registers	0.9	0.9	0.8	
	FMC kernel	6.1	5.5	5.3	
	QUADSPI registers	1.5	1.4	1.3	
	QUADSPI kernel	0.9	0.8	0.7	
	SDMMC1 registers	8	7.2	6.8	
	SDMMC1 kernel	2.4	2	1.8	
	DTCM1	5.7	5	4.5	
	DTCM2	5.5	4.8	4.3	
	ITCM	3.2	2.9	2.6	
	D1SRAM1	7.6	6.8	6.1	
	Bridge AHB3	7.5	6.8	6.3	
AHB1	DMA1	1.1	1	1	
	DMA2	1.7	1.4	1.1	
	ADC1/2 registers	3.9	3.2	3.1	
	ADC1/2 kernel	0.9	0.8	0.7	
	ART	5.5	4.5	4.2	
	ETH1MAC ETH1TX ETH1RX	16	14	13	
	USB1OTG registers	15	14	13	
	USB1OTG kernel	-	8.5	8.5	
	USB1ULPI	0.3	0.3	0.1	
	USB2OTG registers	15	13	12	
	USB2OTG kernel	-	8.6	8.6	
	USB2ULPI	16	16	16	
	Bridge AHB1	10	9.6	8.6	

Table 37. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
AHB2	DCMI	1.7	1.7	1.7	µA/MHz
	CRYP	0.1	0.1	0.1	
	HASH	0.1	0.1	0.1	
	RNG registers	1.8	1.4	1.2	
	RNG kernel	-	9.6	9.6	
	SDMMC2 registers	13	12	11	
	SDMMC2 kernel	2.7	2.5	2.4	
	D2SRAM1	3.3	3.1	2.8	
	D2SRAM2	2.9	2.7	2.5	
	D2SRAM3	1.9	1.8	1.7	
	Bridge AHB2	0.1	0.1	0.1	
AHB4	GPIOA	1.1	1	0.9	
	GPIOB	1	0.9	0.9	
	GPIOC	1.4	1.3	1.3	
	GPIOD	1.1	1	0.9	
	GPIOE	1	0.9	0.8	
	GPIOF	0.9	0.8	0.8	
	GPIOG	0.9	0.7	0.7	
	GPIOH	1	0.9	0.9	
	GPIOI	0.9	0.9	0.8	
	GPIOJ	0.9	0.8	0.8	
	GPIOK	0.9	0.8	0.7	
	CRC	0.5	0.4	0.4	
	BDMA	6.2	5.8	5.5	
	ADC3 registers	1.8	1.7	1.7	
	ADC3 kernel	0.1	0.1	0.1	
	Backup SRAM	1.9	1.8	1.8	
	Bridge AHB4	0.1	0.1	0.1	
APB3	LCD-TFT	12	11	10	µA/MHz
	WWDG1	0.5	0.4	0.3	
	Bridge APB3	0.5	0.2	0.1	

Table 37. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB1	TIM2	3.5	3.2	2.9	µA/MHz
	TIM3	3.4	3.1	2.7	
	TIM4	2.7	2.5	1.9	
	TIM5	3.2	2.9	2.5	
	TIM6	1	0.8	0.7	
	TIM7	1	0.9	0.7	
	TIM12	1.7	1.5	1.2	
	TIM13	1.5	1.3	1	
	TIM14	1.4	1.3	0.9	
	LPTIM1 registers	0.7	0.6	0.5	
	LPTIM1 kernel	2.3	2.1	1.9	
	WWDG2	0.6	0.4	0.4	
	SPI2 registers	1.8	1.5	1.2	
	SPI2 kernel	0.6	0.5	0.5	
	SPI3 registers	1.5	1.3	1.1	
	SPI3 kernel	0.6	0.5	0.5	
	SPDIFRX registers	0.6	0.5	0.3	
	SPDIFRX kernel	2.9	2.4	2.4	
	USART2 registers	1.4	1.3	1	
	USART2 kernel	4.7	4.1	4	
	USART3 registers	1.4	1.3	1	
	USART3 kernel	4.2	3.8	3.5	
	UART4 registers	1.5	1.1	1	
	UART4 kernel	3.7	3.6	3.2	

Table 37. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB1 (continued)	UART5 registers	1.4	1.4	1	µA/MHz
	UART5 kernel	3.6	3.2	3.1	
	I2C1 registers	0.8	0.8	0.6	
	I2C1 kernel	2	1.8	1.7	
	I2C2 registers	0.7	0.7	0.4	
	I2C2 kernel	1.9	1.7	1.6	
	I2C3 registers	0.9	0.7	0.6	
	I2C3 kernel	2.1	1.9	1.9	
	HDMI-CEC registers	0.5	0.3	0.3	
	DAC1/2	1.4	1.1	0.9	
	USART7 registers	1.9	1.8	1.3	
	USART7 kernel	4	3.5	3.3	
	USART8 registers	1.6	1.5	1.2	
	USART8 kernel	4	3.6	3.3	
	CRS	3.4	3.1	2.9	
	SWPMI registers	2.3	2	2	
	SWPMI kernel	0.1	0.1	0.1	
	OPAMP	0.5	0.4	0.4	
	MDIO	2.7	2.4	2.3	
	FDCAN registers	16	15	14	
	FDCAN kernel	7.8	7.6	7.1	
	Bridge APB1	0.1	0.1	0.1	

Table 37. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB2	TIM1	5.1	4.8	4.3	µA/MHz
	TIM8	5.4	4.9	4.6	
	USART1 registers	2.7	2.6	2.5	
	USART1 kernel	0.1	0.1	0.1	
	USART6 registers	2.6	2.5	2.5	
	USART6 kernel	0.1	0.1	0.1	
	SPI1 registers	1.8	1.6	1.6	
	SPI1 kernel	1	0.8	0.6	
	SPI4 registers	1.6	1.5	1.5	
	SPI4 kernel	0.5	0.4	0.4	
	TIM15	3.1	2.8	2.7	
	TIM16	2.4	2.1	2.1	
	TIM17	2.2	2	1.9	
	SPI5 registers	1.8	1.7	1.7	
	SPI5 kernel	0.6	0.5	0.3	
	SAI1 registers	1.5	1.4	1.4	
	SAI1 kernel	2	1.7	1.5	
	SAI2 registers	1.5	1.5	1.3	
	SAI2 kernel	2.2	1.9	1.8	
	SAI3 registers	1.8	1.6	1.6	
	SAI3 kernel	2.5	2.3	2.1	
	DFSDM1 registers	6	5.4	5.2	
	DFSDM1 kernel	0.9	0.8	0.7	
	HRTIM	40	37	35	
	Bridge APB2	0.1	0.1	0.1	

Table 37. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB4	SYSCFG	1	0.7	0.7	µA/MHz
	LPUART1 registers	1.1	1.1	1.1	
	LPUART1 kernel	2.6	2.4	2.1	
	SPI6 registers	1.6	1.5	1.4	
	SPI6 kernel	0.2	0.2	0.2	
	I2C4 registers	0.1	0.1	0.1	
	I2C4 kernel	2.4	2.1	2	
	LPTIM2 registers	0.5	0.5	0.5	
	LPTIM2 kernel	2.3	2.1	1.8	
	LPTIM3 registers	0.5	0.5	0.5	
	LPTIM3 kernel	2	2.1	1.5	
	LPTIM4 registers	0.5	0.5	0.5	
	LPTIM4 kernel	2	2	1.9	
	LPTIM5 registers	0.5	0.5	0.5	
	LPTIM5 kernel	2	1.8	1.5	
	COMP1/2	0.7	0.5	0.5	
	VREFBUF	0.6	0.4	0.4	
	RTC	1.2	1.1	1.1	
	SAI4 registers	1.6	1.5	1.4	
	SAI4 kernel	1.3	1.3	1.2	
	Bridge APB4	0.1	0.1	0.1	

Table 38. Peripheral current consumption in Stop, Standby and VBAT mode

Symbol	Parameter	Conditions	Typ	Unit
			3 V	
I_{DD}	RTC+LSE low drive	-	2.32	µA
	RTC+LSE medium-low drive	-	2.4	
	RTC+LSE medium-high drive	-	2.7	
	RTC+LSE High drive	-	3	

6.3.7 Wakeup time from low-power modes

The wakeup times given in Table 39 are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PC1) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 39. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	9	10	CPU clock cycles
t_{WUSTOP}(2)	Wakeup from Stop	VOS3, HSI, Flash memory in normal mode	4.4	5.6	µs
		VOS3, HSI, Flash memory in low-power mode	12	15	
		VOS4, HSI, Flash memory in normal mode	15	20	
		VOS4, HSI, Flash memory in low-power mode	23	28	
		VOS5, HSI, Flash memory in normal mode	30	71	
		VOS5, HSI, Flash memory in low-power mode	38	47	
		VOS3, CSI, Flash memory in normal mode	27	37	
		VOS3, CSI, Flash memory in low power mode	36	50	
		VOS4, CSI, Flash memory in normal mode	38	48	
		VOS4, CSI, Flash memory in low-power mode	47	61	
		VOS5, CSI, Flash memory in normal mode	52	64	
		VOS5, CSI, Flash memory in low-power mode	62	77	
$t_{WUSTOP2}$(2)	Wakeup from Stop, clock kept running	VOS3, HSI, Flash memory in normal mode	2.6	3.4	
		VOS3, CSI, Flash memory in normal mode	26	36	
$t_{WUSTDBY}$(2)	Wakeup from Standby mode	-	390	500	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

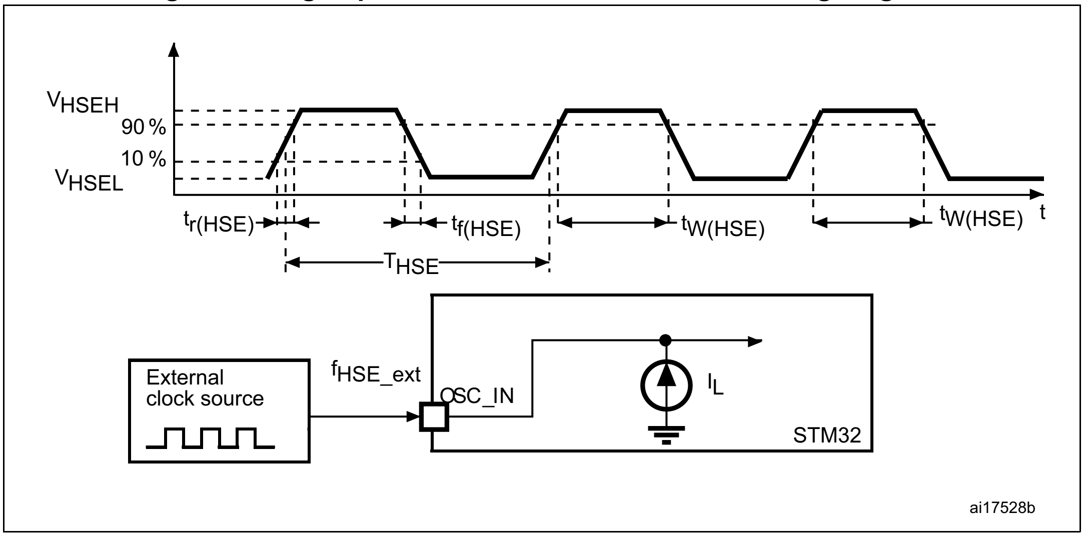
The external clock signal has to respect the *Table 57: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 14*.

Table 40. High-speed external user clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	4	25	50	MHz
V_{SW} ($V_{HSEH} - V_{HSEL}$)	OSC_IN amplitude	$0.7V_{DD}$	-	V_{DD}	V
V_{DC}	OSC_IN input voltage	V_{SS}	-	$0.3V_{SS}$	V
$t_{W(HSE)}$	OSC_IN high or low time	7	-	-	ns

1. Guaranteed by design.

Figure 14. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 57: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 15*.

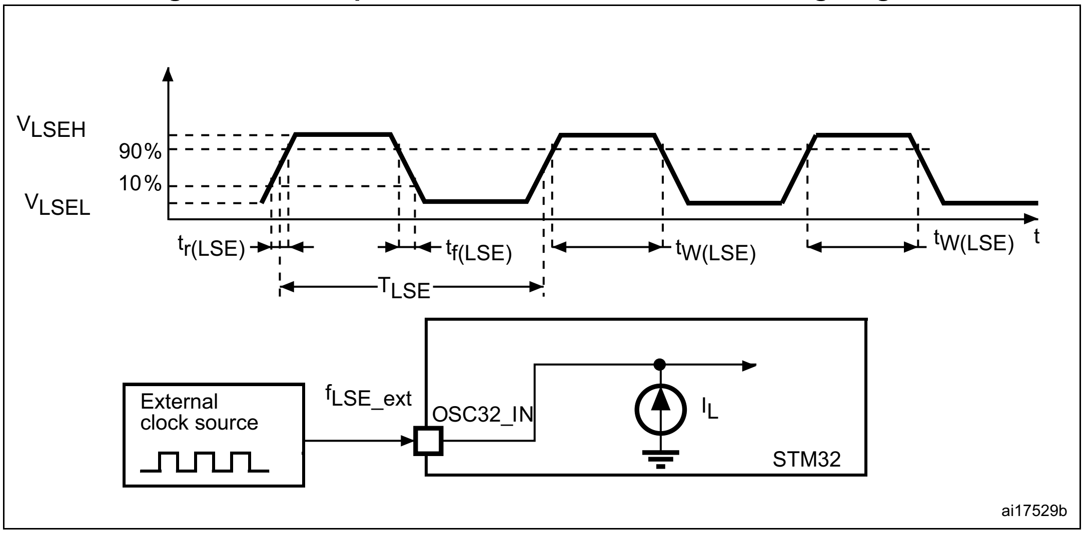
Table 41. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 15. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 42. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 42. 4-48 MHz HSE oscillator characteristics(1)

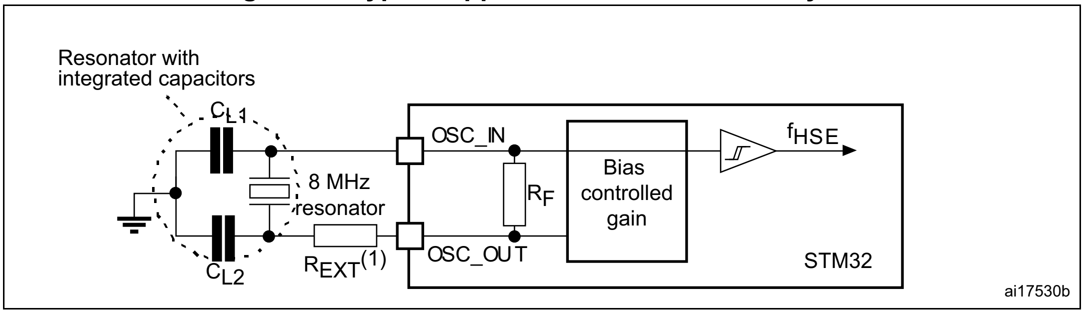
Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	4	mA
		V_{DD}=3 V, Rm=30 Ω C_L=10pF@4MHz	-	0.35	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 8 MHz	-	0.40	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 16 MHz	-	0.45	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 32 MHz	-	0.65	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 48 MHz	-	0.95	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t_{SU}(4)	Start-up time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 16). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

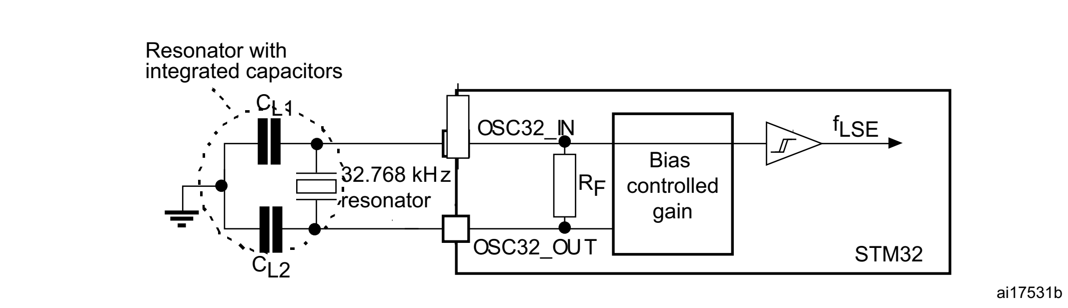
Table 43. Low-speed external user clock characteristics(1)

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	290	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	390	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	550	-	
		LSEDRV[1:0] = 11, High drive capability	-	900	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	VDD is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers.
3. t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 17. Typical application with a 32.768 kHz crystal



1. *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

6.3.9 Internal clock source characteristics

The parameters given in *Table 44* and *Table 47* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

48 MHz high-speed internal RC oscillator (HSI48)

Table 44. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD}=3.3 V, TJ=30 °C	-	48	-	MHz
TRIM(1)	USER trimming step	-	-	0.17	-	%
USER TRIM COVERAGE(2)	USER TRIMMING Coverage	± 32 steps	-	±5.45	-	%
DuCy(HSI48)(1)	Duty Cycle	-	-	50	-	%
ACCHSI48_REL(2)	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD}=1.62 to 3.6 V, T_J=-40 to 105 °C	–5	-	4	%
DVDD(HSI48)(2)	HSI48 oscillator frequency drift with V_{DD}(3)	V_{DD}=3 to 3.6 V	-	0.025	0.05	%
		V_{DD}=1.62 V to 3.6 V	-	0.05	0.1	
$t_{su(HSI48)}$(1)	HSI48 oscillator start-up time	-	-	2.1	3.5	µs
$I_{DD(HSI48)}$(1)	HSI48 oscillator power consumption	-	-	350	400	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	± 0.15	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	± 0.25	-	ns

1. Guaranteed by design.
2. Guaranteed by characterization.
3. These values are obtained by using the formula:
(Freq(3.6V) - Freq(3.0V)) / Freq(3.0V) or (Freq(3.6V) - Freq(1.62V)) / Freq(1.62V).
4. Jitter measurements are performed without clock source activated in parallel.

64 MHz high-speed internal RC oscillator (HSI)

Table 45. HSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	V_{DD}=3.3 V, T_J=30 °C	-	64	-	MHz
TRIM	HSI user trimming step	Trimming is not a multiple of 32	-	0.24	0.32	%
		Trimming is 128, 256 and 384	−5.2	−1.8	-	
		Trimming is 64, 192, 320 and 448	−1.4	−0.8	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)	−0.6	−0.25	-	
DuCy(HSI)	Duty Cycle	-	45	-	55	%
$\Delta_{VDD\ (HSI)}$	HSI oscillator frequency drift over V_{DD} (reference is 3.3 V)	V_{DD}=1.62 to 3.6 V	−0.12	-	0.03	%
$\Delta_{TEMP\ (HSI)}$	HSI oscillator frequency drift over temperature (reference is 64 MHz)	T_J=-20 to 105 °C	−1[2]	-	1[2]	%
		T_J=−40 to $T_J$max °C	−2[2]		1[2]	
t_{su}(HSI)	HSI oscillator start-up time	-	-	1.4	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1% of target frequency	-	3	5	µs
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by characterization.

4 MHz low-power internal RC oscillator (CSI)

Table 46. CSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}	CSI frequency	V_{DD}=3.3 V, T_J=30 °C	3.96[2]	4	4.04[2]	MHz
TRIM	Trimming step	-	-	0.35	-	%
DuCy(CSI)	Duty Cycle	-	45	-	55	%
Δ_{VDD} (CSI) + Δ_{TEMP} (CSI)	CSI oscillator frequency drift over V_{DD} & drift over temperature	V_{DD}=1.62 to 3.6 V T_J = 0 to 85 °C	-	±1[3]	-	%
$t_{su(CSI)}$	CSI oscillator startup time	-	-	1	-	µs
$t_{stab(CSI)}$	CSI oscillator stabilization time (to reach ±3% of f_{CSI})	-	-	-	4	cycle
$I_{DD(CSI)}$	CSI oscillator power consumption	-	-	23	30	µA

1. Guaranteed by design.
2. Guaranteed by test in production.
3. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 47. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.3 V, T_J = 25 °C (after calibration)	31.4	32	32.6	kHz
		T_J = –40 to 105 °C, V_{DD} = 1.62 to 3.6 V	29.76	-	33.60	
$t_{su(LSI)}$[1]	LSI oscillator startup time	-	-	80	130	µs
$t_{stab(LSI)}$[1]	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
$I_{DD(LSI)}$[1]	LSI oscillator power consumption	-	-	130	280	nA

1. Guaranteed by design.

6.3.10 PLL characteristics

The parameters given in *Table 48* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 48. Main PLL characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	2	-	16	MHz
	PLL input clock duty cycle	-	10	-	90	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling range 1	1.5	-	400[2]	MHz
		Voltage scaling range 2	1.5	-	300	
		Voltage scaling range 3	1.5	-	200	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q/R	Voltage scaling range 1	1.5	-	400[2]	
		Voltage scaling range 2	1.5	-	300	
		Voltage scaling range 3	1.5	-	200	
f_{VCO_OUT}	PLL VCO output	-	192	-	836	
t_{LOCK}	PLL lock time	Normal mode	-	50[3]	150[3]	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)	-	58[3]	166[3]	

Table 48. Main PLL characteristics[1] (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter	Cycle-to-cycle jitter	VCO = 192 MHz		-	134	-	±ps
		VCO = 200 MHz		-	134	-	
		VCO = 400 MHz		-	76	-	
		VCO = 800 MHz		-	39	-	
	Long term jitter	Normal mode		-	±0.7	-	%
		Sigma-delta mode (CKIN = 16 MHz)		-	±0.8	-	
$I_{DD(PLL)}$[3]	PLL power consumption on V_{DD}	VCO freq = 836 MHz	V_{DDA}	-	590	1500	µA
			V_{CORE}	-	720	-	
		VCO freq = 192 MHz	V_{DDA}	-	180	600	
			V_{CORE}	-	280	-	

1. Guaranteed by design unless otherwise specified.
2. Due to product limitation to 400 MHz.
3. Guaranteed by characterization results.

6.3.11 Memory characteristics

Flash memory

The characteristics are given at T_J = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 49. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode	-	6.5	-	mA
		Write / Erase 16-bit mode	-	11.5	-	
		Write / Erase 32-bit mode	-	20	-	
		Write / Erase 64-bit mode	-	35	-	

Table 50. Flash memory programming (single bank configuration nDBANK=1)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word (266 bits) programming time	Program/erase parallelism x 8	-	290	580(2)	µs
		Program/erase parallelism x 16	-	180	360	
		Program/erase parallelism x 32	-	130	260	
		Program/erase parallelism x 64	-	100	200	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism x 8	-	2	4	s
		Program/erase parallelism x 16	-	1.8	3.6	
		Program/erase parallelism x 32	-			
t_{ME}	Mass erase time	Program/erase parallelism x 8	-	13	26	
		Program/erase parallelism x 16	-	8	16	
		Program/erase parallelism x 32	-	6	12	
		Program/erase parallelism x 64	-	5	10	
V_{prog}	Programming voltage	Program parallelism x 8	1.62	-	3.6	V
		Program parallelism x 16				
		Program parallelism x 32				
		Program parallelism x 64	1.8	-	3.6	

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10K erase operations.

Table 51. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value Min(1)	Unit
N_{END}	Endurance	T_J = –40 to +125 °C (6 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 85 °C	30	Years
		10 kcycles at T_A = 55 °C	20	

1. Guaranteed by characterization results.

6.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 52*. They are based on the EMS levels and classes defined in application note AN1709.

Table 52. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, UFBGA240, $f_{rcc\_c\_ck}$ = 400 MHz, conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance		4B

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 53. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/400 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, UFBGA240 package, conforming to IEC61967-2	0.1 to 30 MHz	6	dBµV
			30 to 130 MHz	5	
			130 MHz to 1 GHz	13	
			1 GHz to 2 GHz	7	
			EMI Level	2.5	-

6.3.13 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 54. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	All	1C	1000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All	C1	250	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 55. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_A = +25 °C conforming to JESD78	II level A

6.3.14 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 56. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	PA7, PC5, PG1, PB14, PJ7, PA11, PA12, PA13, PA14, PA15, PJ12, PB4	5	0	mA
	PA2, PH2, PH3, PE8, PA6, PA7, PC4, PE7, PE10, PE11	0	NA	
	PA0, PA_C, PA1, PA1_C, PC2, PC2_C, PC3, PC3_C, PA4, PA5, PH4, PH5, BOOT0	0	0	
	All other I/Os	5	NA	

1. Guaranteed by characterization.

6.3.15 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 57: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 22: General operating conditions*. All I/Os are CMOS and TTL compliant (except for BOOT0).

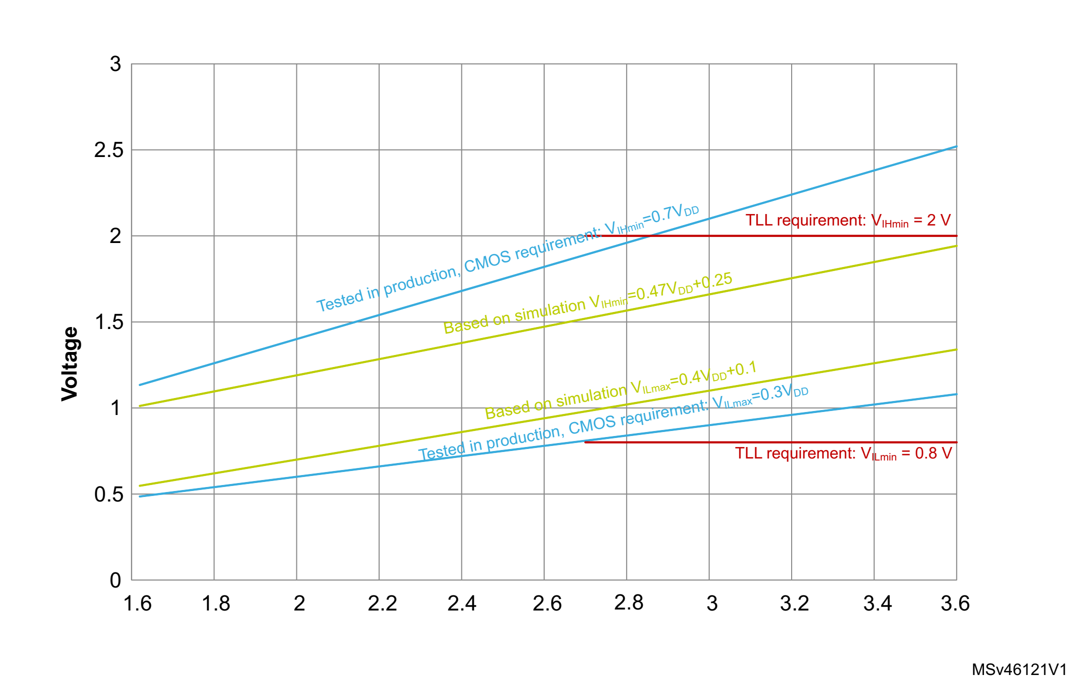
Table 57. I/O static characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage except BOOT0	1.62 V<V_{DD}<3.6 V	-	-	0.3xV_{DD}	V
	I/O input low level voltage except BOOT0		-	-	0.4xV_{DD}− 0.1	
	BOOT0 I/O input low level voltage		-	-	0.19xV_{DD} +0.1	
V_{IH}(1)	I/O input high level voltage except BOOT0	1.62 V<V_{DD}<3.6 V	0.7xV_{DD}	-	-	V
	I/O input low level voltage except BOOT0		0.47xV_{DD}+ 0.25	-	-	
	BOOT0 I/O input high level voltage		0.17xV_{DD}+ 0.6	-	-	
V_{HYS}(1)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V< V_{DD} <3.6 V	-	250	-	mV
	BOOT0 I/O input hysteresis		-	200	-	
R_{PU}	Weak pull-up equivalent resistor(2)	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(2)	V_{IN}=V_{DD}(3)	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by design.
2. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).
3. Max(VDDXXX) is the maximum value of all the I/O supplies.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 18*.

Figure 18. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 20*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 20*).

Output voltage levels

Unless otherwise specified, the parameters given in Table 58 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 22: General operating conditions. All I/Os are CMOS and TTL compliant.

Table 58. Output voltage characteristics(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V		0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO}=-8 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4		
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V		0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO}=-8 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4		
V_{OL}(3)	Output low level voltage	I_{IO}=20 mA 2.7 V≤ V_{DD} ≤3.6 V		1.3	
V_{OH}(3)	Output high level voltage	I_{IO}=-20 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−1.3		
V_{OL}(3)	Output low level voltage	I_{IO}=4 mA 1.62 V≤ V_{DD} ≤3.6 V		0.4	
V_{OH} (3)	Output high level voltage	I_{IO}=-4 mA 1.62 V≤V_{DD}<3.6 V	V_{DD}–-0.4		
V_{OLFM+}(3)	Output low level voltage for an FTf IO pin in FM+ mode	I_{IO}= 20 mA 2.3 V≤ V_{DD}≤3.6 V	-	0.4	
		I_{IO}= 10 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 19: Voltage characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of SYSCFG_CCCSR register can be used to optimize the I/O speed when the product voltage is below 2.5 V.

Table 59. Output timing characteristics (HSLV OFF)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	12	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	12	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	16	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	4	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	16.6	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	33.3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	13.3	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
01	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	60	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	80	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	110	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	5.2	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.2	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	7.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	2.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	5.2	

Table 59. Output timing characteristics (HSLV OFF)[1] (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}[2]	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	85	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	35	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	110	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	40	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	166	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	100	
	t_r/t_f[3]	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	3.8	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	6.9	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	2.8	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	5.2	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	1.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	3.3	
11	F_{max}[2]	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	100	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	50	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	133	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	66	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	220	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	85	
	t_r/t_f[3]	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	3.3	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	6.6	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	2.4	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	4.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	1.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V[4]	-	2.7	

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions:
   $(t_r+t_f) \leq 2/3$ T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Output buffer timing characteristics (HSLV option enabled)

Table 60. Output timing characteristics (HSLV ON)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	11	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	9	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	
01	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	50	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	58	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	66	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	4.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
10	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	55	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	80	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	133	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.8	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	4	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	2.4	
11	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	60	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	90	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	175	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.3	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	3.6	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	1.9	

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions:
   $(t_r+t_f) \leq 2/3$ T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 57: I/O static characteristics*).

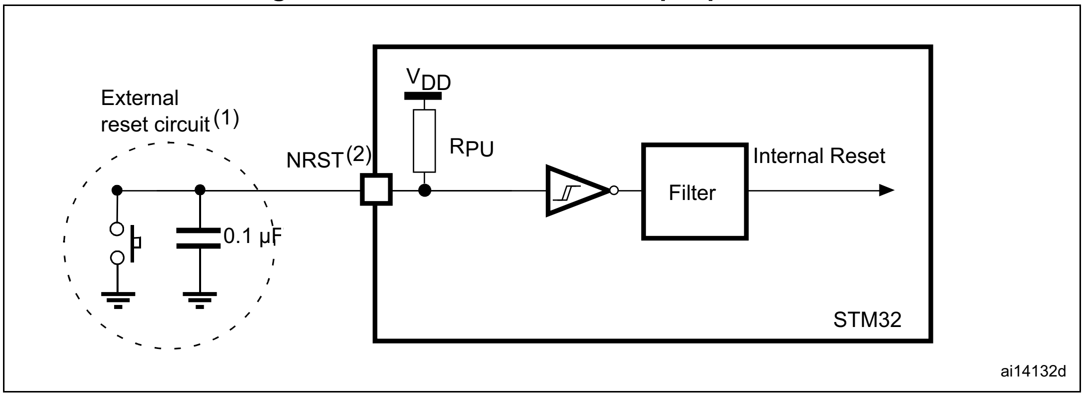
Unless otherwise specified, the parameters given in *Table 61* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 61. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	$1.71\ V < V_{DD} < 3.6\ V$	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	$1.71\ V < V_{DD} < 3.6\ V$	300	-	-	ns
		$1.62\ V < V_{DD} < 3.6\ V$	1000	-	-	ns

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 19. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 61*. Otherwise the reset is not taken into account by the device.

6.3.17 FMC characteristics

Unless otherwise specified, the parameters given in *Table 62* to *Table 75* for the FMC interface are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

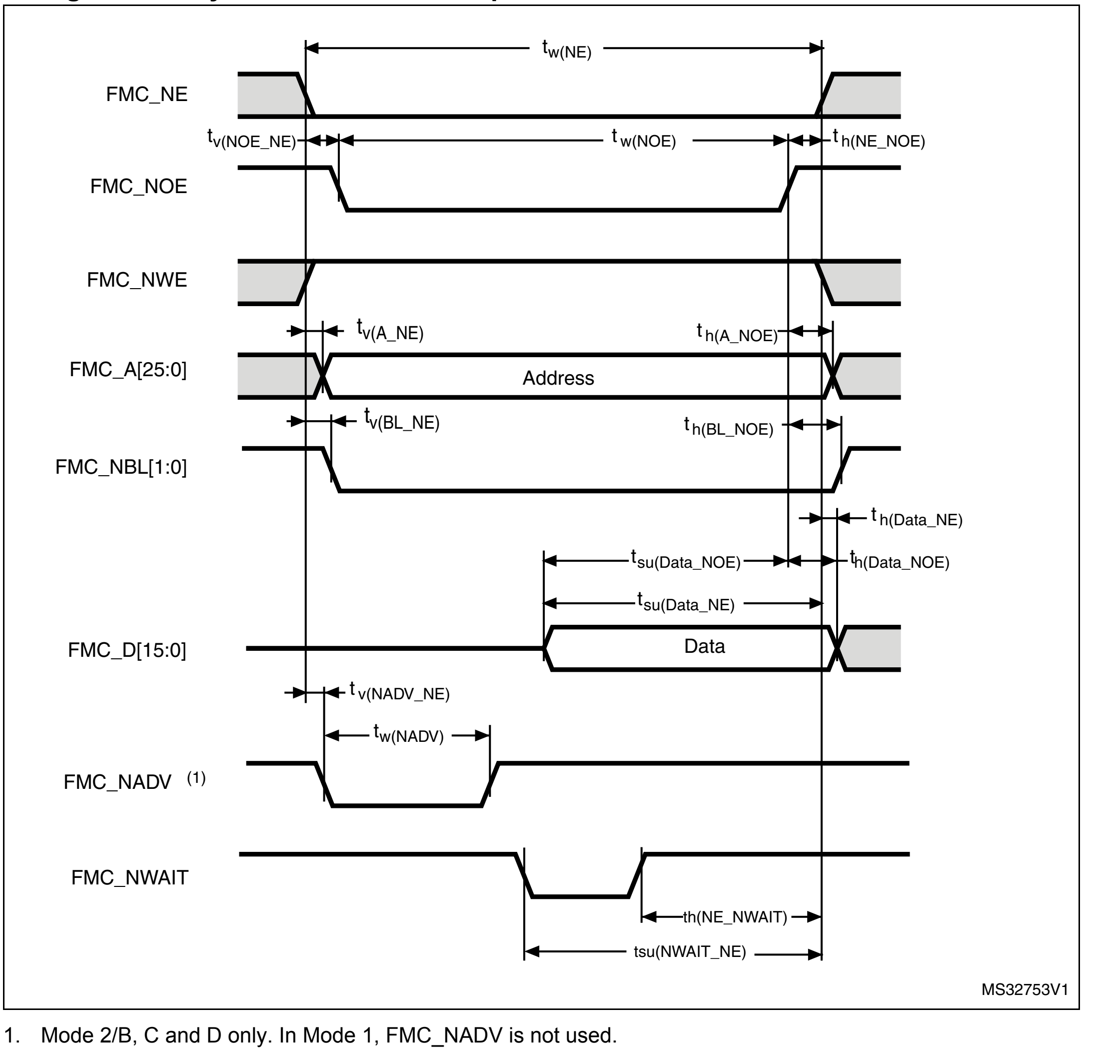
Asynchronous waveforms and timings

Figure 20 through *Figure 23* represent asynchronous waveforms and *Table 62* through *Table 69* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capcitive load CL = 30 pF

In all timing tables, the T_{KERCK} is the fmc_ker_ck clock period.

Figure 20. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 62. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{fmc\_ker\_ck} - 1$	$2\ T_{fmc\_ker\_ck} + 1$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	11	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	11	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck} + 1$	

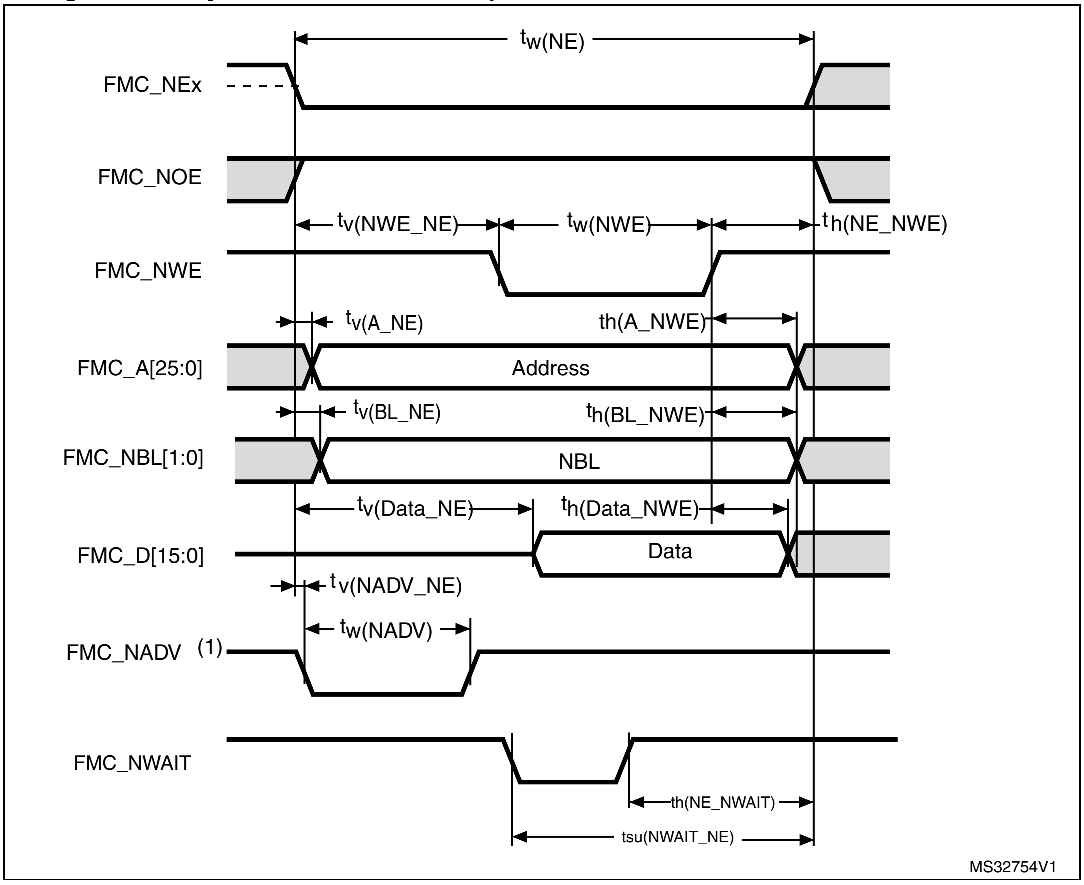
1. Guaranteed by characterization results.

Table 63. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{fmc\_ker\_ck} + 1$	$7T_{fmc\_ker\_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc\_ker\_ck} - 1$	$5T_{fmc\_ker\_ck} + 1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc\_ker\_ck} - 0.5$		
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc\_ker\_ck} + 11$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3T_{fmc\_ker\_ck} + 11.5$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 64. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc\_ker\_ck} - 1$	$3T_{fmc\_ker\_ck}$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_ck}$	$T_{fmc\_ker\_ck} + 1$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc\_ker\_ck} - 0.5$	$T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck}$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{fmc\_ker\_ck} + 2.5$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc\_ker\_ck}+0.5$	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck} + 1$	

1. Guaranteed by characterization results.

Table 65. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc\_ker\_ck} - 1$	$8T_{fmc\_ker\_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc\_ker\_ck} - 1.5$	$6T_{fmc\_ker\_ck} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc\_ker\_ck} + 13$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck} + 13$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 22. Asynchronous multiplexed PSRAM/NOR read waveforms

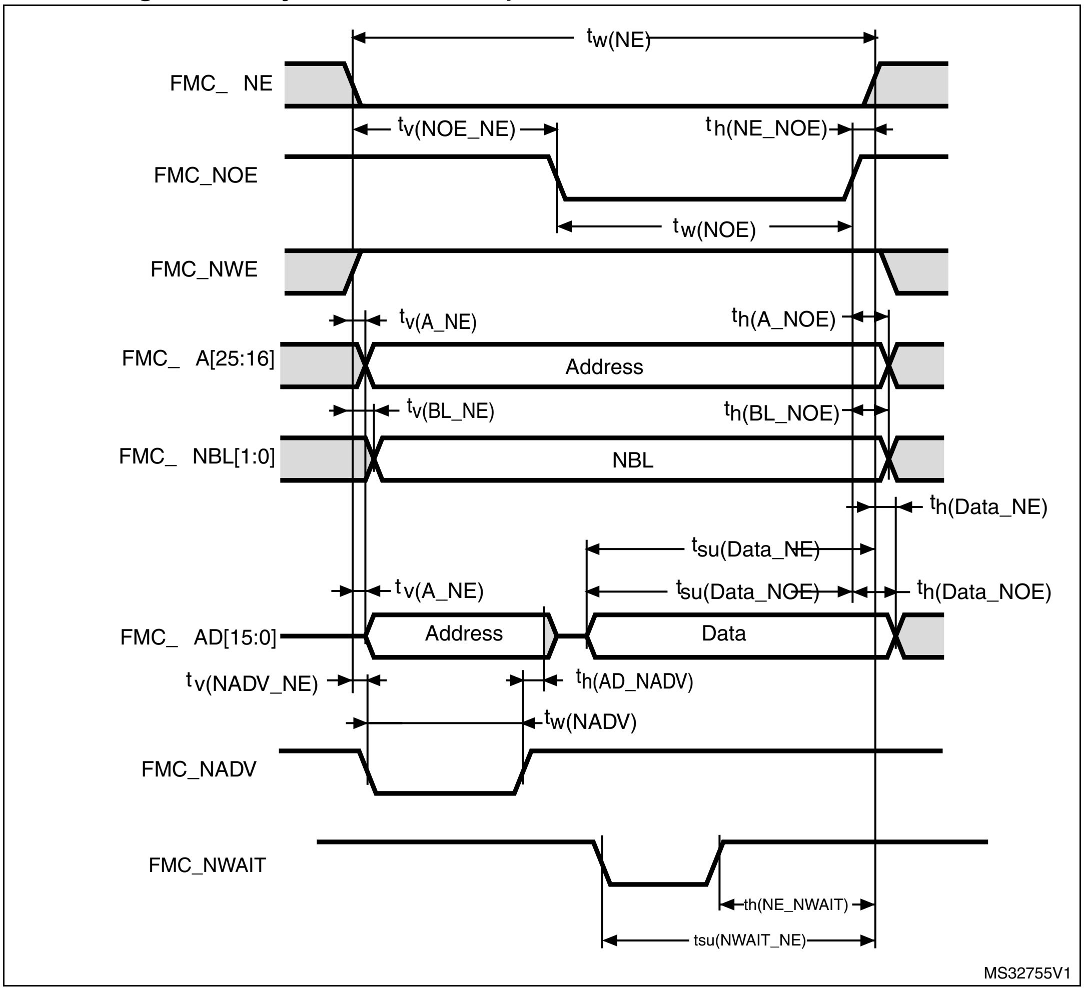


Table 66. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc\_ker\_ck} - 1$	$3T_{fmc\_ker\_ck} + 1$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc\_ker\_ck}$	$2T_{fmc\_ker\_ck} + 0.5$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc\_ker\_ck} - 1$	$T_{fmc\_ker\_ck} + 1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck} - 0.5$	$T_{fmc\_ker\_ck}+1$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{h(BL\_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{fmc\_ker\_ck} - 2$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	$T_{fmc\_ker\_ck} - 2$	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results.

Table 67. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc\_ker\_ck} - 1$	$8T_{fmc\_ker\_ck}$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc\_ker\_ck} - 1.5$	$5T_{fmc\_ker\_ck} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc\_ker\_ck} + 3$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck}$	-	

1. Guaranteed by characterization results.

Figure 23. Asynchronous multiplexed PSRAM/NOR write waveforms

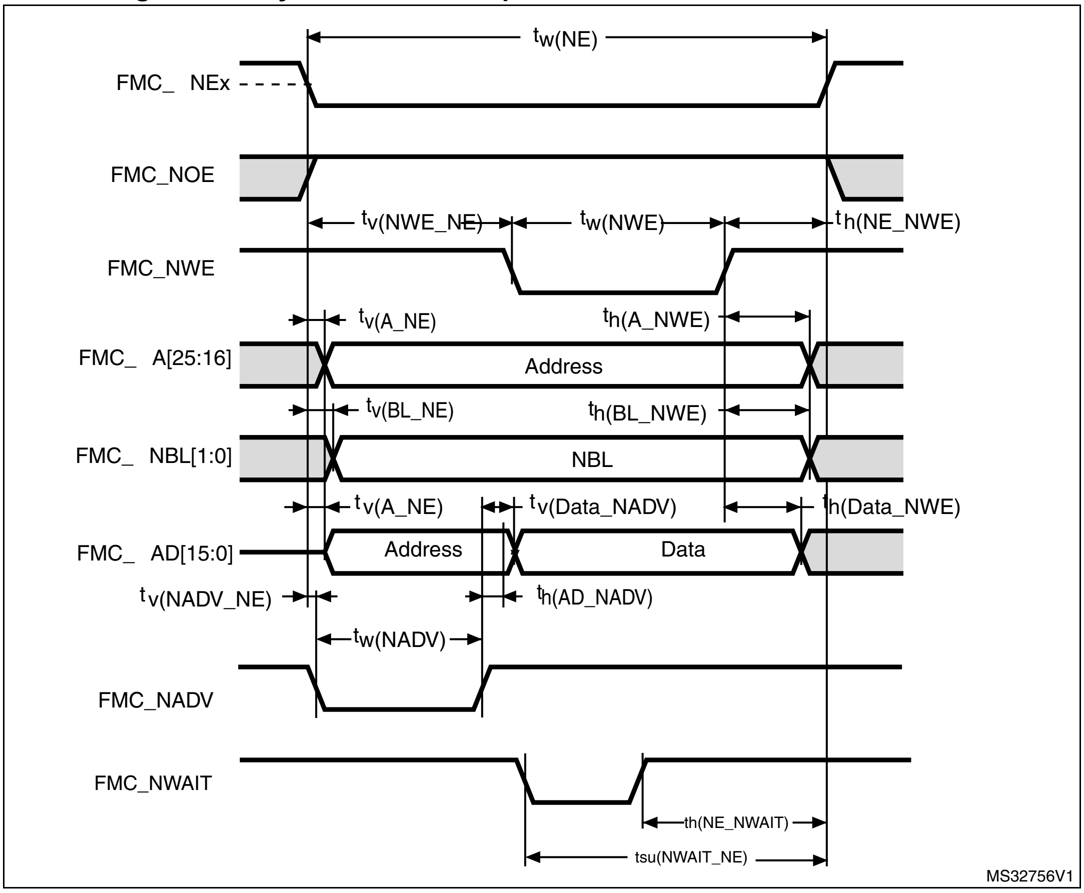


Table 68. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_c} - 1$	$4T_{fmc\_ker\_ck}$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_c} - 1$	$T_{fmc\_ker\_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc\_ker\_ck} - 0.5$	$2T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck}$	$T_{fmc\_ker\_ck} + 1$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc\_ker\_ck} + 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc\_ker\_ck} + 0.5$	-	

1. Guaranteed by characterization results.

Table 69. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc\_ker\_ck} - 1$	$9T_{fmc\_ker\_ck}$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc\_ker\_ck} - 0.5$	$7T_{fmc\_ker\_ck} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{fmc\_ker\_ck} + 3$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck}$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 24 through *Figure 27* represent synchronous waveforms and *Table 70* through *Table 73* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period, with the following FMC_CLK maximum values:

- For 2.7 V<V_{DD}<3.6 V, FMC_CLK =133 MHz at 20 pF
- For 1.8 V<V_{DD}<1.9 V, FMC_CLK =100 MHz at 20 pF
- For 1.62 V<V_{DD}<1.8 V, FMC_CLK =100 MHz at 15 pF

Figure 24. Synchronous multiplexed NOR/PSRAM read timings

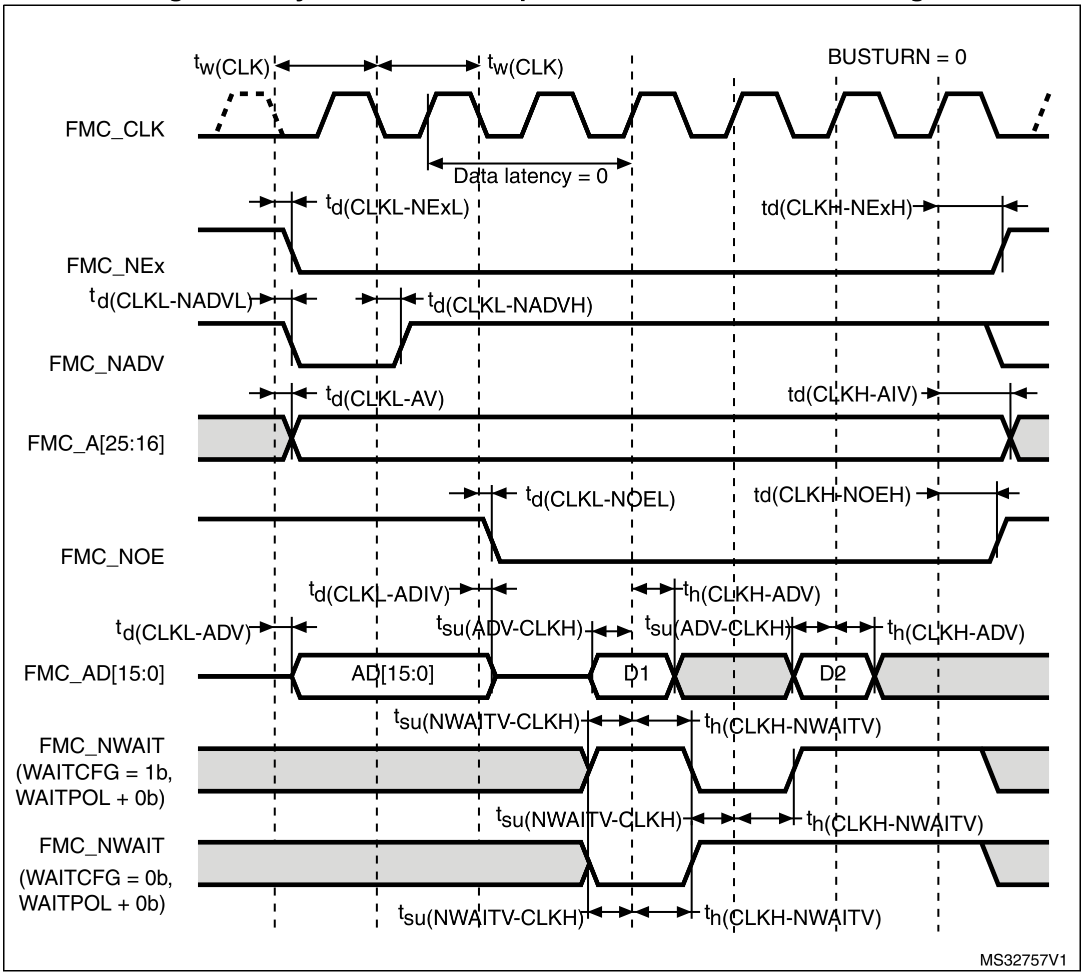


Table 70. Synchronous multiplexed NOR/PSRAM read timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Figure 25. Synchronous multiplexed PSRAM write timings

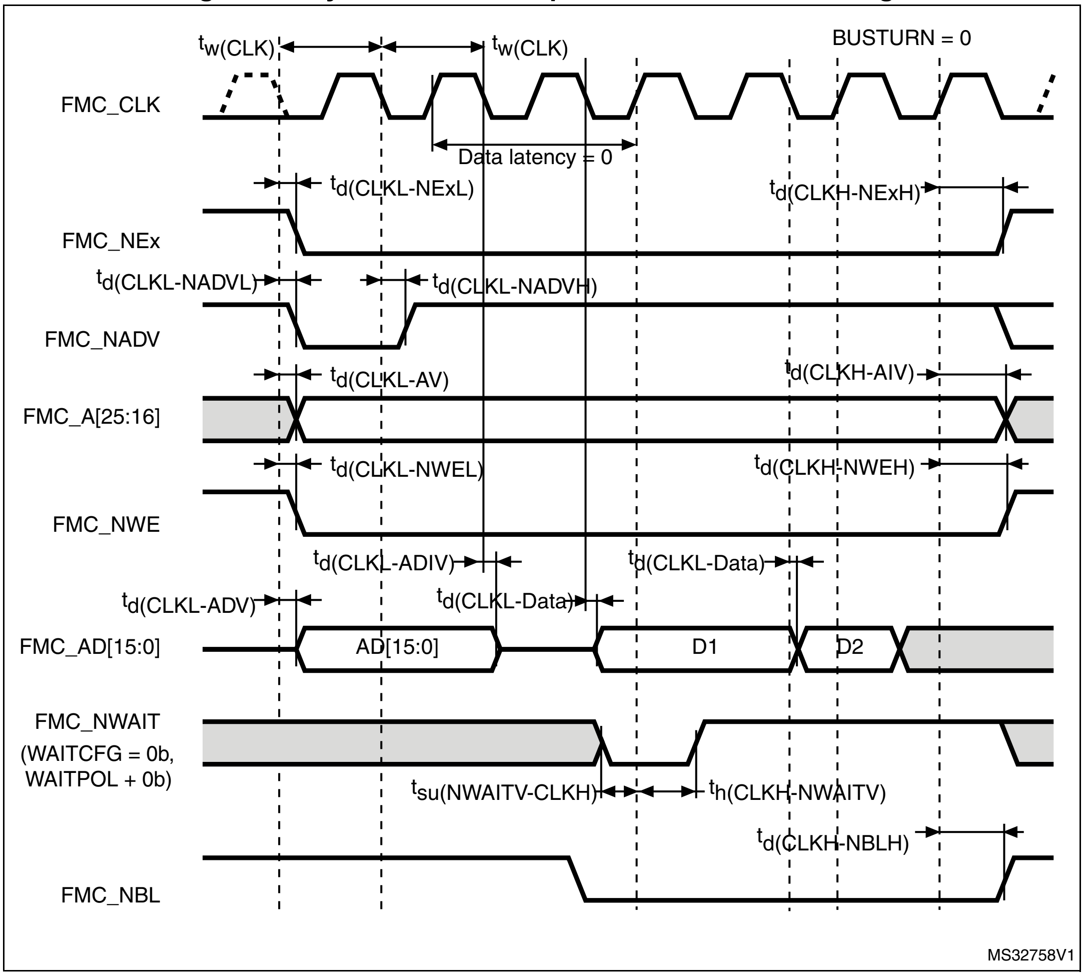


Table 71. Synchronous multiplexed PSRAM write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	2.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Figure 26. Synchronous non-multiplexed NOR/PSRAM read timings

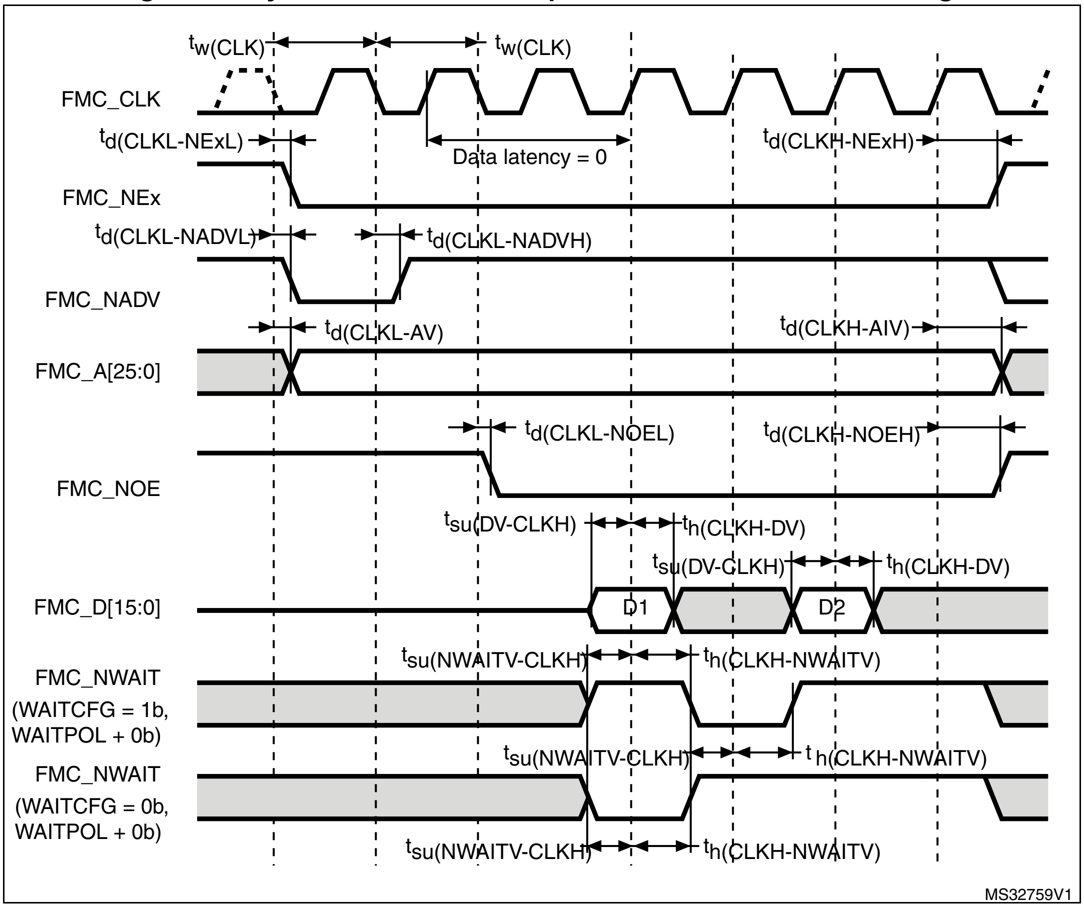


Table 72. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	1	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Figure 27. Synchronous non-multiplexed PSRAM write timings

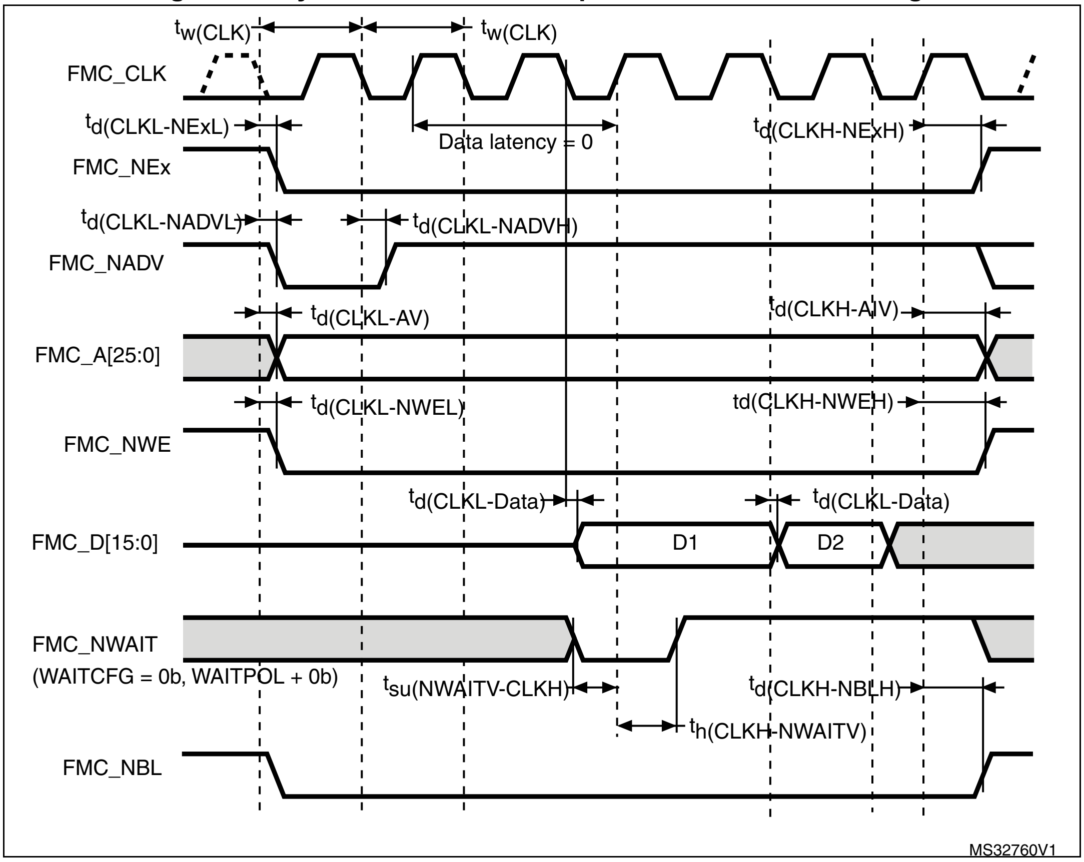


Table 73. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc\_ker\_ck} + 1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc\_ker\_ck} + 1$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 28 through *Figure 31* represent synchronous waveforms, and *Table 74* and *Table 75* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- C_L = 30 pF

In all timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period.

Figure 28. NAND controller waveforms for read access

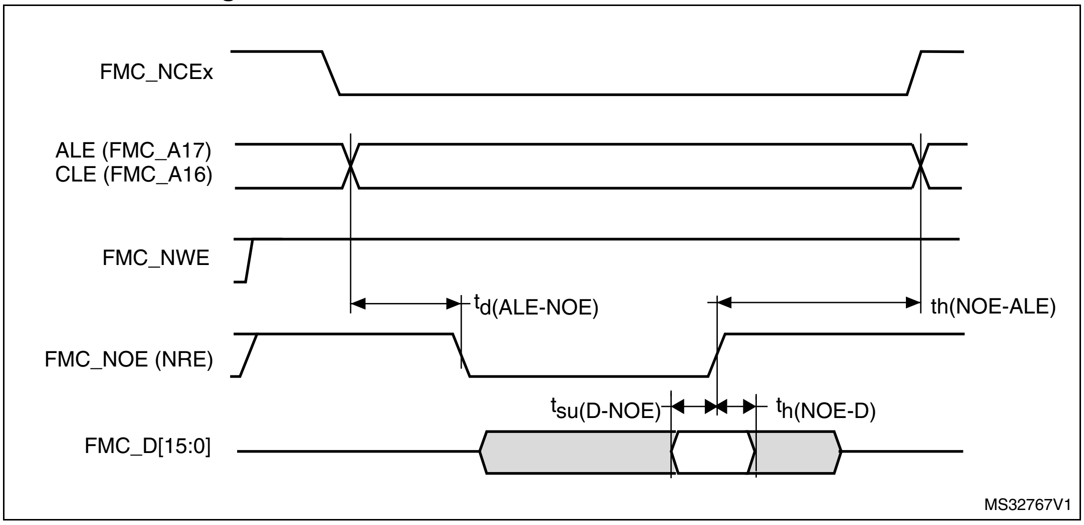


Figure 29. NAND controller waveforms for write access

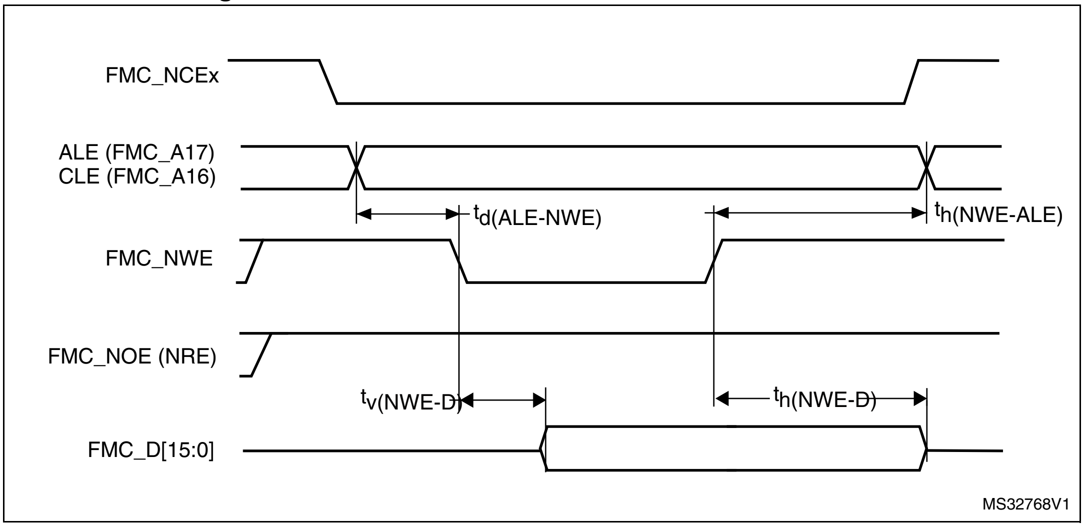


Figure 30. NAND controller waveforms for common memory read access

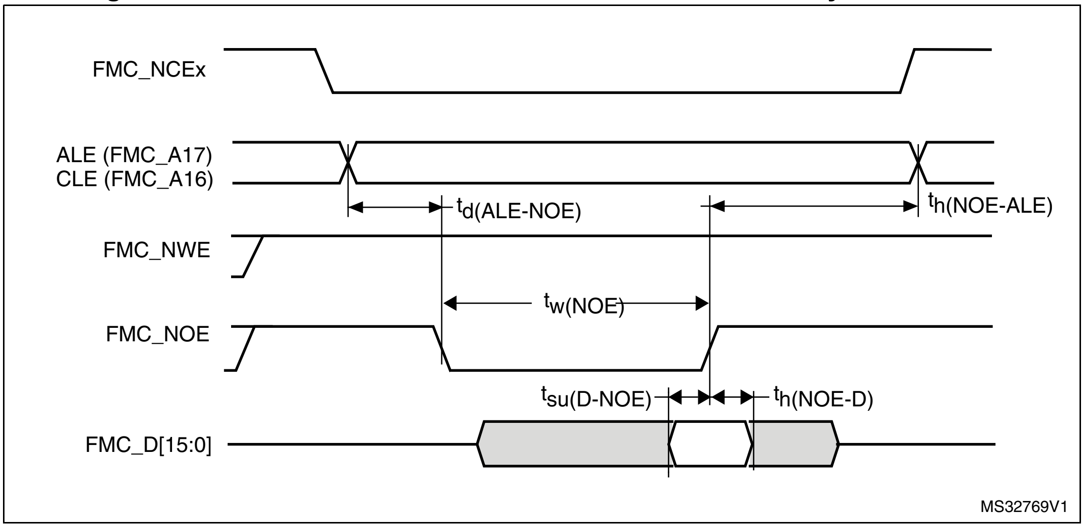


Figure 31. NAND controller waveforms for common memory write access

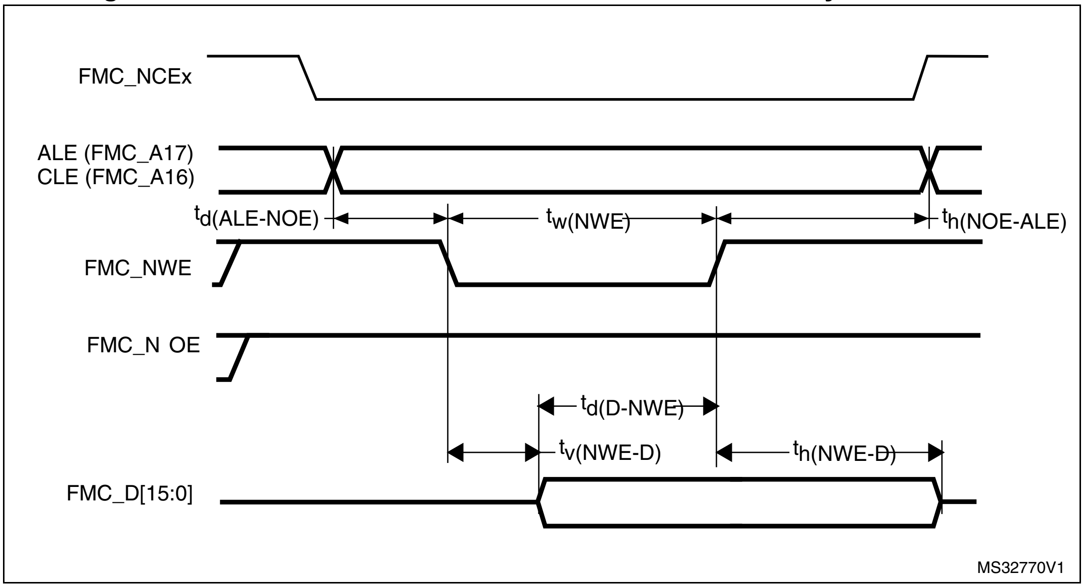


Table 74. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	8	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc\_ker\_ck} + 1$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc\_ker\_ck} - 2$	-	

1. Guaranteed by characterization results.

Table 75. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck} + 0.5$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc\_ker\_ck} - 0.5$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc\_ker\_ck} - 1$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc\_ker\_ck} - 1$	-	

1. Guaranteed by characterization results.

SDRAM waveforms and timings

In all timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period, with the following FMC_CLK maximum values:

- For 1.8 V<V_{DD}<3.6V: FMC_CLK =100 MHz at 20 pF
- For 1.62 V<$_{DD}$<1.8 V, FMC_CLK =100 MHz at 30 pF

Figure 32. SDRAM read access waveforms (CL = 1)

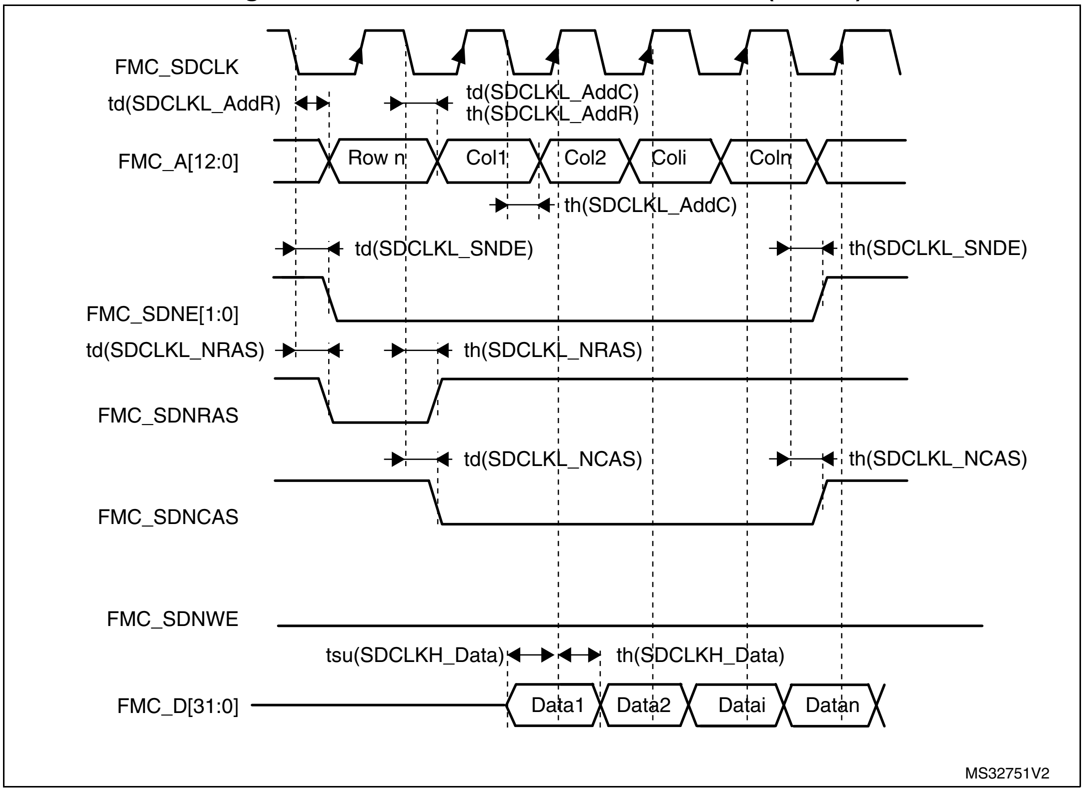


Table 76. SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	1	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL- SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 77. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	1.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	2.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Figure 33. SDRAM write access waveforms

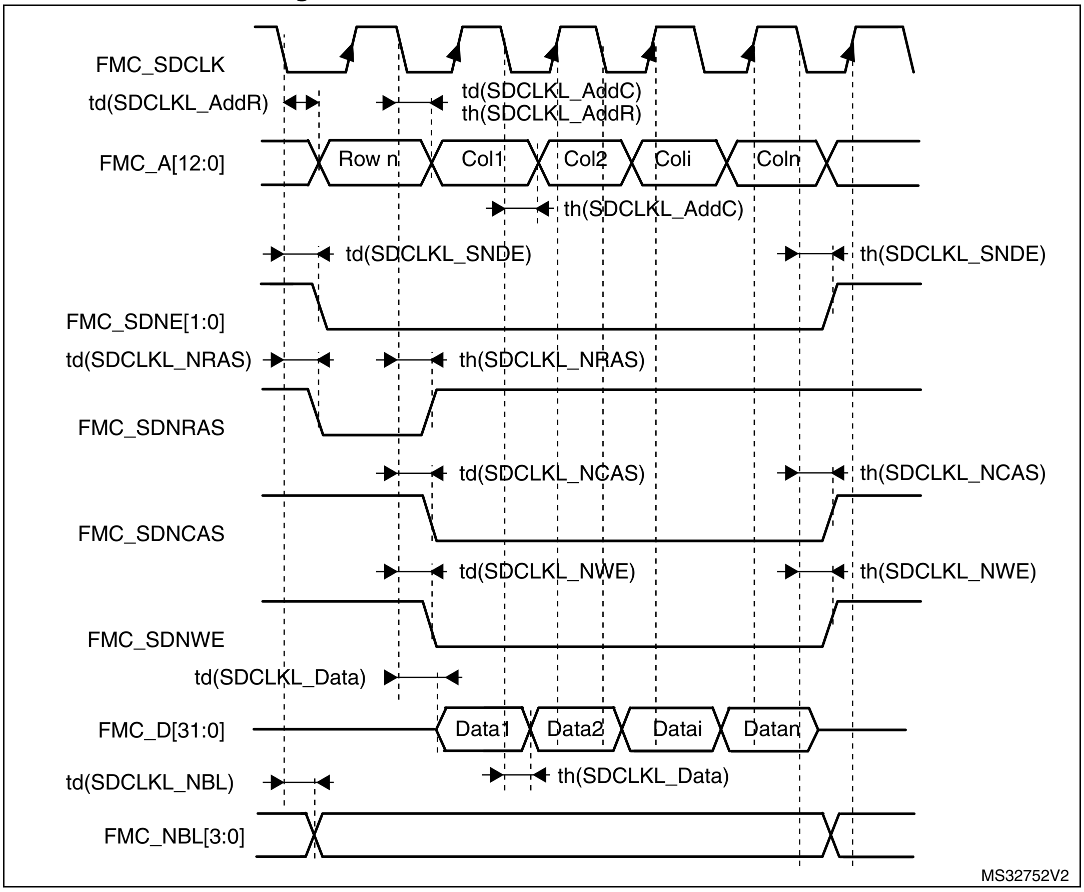


Table 78. SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 0.5$	ns
$t_{d(SDCLKL\_Data)}$	Data output valid time	-	3	
$t_{h(SDCLKL\_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL\_SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL\_SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL-\_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.

Table 79. LPSDR SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 0.5$	ns
$t_{d(SDCLKL\_Data)}$	Data output valid time	-	2.5	
$t_{h(SDCLKL\_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	2.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	3	
$t_{h(SDCLKL-SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

6.3.18 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 80* and *Table 81* for Quad-SPI are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 80. Quad-SPI characteristics in SDR mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1/t(CK)}$	Quad-SPI clock frequency	$2.7\text{ V} \leq V_{DD} < 3.6\text{ V}$ C_L=20 pF	-	-	133	MHz
		$1.62\text{ V} < V_{DD} < 3.6\text{ V}$ C_L=15 pF	-	-	100	
$t_{w(CKH)}$	Quad-SPI clock high and low time	-	$t_{(CK)}/2$ -0.5	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2 + 0.5$	
$t_{s(IN)}$	Data input setup time	-	1.5	-	-	
$t_{h(IN)}$	Data input hold time		2	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1.5	2	
$t_{h(OUT)}$	Data output hold time	-	0.5	-	-	

Table 81. Quad SPI characteristics in DDR mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1/t(CK)}$	Quad-SPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	100	MHz
		1.62 V<V_{DD}<3.6 V CL=15 pF	-	-	100	
$t_{w(CKH)}$	Quad-SPI clock high and low time	-	$t_{(CK)}/2$ - 0.5	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2$+0.5	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	-	2	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	-	2	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	DHHC=0	-	3.5	4	
		DHHC=1 Pres=1, 2...	-	$t_{(CK)}/4$+3.5	$t_{(CK)}/4$+4	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	DHHC=0	3	-	-	
		DHHC=1 Pres=1, 2...	$t_{(CK)}/4$+3	-	-	

Figure 34. Quad-SPI timing diagram - SDR mode

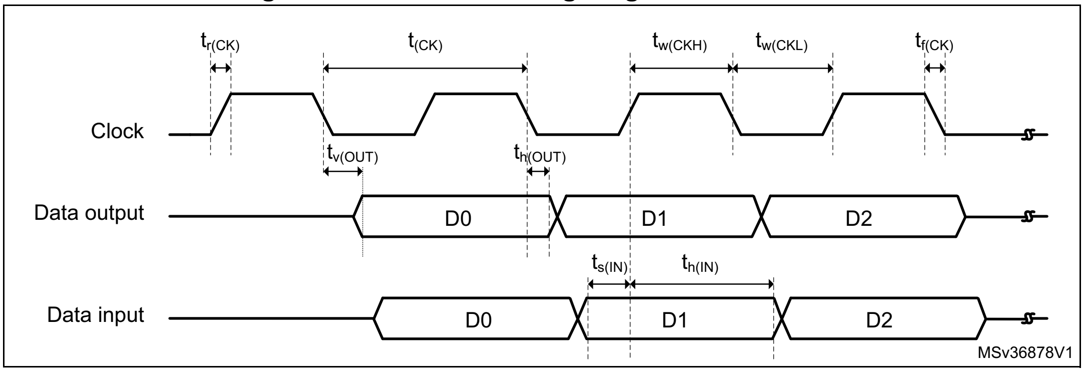
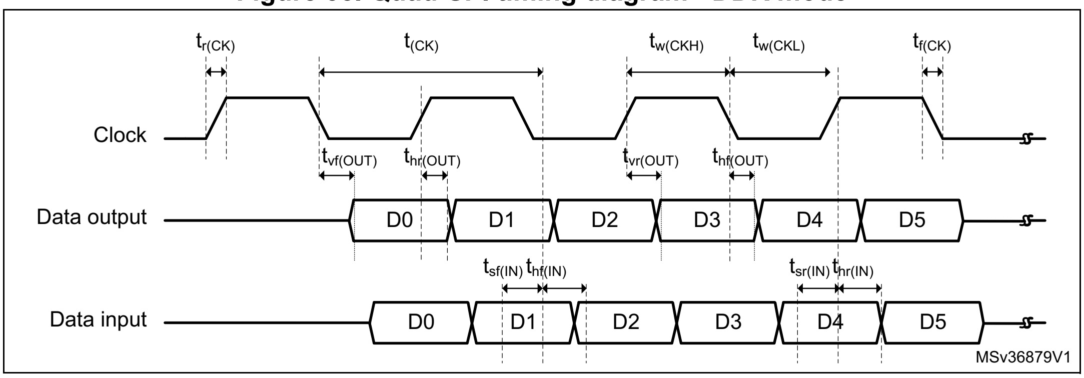


Figure 35. Quad-SPI timing diagram - DDR mode



6.3.19 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 83* for the delay block are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage summarized in *Table 22: General operating conditions*.

Table 82. Dynamics characteristics: Delay Block characteristics

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>t_{init}</td><td>Initial delay</td><td>-</td><td>1400</td><td>2200</td><td>2400</td><td rowspan="2">ps</td></tr>
<tr><td>t_{Δ}</td><td>Unit Delay</td><td>-</td><td>35</td><td>40</td><td>45</td></tr>
</table>

6.3.20 16-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 83* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 83. ADC characteristics(1)

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>V_{DDA}</td><td>Analog power supply</td><td colspan="2">-</td><td>1.62</td><td>-</td><td>3.6</td><td rowspan="4">V</td></tr>
<tr><td rowspan="2">V_{REF+}</td><td rowspan="2">Positive reference voltage</td><td colspan="2">$V_{DDA} \geq 2$ V</td><td>2</td><td>-</td><td>V_{DDA}</td></tr>
<tr><td colspan="2">$V_{DDA} < 2$ V</td><td colspan="3">V_{DDA}</td></tr>
<tr><td>V_{REF-}</td><td>Negative reference voltage</td><td colspan="2">-</td><td colspan="3">V_{SSA}</td></tr>
<tr><td rowspan="2">f_{ADC}</td><td rowspan="2">ADC clock frequency</td><td rowspan="2">$2\text{ V} \leq V_{DDA} \leq 3.3\text{ V}$</td><td>BOOST = 1</td><td>-</td><td>-</td><td>36</td><td rowspan="2">MHz</td></tr>
<tr><td>BOOST = 0</td><td>-</td><td>-</td><td>20</td></tr>
<tr><td rowspan="15">f_S</td><td rowspan="5">Sampling rate for Fast channels, BOOST = 1, f_{ADC} = 36 MHz</td><td colspan="2">16-bit resolution</td><td>-</td><td>-</td><td>3.60</td><td rowspan="15">MSPS</td></tr>
<tr><td colspan="2">14-bit resolution</td><td>-</td><td>-</td><td>4.00</td></tr>
<tr><td colspan="2">12-bit resolution</td><td>-</td><td>-</td><td>4.50</td></tr>
<tr><td colspan="2">10-bit resolution</td><td>-</td><td>-</td><td>5.00</td></tr>
<tr><td colspan="2">8-bit resolution</td><td></td><td></td><td>6.00</td></tr>
<tr><td rowspan="5">Sampling rate for Fast channels, BOOST = 0, f_{ADC} = 20 MHz</td><td colspan="2">16-bit resolution</td><td>-</td><td>-</td><td>2.00</td></tr>
<tr><td colspan="2">14-bit resolution</td><td>-</td><td>-</td><td>2.20</td></tr>
<tr><td colspan="2">12-bit resolution</td><td>-</td><td>-</td><td>2.50</td></tr>
<tr><td colspan="2">10-bit resolution</td><td>-</td><td>-</td><td>2.80</td></tr>
<tr><td colspan="2">8-bit resolution</td><td></td><td></td><td>3.30</td></tr>
<tr><td rowspan="5">Sampling rate for Fast channels, BOOST = 0, f_{ADC} = 10 MHz</td><td colspan="2">16-bit resolution</td><td>-</td><td>-</td><td>1.00</td></tr>
<tr><td colspan="2">14-bit resolution</td><td>-</td><td>-</td><td>1.00</td></tr>
<tr><td colspan="2">12-bit resolution</td><td>-</td><td>-</td><td>1.00</td></tr>
<tr><td colspan="2">10-bit resolution</td><td>-</td><td>-</td><td>1.00</td></tr>
<tr><td colspan="2">8-bit resolution</td><td></td><td></td><td>1.00</td></tr>
</table>

Table 83. ADC characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG}	External trigger frequency	f_{ADC} = 36 MHz	-	-	3.6	MHz
		16-bit resolution	-	-	10	$1/f_{ADC}$
V_{AIN}[2]	Conversion voltage range	-	0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-	$V_{REF}/2-10\%$	$V_{REF}/2$	$V_{REF}/2+10\%$	
R_{AIN}	External input impedance	See *Equation 1* for details	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	4	-	pF
t_{ADCREG_STUP}	ADC LDO startup time	-	-	5	10	µs
t_{STAB}	ADC power-up time	LDO already started	1			conversion cycle
t_{CAL}	Offset and linearity calibration time	-	16384			$1/f_{ADC}$
t_{OFF_CAL}	Offset calibration time	-	1280			
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	
		CKMODE = 01	-	-	2	
		CKMODE = 10			2.25	
		CKMODE = 11			2.125	
$t_{LATRINJ}$	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	-	-	0.067	
		CKMODE = 01	2.5	3	3.5	
		CKMODE = 10	-	-	3	
		CKMODE = 11	-	-	3.25	
		CKMODE = 00	-	-	3.125	
t_S	Sampling time	-	1.5	-	640.5	
t_{CONV}	Total conversion time (including sampling time)	N-bit resolution	t_S + 0.5 + N/2 (9 to 648 cycles in 14-bit mode)			

1. Guaranteed by design.
2. Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} to V_{SSA}.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution).

Table 84. ADC accuracy(1)(2)(3)

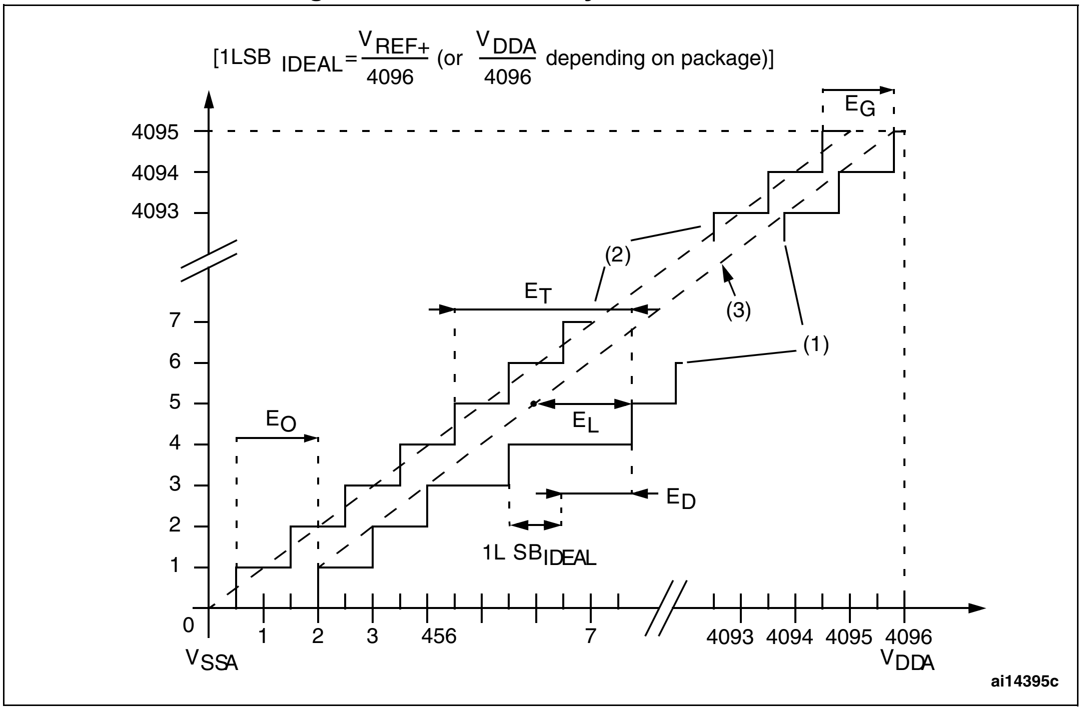
Symbol	Parameter	Conditions(4)		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	BOOST = 1	-	±6	-	±LSB
			BOOST = 0	-	±8	-	
		Differential	BOOST = 1	-	±10	-	
			BOOST = 0	-	±16	-	
ED	Differential linearity error	Single ended	BOOST = 1	-	2	-	
			BOOST = 0	-	1	-	
		Differential	BOOST = 1	-	8	-	
			BOOST = 0	-	2	-	
EL	Integral linearity error	Single ended	BOOST = 1	-	±6	-	
			BOOST = 0	-	±4	-	
		Differential	BOOST = 1	-	±6	-	
			BOOST = 0	-	±4	-	
ENOB(5)	Effective number of bits (2 MSPS)	Single ended	BOOST = 1	-	11.6	-	bits
			BOOST = 0	-	12	-	
		Differential	BOOST = 1	-	13.3	-	
			BOOST = 0	-	13.5	-	
SINAD(5)	Signal-to-noise and distortion ratio (2 MSPS)	Single ended	BOOST = 1	-	71.6	-	dB
			BOOST = 0	-	74	-	
		Differential	BOOST = 1	-	81.83	-	
			BOOST = 0	-	83	-	
SNR(5)	Signal-to-noise ratio (2 MSPS)	Single ended	BOOST = 1	-	72	-	
			BOOST = 0	-	74	-	
		Differential	BOOST = 1	-	82	-	
			BOOST = 0	-	83	-	
THD(5)	Total harmonic distortion	Single ended	BOOST = 1	-	−78	-	
		Single ended	BOOST = 0	-	−80	-	
			BOOST = 1	-	−90	-	
		Differential	BOOST = 0	-	−95	-	

1. Guaranteed by characterization for BGA packages, the values for LQFP packages might differ.
2. ADC DC accuracy values are measured after internal calibration.
3. The above table gives the ADC performance in 16-bit mode.
4. ADC clock frequency ≤ 36 MHz, 2 V ≤ V_{DDA} ≤3.3 V, 1.6 V ≤ V_{REF} ≤ V_{DDA}, BOOSTEN (for I/O) = 1.
5. ENOB, SINAD, SNR and THD are specified for V_{DDA} = V_{REF} = 3.3 V.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

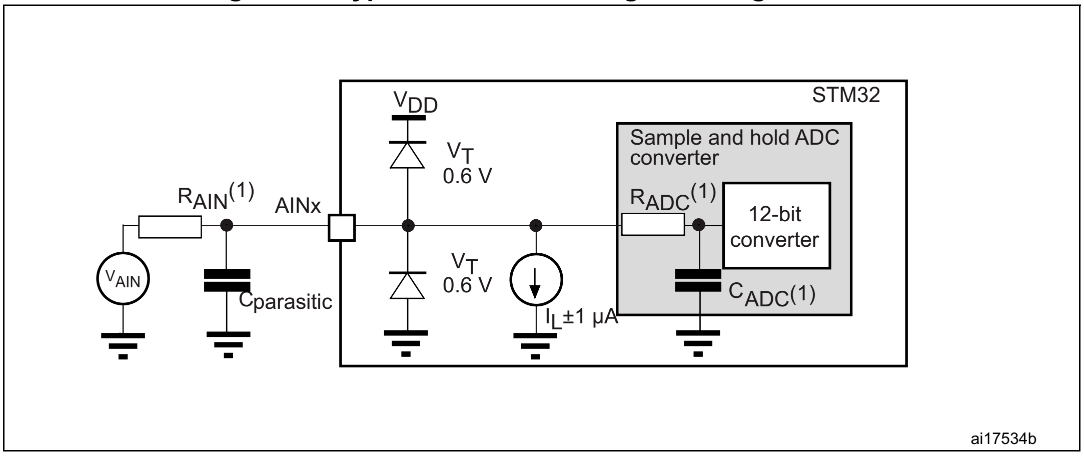
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.15* does not affect the ADC accuracy.

Figure 36. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 37. Typical connection diagram using the ADC

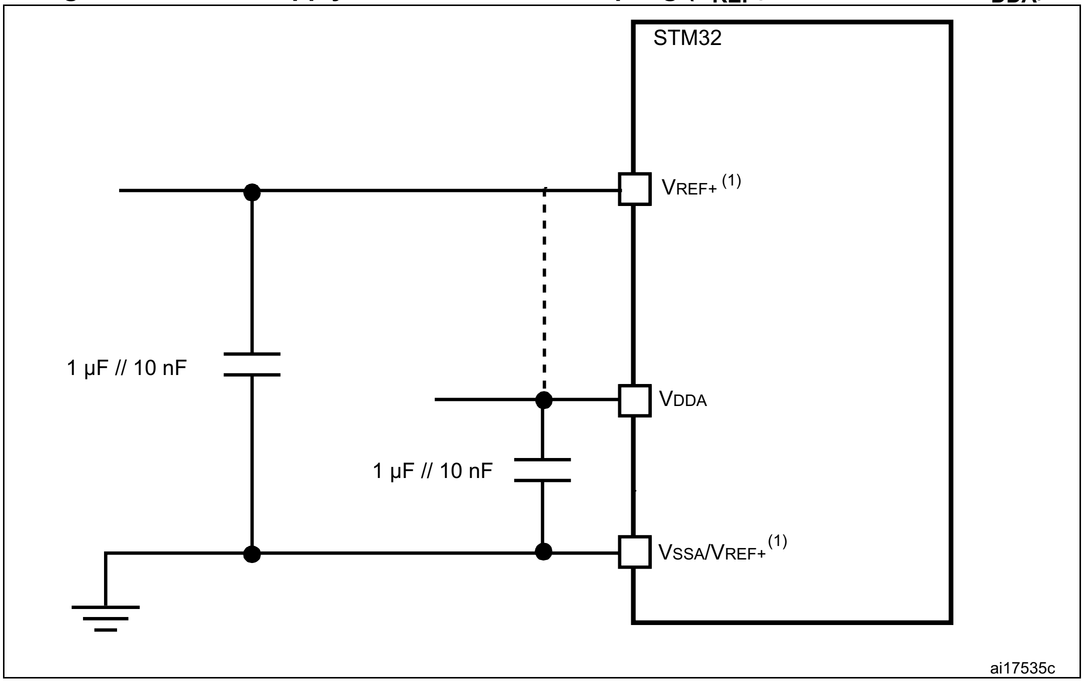


1. Refer to *Table 83* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

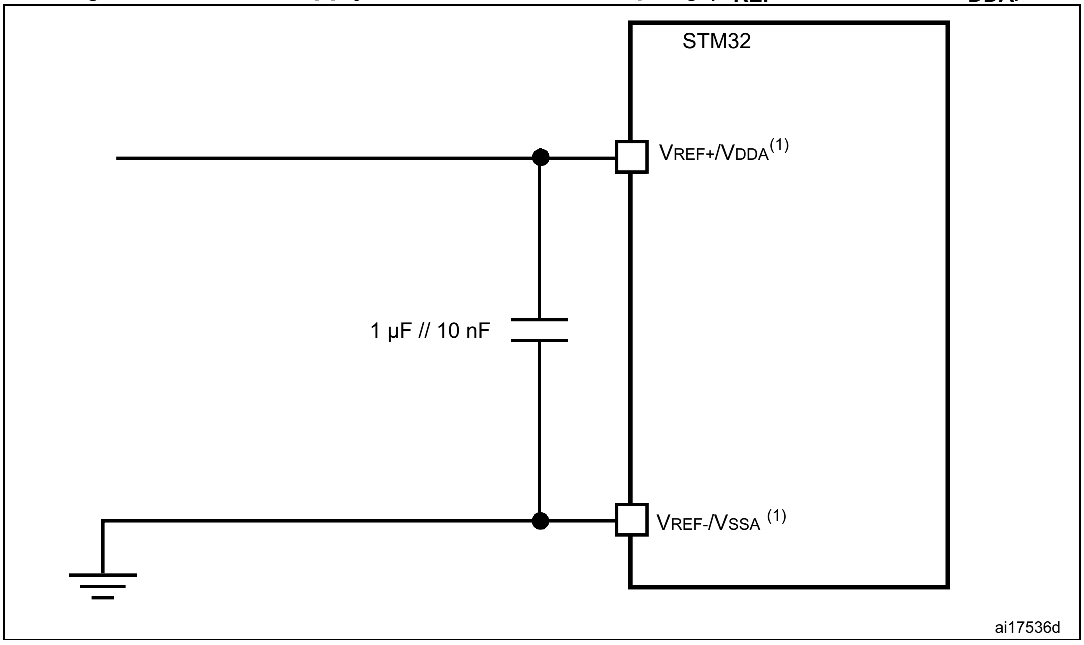
Power supply decoupling should be performed as shown in *Figure 38* or *Figure 39*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 38. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

Figure 39. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

6.3.21 DAC electrical characteristics

Table 85. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	
R_L	Resistive Load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O(1)	Output Impedance	DAC output buffer OFF		10.3	13	16	
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	
C_L(1)	Capacitive Load	DAC output buffer OFF		-	-	50	pF
C_{SH}(1)		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} −0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer OFF, ±1LSB C_L=10 pF		-	1.7(1)	2(1)	µs
t_{WAKEUP}(2)	Wakeup time from off state (setting the Enx bit in the DAC Control register) until the ±1LSB final value	Normal mode, DAC output buffer ON, $C_L \leq$ 50 pF, R_L = 5 kΩ		-	5	7.5	µs
V_{offset}(1)	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	850	-	µV
		V_{REF+} = 1.8 V		-	425	-	

Table 85. DAC characteristics (continued)

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="5">$I_{DDA(DAC)}$</td><td rowspan="5">DAC quiescent consumption from V_{DDA}</td><td rowspan="2">DAC output buffer ON</td><td>No load, middle code (0x800)</td><td>-</td><td>360</td><td>-</td><td rowspan="11">µA</td></tr>
<tr><td>No load, worst code (0xF1C)</td><td>-</td><td>490</td><td>-</td></tr>
<tr><td>DAC output buffer OFF</td><td>No load, middle/worst code (0x800)</td><td>-</td><td>20</td><td>-</td></tr>
<tr><td colspan="2">Sample and Hold mode, C_{SH}=100 nF</td><td>-</td><td>$360 \cdot T_{ON}/(T_{ON}+T_{OFF})$</td><td>-</td></tr>
<tr></tr>
<tr><td rowspan="6">$I_{DDV}(DAC)$</td><td rowspan="6">DAC consumption from V_{REF+}</td><td rowspan="2">DAC output buffer ON</td><td>No load, middle code (0x800)</td><td>-</td><td>170</td><td>-</td></tr>
<tr><td>No load, worst code (0xF1C)</td><td>-</td><td>170</td><td>-</td></tr>
<tr><td>DAC output buffer OFF</td><td>No load, middle/worst code (0x800)</td><td>-</td><td>160</td><td>-</td></tr>
<tr><td colspan="2">Sample and Hold mode, Buffer ON, C_{SH}=100 nF (worst code)</td><td>-</td><td>$170 \cdot T_{ON}/(T_{ON}+T_{OFF})$</td><td>-</td></tr>
<tr><td colspan="2">Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (worst code)</td><td>-</td><td>$160 \cdot T_{ON}/(T_{ON}+T_{OFF})$</td><td>-</td></tr>
</table>

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).

Table 86. DAC accuracy(1)

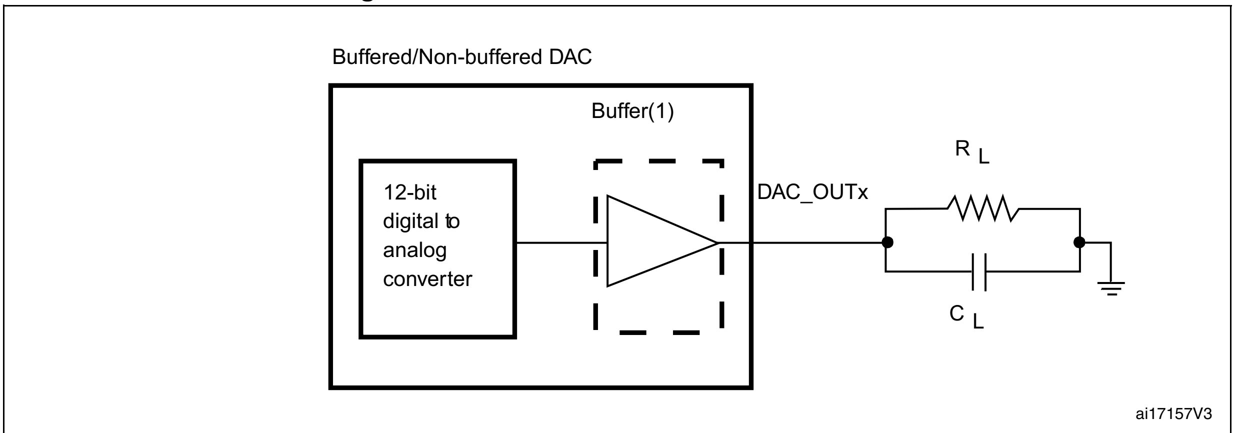
<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="2">DNL</td><td rowspan="2">Differential non linearity(2)</td><td colspan="2">DAC output buffer ON</td><td>-</td><td>±2</td><td>-</td><td rowspan="2">LSB</td></tr>
<tr><td colspan="2">DAC output buffer OFF</td><td>-</td><td>±2</td><td>-</td></tr>
<tr><td rowspan="2">INL</td><td rowspan="2">Integral non linearity(3)</td><td colspan="2">DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ</td><td>-</td><td>±4</td><td>-</td><td rowspan="2">LSB</td></tr>
<tr><td colspan="2">DAC output buffer OFF, $C_L \leq 50$ pF, no R_L</td><td>-</td><td>±4</td><td>-</td></tr>
<tr><td rowspan="3">Offset</td><td rowspan="3">Offset error at code 0x800 (3)</td><td rowspan="2">DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ</td><td>V_{REF+} = 3.6 V</td><td>-</td><td>-</td><td>±12</td><td rowspan="3">LSB</td></tr>
<tr><td>V_{REF+} = 1.8 V</td><td>-</td><td>-</td><td>±25</td></tr>
<tr><td colspan="2">DAC output buffer OFF, $C_L \leq 50$ pF, no R_L</td><td>-</td><td>-</td><td>±8</td></tr>
<tr><td>Offset1</td><td>Offset error at code 0x001(4)</td><td colspan="2">DAC output buffer OFF, $C_L \leq 50$ pF, no R_L</td><td>-</td><td>-</td><td>±5</td><td>LSB</td></tr>
</table>

Table 86. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	$V_{REF+} = 3.6$ V	-	-	±5	LSB
			$V_{REF+} = 1.8$ V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON,$C_L \leq 50$ pF, $R_L \geq 5$ kΩ		-	-	±1	%
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±1	
TUE	Total unadjusted error	DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±12	LSB
SNR	Signal-to-noise ratio(6)	DAC output buffer ON,$C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz, BW = 500 KHz		-	67.8	-	dB
SINAD	Signal-to-noise and distortion ratio(6)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz		-	67.5	-	dB
ENOB	Effective number of bits	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz		-	10.9	-	bits

1. Guaranteed by characterization.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2 V) when the buffer is ON.
6. Signal is -0.5dBFS with $F_{sampling}$=1 MHz.

Figure 40. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.22 Voltage reference buffer characteristics

Table 87. VREFBUF characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VSCALE = 000	2.8	3.3	3.6	V
			VSCALE = 001	2.4	-	3.6	
			VSCALE = 010	2.1	-	3.6	
			VSCALE = 011	1.8	-	3.6	
		Degraded mode	VSCALE = 000	1.62	-	2.80	
			VSCALE = 001	1.62	-	2.40	
			VSCALE = 010	1.62	-	2.10	
			VSCALE = 011	1.62	-	1.80	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode	VSCALE = 000	-	2.5	-	
			VSCALE = 001	-	2.048	-	
			VSCALE = 010	-	1.8	-	
			VSCALE = 011	-	1.5	-	
		Degraded mode[2]	VSCALE = 000	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 001	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 010	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 011	V_{DDA}– 150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.2	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal Mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	−40 °C < T_J < +105 °C	-	-	-	T_{coeff} xV_{REFINT} + 50	ppm/ °C
		0 °C < T_J < +50 °C	-	-	-	T_{coeff} xV_{REFINT} + 50	
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100KHz	-	-	40	-	

Table 87. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{START}	Start-up time	C_L=0.5 µF	-	-	300	-	µs
		C_L=1 µF	-	-	500	-	
		C_L=1.5 µF	-	-	650	-	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(3)	-		-	8	-	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	25	µA
		I_{LOAD} = 500 µA	-	-	16	30	
		I_{LOAD} = 4 mA	-	-	32	50	

1. Guaranteed by design.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}−drop voltage).
3. To properly control VREFBUF I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 1.8 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VSCALE = 011, 010, 001 and 000, respectively.

6.3.23 Temperature sensor characteristics

Table 88. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	-	3	°C
Avg_Slope(2)	Average slope	-	2	-	mV/°C
V_{30}(3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run}(1)	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. Guaranteed by design.
2. Guaranteed by characterization.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

Table 89. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA}=3.3 V	0x1FF1 E820 -0x1FF1 E821
TS_CAL2	Temperature sensor raw data acquired value at 110 °C, V_{DDA}=3.3 V	0x1FF1 E840 - 0x1FF1 E841

6.3.24 V_{BAT} monitoring characteristics

Table 90. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	26	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input				µs

1. Guaranteed by design.

Table 91. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	KΩ
		VBRS in PWR_CR3= 1		1.5	-	

6.3.25 Voltage booster for analog switch

Table 92. Voltage booster for analog switch characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.62	2-6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	$1.62\ V \leq V_{DD} \leq 2.7\ V$	-	-	125	µA
		$2.7\ V < V_{DD} < 3.6\ V$	-	-	250	

6.3.26 Comparator characteristics

Table 93. COMP characteristics(1)

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>V_{DDA}</td><td>Analog supply voltage</td><td colspan="2">-</td><td>1.62</td><td>3.3</td><td>3.6</td><td rowspan="3">V</td></tr>
<tr><td>V_{IN}</td><td>Comparator input voltage range</td><td colspan="2">-</td><td>0</td><td>-</td><td>V_{DDA}</td></tr>
<tr><td>V_{BG}(2)</td><td>Scaler input voltage</td><td colspan="2">-</td><td colspan="3">Refer to V_{REFINT}</td></tr>
<tr><td>V_{SC}</td><td>Scaler offset voltage</td><td colspan="2">-</td><td>-</td><td>±5</td><td>±10</td><td>mV</td></tr>
<tr><td rowspan="2">$I_{DDA(SCALER)}$</td><td rowspan="2">Scaler static consumption from V_{DDA}</td><td colspan="2">BRG_EN=0 (bridge disable)</td><td>-</td><td>0.2</td><td>0.3</td><td rowspan="2">µA</td></tr>
<tr><td colspan="2">BRG_EN=1 (bridge enable)</td><td>-</td><td>0.8</td><td>1</td></tr>
<tr><td>t_{START_SCALER}</td><td>Scaler startup time</td><td colspan="2">-</td><td>-</td><td>140</td><td>250</td><td>µs</td></tr>
<tr><td rowspan="3">t_{START}</td><td rowspan="3">Comparator startup time to reach propagation delay specification</td><td colspan="2">High-speed mode</td><td>-</td><td>2</td><td>5</td><td rowspan="3">µs</td></tr>
<tr><td colspan="2">Medium mode</td><td>-</td><td>5</td><td>20</td></tr>
<tr><td colspan="2">Ultra-low-power mode</td><td>-</td><td>15</td><td>80</td></tr>
<tr><td rowspan="6">t_D</td><td rowspan="3">Propagation delay for 200 mV step with 100 mV overdrive</td><td colspan="2">High-speed mode</td><td>-</td><td>50</td><td>80</td><td>ns</td></tr>
<tr><td colspan="2">Medium mode</td><td>-</td><td>0.5</td><td>1.2</td><td rowspan="2">µs</td></tr>
<tr><td colspan="2">Ultra-low-power mode</td><td>-</td><td>2.5</td><td>7</td></tr>
<tr><td rowspan="3">Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs</td><td colspan="2">High-speed mode</td><td>-</td><td>50</td><td>120</td><td>ns</td></tr>
<tr><td colspan="2">Medium mode</td><td>-</td><td>0.5</td><td>1.2</td><td rowspan="2">µs</td></tr>
<tr><td colspan="2">Ultra-low-power mode</td><td>-</td><td>2.5</td><td>7</td></tr>
<tr><td>V_{offset}</td><td>Comparator offset error</td><td colspan="2">Full common mode range</td><td>-</td><td>±5</td><td>±20</td><td>mV</td></tr>
<tr><td rowspan="4">V_{hys}</td><td rowspan="4">Comparator hysteresis</td><td colspan="2">No hysteresis</td><td>-</td><td>0</td><td>-</td><td rowspan="4">mV</td></tr>
<tr><td colspan="2">Low hysteresis</td><td>-</td><td>10</td><td>-</td></tr>
<tr><td colspan="2">Medium hysteresis</td><td>-</td><td>20</td><td>-</td></tr>
<tr><td colspan="2">High hysteresis</td><td>-</td><td>30</td><td>-</td></tr>
<tr><td rowspan="6">I_{DDA}(COMP)</td><td rowspan="6">Comparator consumption from V_{DDA}</td><td rowspan="2">Ultra-low-power mode</td><td>Static</td><td>-</td><td>400</td><td>600</td><td rowspan="2">nA</td></tr>
<tr><td>With 50 kHz ±100 mV overdrive square signal</td><td>-</td><td>800</td><td>-</td></tr>
<tr><td rowspan="2">Medium mode</td><td>Static</td><td>-</td><td>5</td><td>7</td><td rowspan="4">µA</td></tr>
<tr><td>With 50 kHz ±100 mV overdrive square signal</td><td>-</td><td>6</td><td>-</td></tr>
<tr><td rowspan="2">High-speed mode</td><td>Static</td><td>-</td><td>70</td><td>100</td></tr>
<tr><td>With 50 kHz ±100 mV overdrive square signal</td><td>-</td><td>75</td><td>-</td></tr>
</table>

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 26: Embedded reference voltage*.

6.3.27 Operational amplifiers characteristics

Table 94. OPAMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage Range	-	2	3.3	3.6	V
CMIR	Common Mode Input Range	-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	25°C, no load on output	-	-	±1.5	mV
		All voltages and temperature, no load	-	-	±2.5	mV
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±3.0	-	µV/°C
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1*V_{DDA})	-	-	1.1	1.5	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9*V_{DDA})	-	-	1.1	1.5	mV
I_{LOAD}	Drive current	-	-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-	-	-	270	µA
C_{LOAD}	Capacitive load	-	-	-	50	pF
CMRR	Common mode rejection ratio	-	-	80	-	dB
PSRR	Power supply rejection ratio	$C_{LOAD} \leq 50pf$ / $R_{LOAD} \geq 4\ k\Omega$(2) at 1 kHz, $V_{com}=V_{DDA}/2$	-	66	-	dB
GBW	Gain bandwidth product for high supply range	-	-	7.3	-	MHz
SR	Slew rate (from 10% and 90% of output voltage)	Normal mode	-	3	-	V/µs
		High-speed mode	-	30	-	V/µs
AO	Open loop gain	-	-	90	-	dB
φm	Phase margin	-	-	55	-	°
GM	Gain margin	-	-	12	-	dB

Table 94. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OHSAT}	High saturation voltage	I_{load}=max or R_{LOAD}=min(2), Input at V_{DDA}		V_{DDA} −100 mV	-	-	mV
V_{OLSAT}	Low saturation voltage	I_{load}=max or R_{LOAD}=min(2), Input at 0 V		-	-	100	mV
t_{WAKEUP}	Wake up time from OFF state	Normal mode	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ(2), follower configuration	-	0.8	3.2	µs
		High speed	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ(2), follower configuration	-	0.9	2.8	
PGA gain	Non inverting gain value	-		-	2	-	-
		-		-	4	-	-
		-		-	8	-	-
		-		-	16	-	-
	Inverting gain value	-		-	−1	-	-
		-		-	−3	-	-
		-		-	−7	-	-
		-		-	−15	-	-
$R_{network}$	R2/R1 internal resistance values in non-inverting PGA mode(3)	PGA Gain=2		-	10/10	-	kΩ/kΩ
		PGA Gain=4		-	30/10	-	
		PGA Gain=8		-	70/10	-	
		PGA Gain=16		-	150/10	-	
	R2/R1 internal resistance values in inverting PGA mode(3)	PGA Gain=-1		-	10/10	-	
		PGA Gain=-3		-	30/10	-	
		PGA Gain=-7		-	70/10	-	
		PGA Gain=-15		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		−15	-	15	%
PGA BW	PGA bandwidth for different non inverting gain	Gain=2		-	GBW/2	-	MHz
		Gain=4		-	GBW/4	-	
		Gain=8		-	GBW/8	-	
		Gain=16		-	GBW/16	-	

Table 94. OPAMP characteristics[1] (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	140	-	nV/√Hz
		at 10 KHz		-	55	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	570	1000	µA
		High-speed mode		-	610	1200	

1. Guaranteed by design, unless otherwise specified.
2. R_{LOAD} is the resistive load connected to VSSA or to VDDA.
3. R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

6.3.28 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 95* for DFSDM are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDMx_CKINx, DFSDMx_DATINx, DFSDMx_CKOUT for DFSDMx).

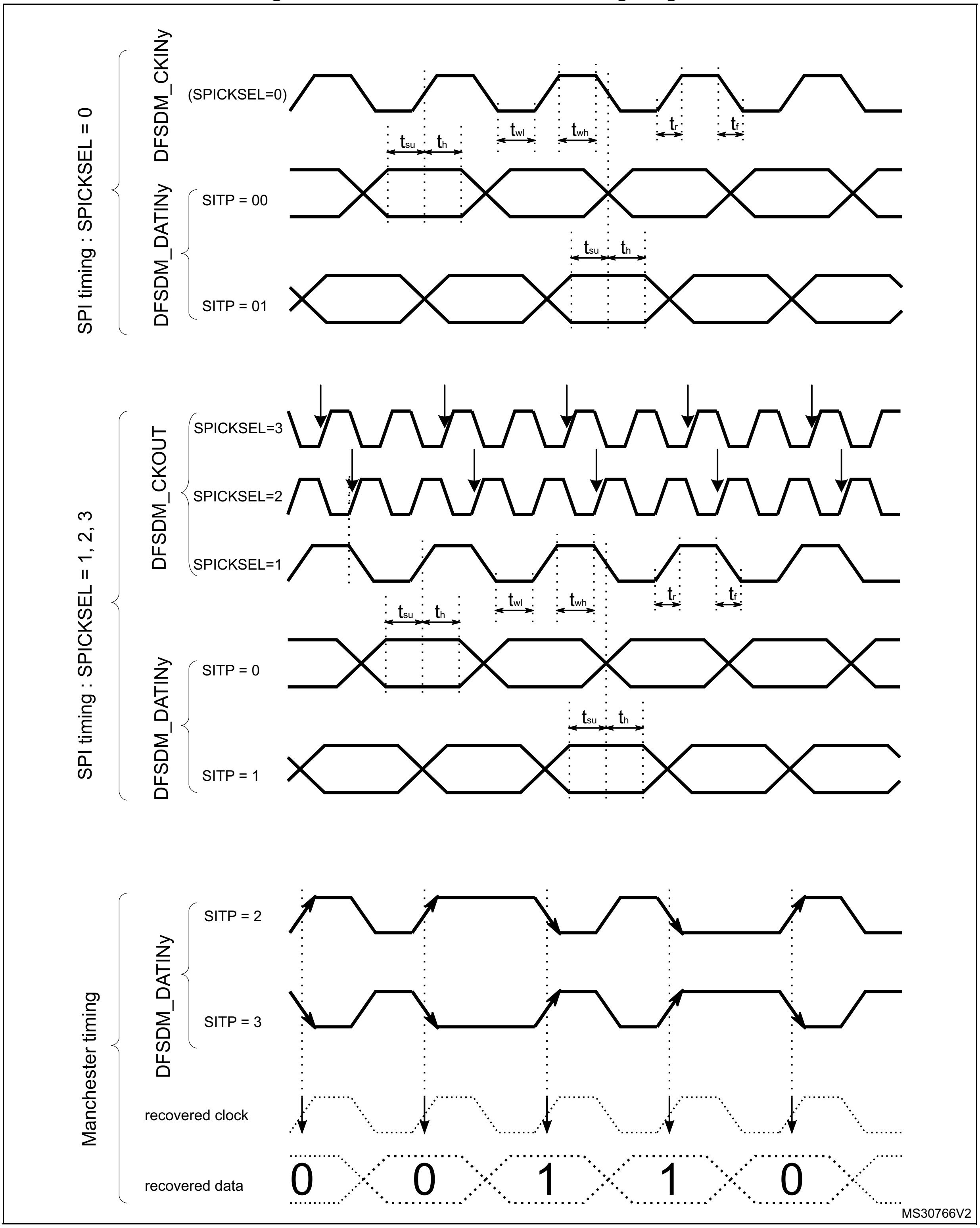
Table 95. DFSDM measured timing 1.62-3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.62 V < V_{DD} < 3.6 V	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 V < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}/4$)	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}/4$)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 1.62 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}/4$)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}/4$)	
f_{CKOUT}	Output clock frequency	1.62 < V_{DD} < 3.6 V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.62 < V_{DD} < 3.6 V	45	50	55	%

Table 95. DFSDM measured timing 1.62-3.6 V (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	TCKIN/2 - 0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	4	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	0.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), $1.62 < V_{DD} < 3.6$ V	(CKOUTDIV+1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

Figure 41. Channel transceiver timing diagrams



6.3.29 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 96* for DCMI are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

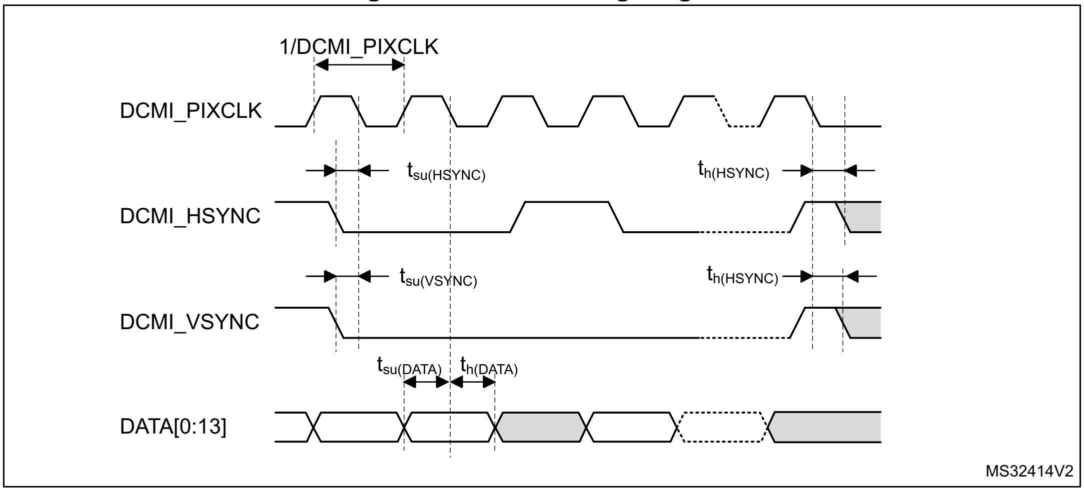
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Table 96. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/$f_{rcc\_c\_ck}$	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	80	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	1	-	ns
$t_{h(DATA)}$	Data input hold time	1	-	ns
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	1.5	-	ns
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	1	-	ns

1. Guaranteed by characterization results.

Figure 42. DCMI timing diagram



6.3.30 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 97* for LCD-TFT are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled

Table 97. LTDC characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CLK}	LTDC clock output frequency	2.7 V < V_{DD} < 3.6 V, 20 pF	-	150	MHz
		2.7 V < V_{DD} < 3.6 V	-	133	
		1.62 V < V_{DD} < 3.6 V	-	90	
D_{CLK}	LTDC clock output duty cycle	-	45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time		$t_{w(CLK)}/2-0.5$	$t_{w(CLK)}/2+0.5$	ns
$t_{v(DATA)}$	Data output valid time		-	0.5	
$t_{h(DATA)}$	Data output hold time		0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time		-	0.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time		0.5	-	

1. Guaranteed by characterization results.

Figure 43. LCD-TFT horizontal timing diagram

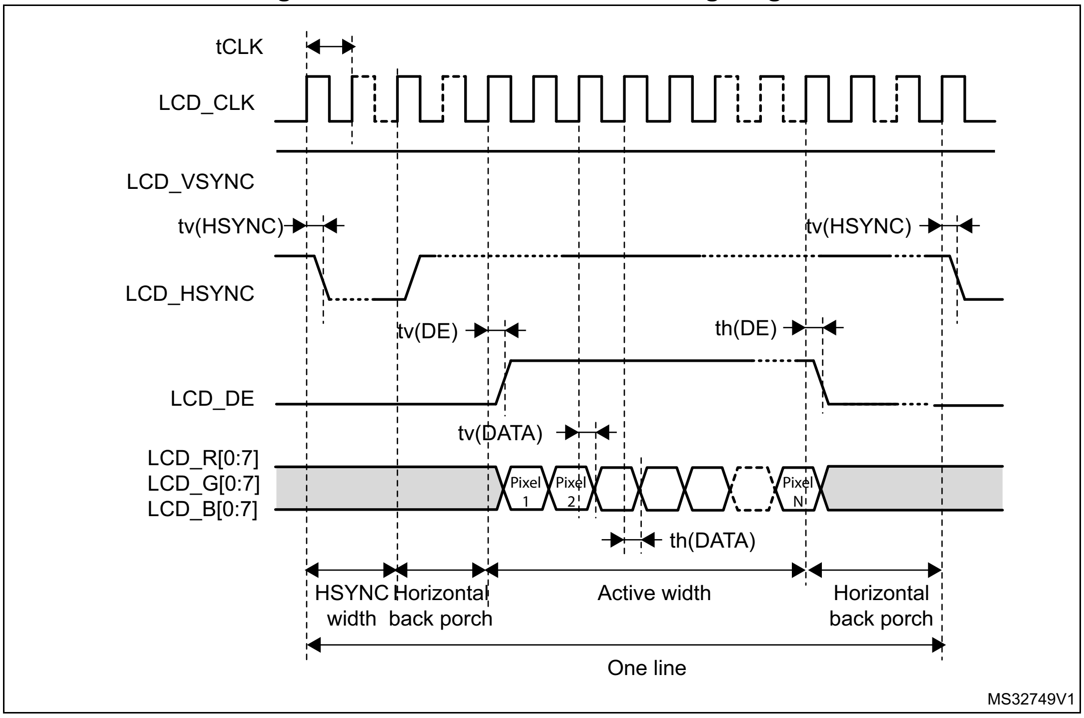
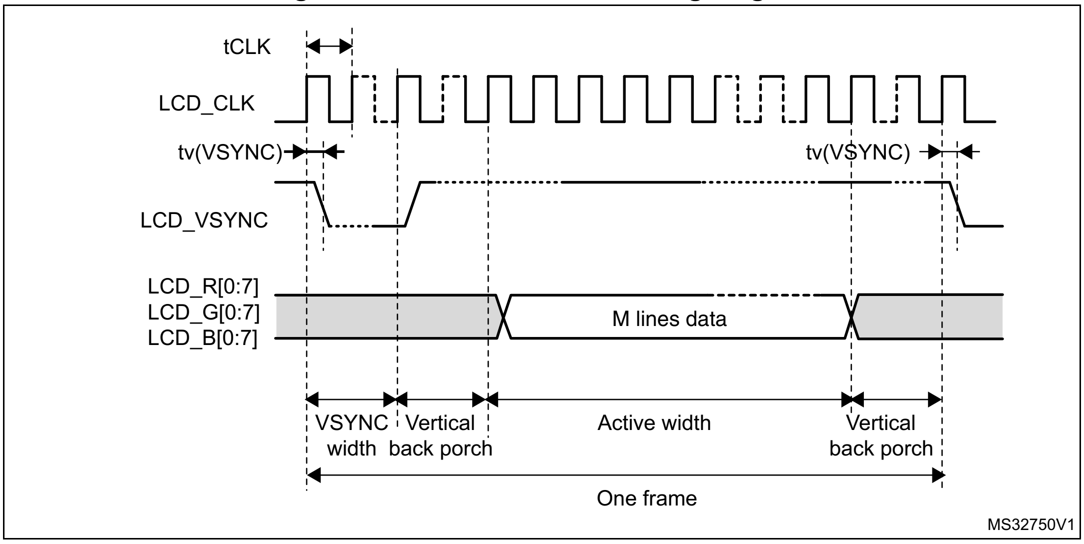


Figure 44. LCD-TFT vertical timing diagram



6.3.31 Timer characteristics

The parameters given in *Table 98* are guaranteed by design.

Refer to *Section 6.3.15: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 98. TIMx characteristics[1][2]

Symbol	Parameter	Conditions[3]	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 200 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 100 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 200 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 200 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4x $F_{rcc\_pclkx\_d2}$.

6.3.32 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0433 reference manual) and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

Table 99. Minimum i2c_ker_ck frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode		2	MHz
		Fast-mode	Analog filter ON DNF=0	8	
			Analog filter OFF DNF=1	9	
		Fast-mode Plus	Analog filter ON DNF=0	17	
			Analog filter OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{load} supported in Fm+, which is given by these formulas:

$$t_{r(SDA/SCL)}=0.8473 x R_p x C_{load}$$

$$R_{p(min)}= (V_{DD}-V_{OL(max)})/I_{OL(max)}$$

Where R_p is the I2C lines pull-up. Refer to *Section 6.3.15: I/O port characteristics* for the I2C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to *Table 100* for the analog filter characteristics:

Table 100. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 101* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled
- HSLV activated when VDD ≤ 2.7 V

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 101. SPI dynamic characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 1.62 V≤V_{DD}≤3.6 V	-	-	90	MHz
		Master mode 2.7 V≤V_{DD}≤3.6 V SPI1,2,3			133	
		Master mode 2.7 V≤V_{DD}≤3.6 V SPI4,5,6			100	
		Slave receiver mode 1.62 V≤V_{DD}≤3.6 V SPI1,2,3			150	
		Slave receiver mode 1.62 V≤V_{DD}≤3.6 V SPI4,5,6			100	
		Slave mode transmitter/full duplex 2.7 V≤V_{DD}≤3.6 V			31	
		Slave mode transmitter/full duplex 1.62 V≤V_{DD}≤3.6 V			25	
$t_{su(NSS)}$	NSS setup time	Slave mode	2	-	-	ns
$t_{h(NSS)}$	NSS hold time		1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PLCK} - 2	T_{PLCK}	T_{PLCK} + 2	

Table 101. SPI dynamic characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MI)}$	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$		Slave mode	2	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	13	27	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	1	5	
$t_{v(SO)}$	Data output valid time	Slave mode, 2.7 V≤V_{DD}≤3.6 V	-	11.5	16	
		Slave mode 1.62 V≤V_{DD}≤3.6 V	-	13	20	
$t_{v(MO)}$		Master mode	-	1	3	
$t_{h(SO)}$	Data output hold time	Slave mode, 1.62 V≤V_{DD}≤3.6 V	9	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.

Figure 45. SPI timing diagram - slave mode and CPHA = 0

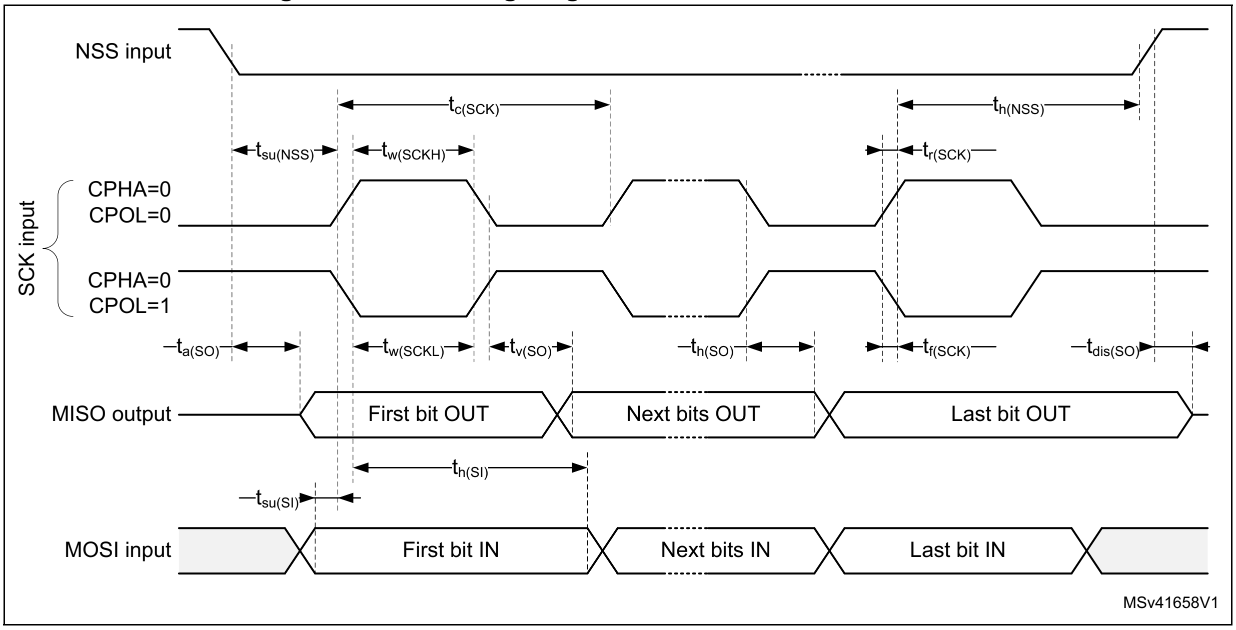
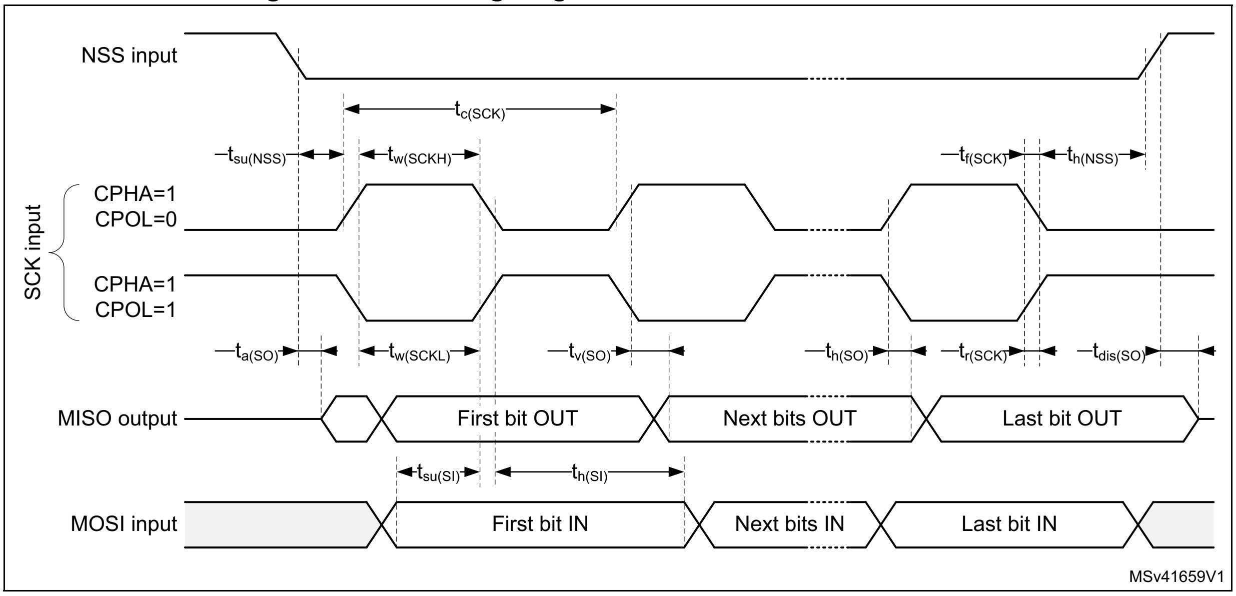
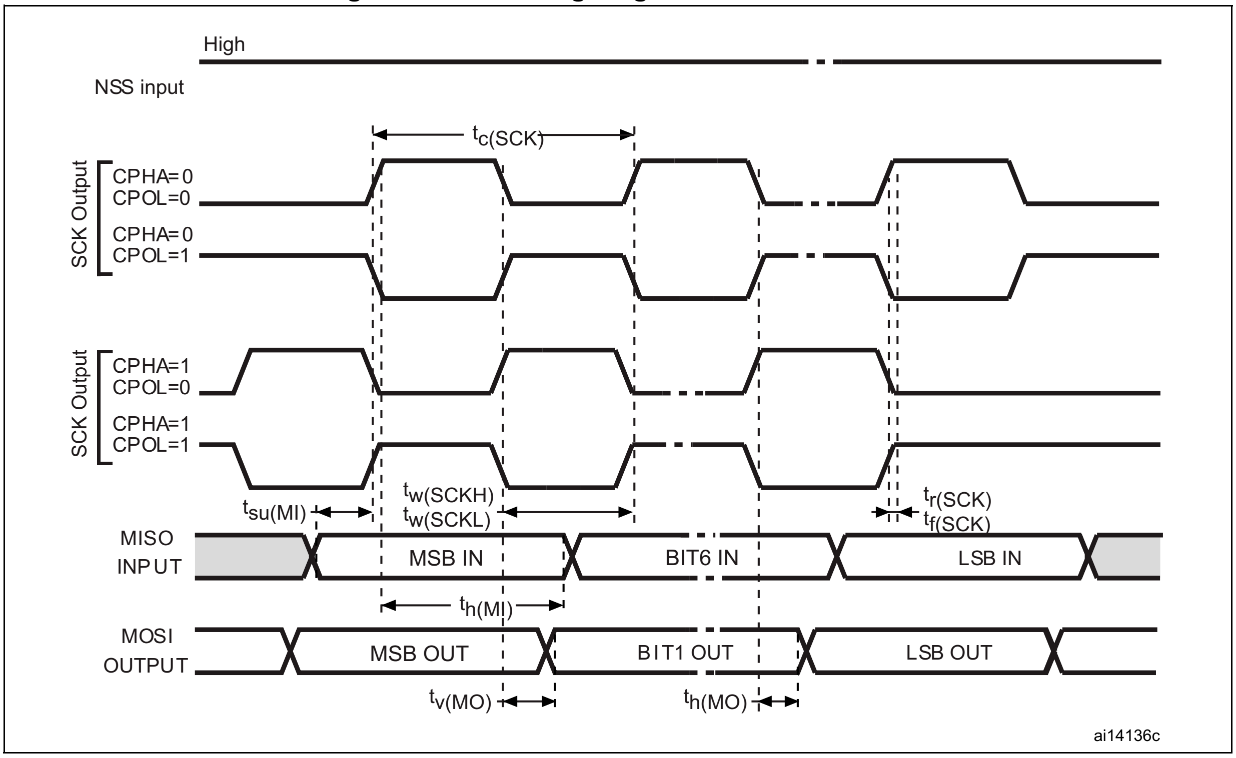


Figure 46. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 47. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 102* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled

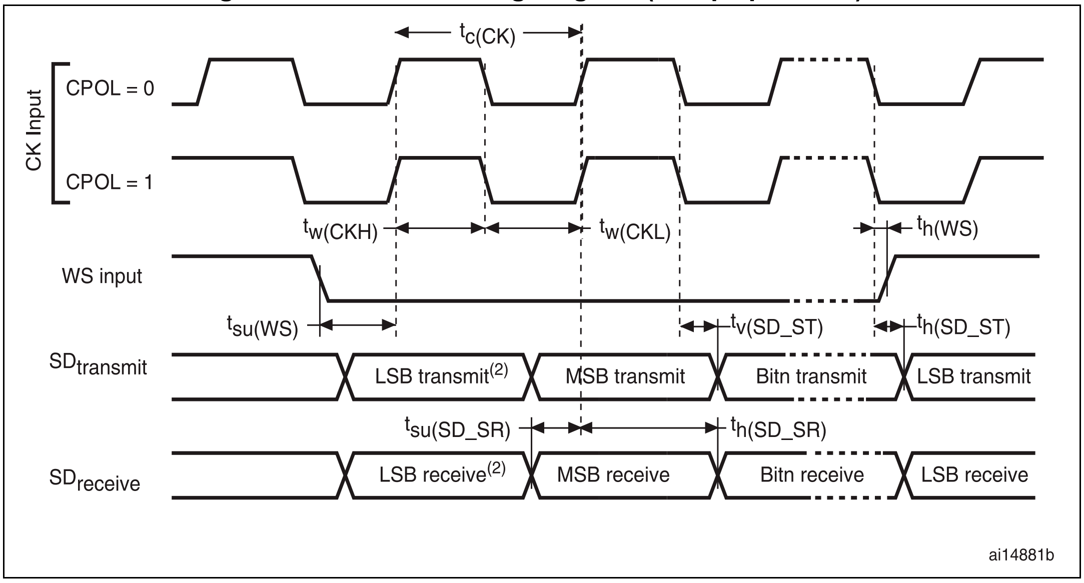
Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 102. I²S dynamic characteristics[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs	MHz
f_{CK}	I2S clock frequency	Master data	-	64xFs	MHz
		Slave data	-	64xFs	
$t_{v(WS)}$	WS valid time	Master mode	-	3.5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

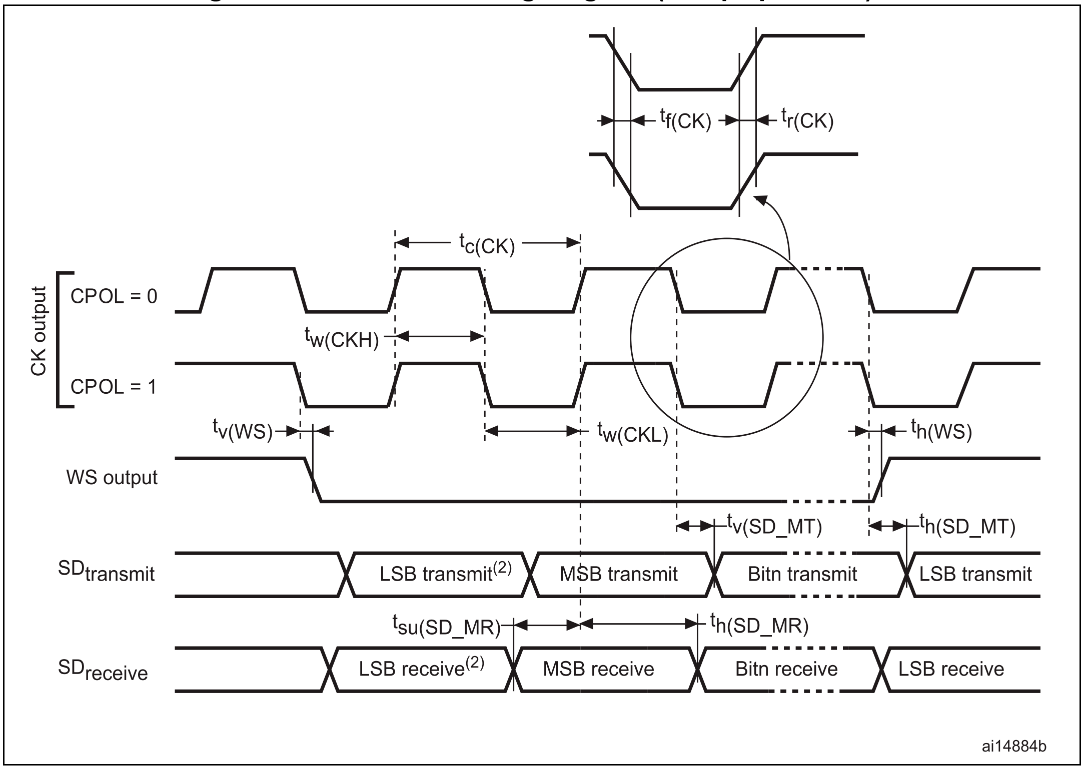
1. Guaranteed by characterization results.

Figure 48. I²S slave timing diagram (Philips protocol)[1]



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 49. I²S master timing diagram (Philips protocol)[1]



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 103* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 103. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	256 x 8K	256xFs	MHz
F_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128xFs(3)	MHz
		Slave data: 32 bits	-	128xFs	
$t_{v(FS)}$	FS valid time	Master mode 2.7≤VDD≤3.6V	-	15	ns
		Master mode 1.71≤VDD≤3.6V	-	20	
$t_{su(FS)}$	FS setup time	Slave mode	7	-	
$t_{h(FS)}$	FS hold time	Master mode	1	-	
		Slave mode	1	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	0.5	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) $2.7 \leq V_{DD} \leq 3.6V$	-	17	ns
		Slave transmitter (after enable edge) $1.62 \leq V_{DD} \leq 3.6V$	-	20	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) $2.7 \leq V_{DD} \leq 3.6V$	-	17	
		Master transmitter (after enable edge) $1.62 \leq V_{DD} \leq 3.6V$	-	20	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	7.55	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With F_S=192 kHz.

Figure 50. SAI master timing waveforms

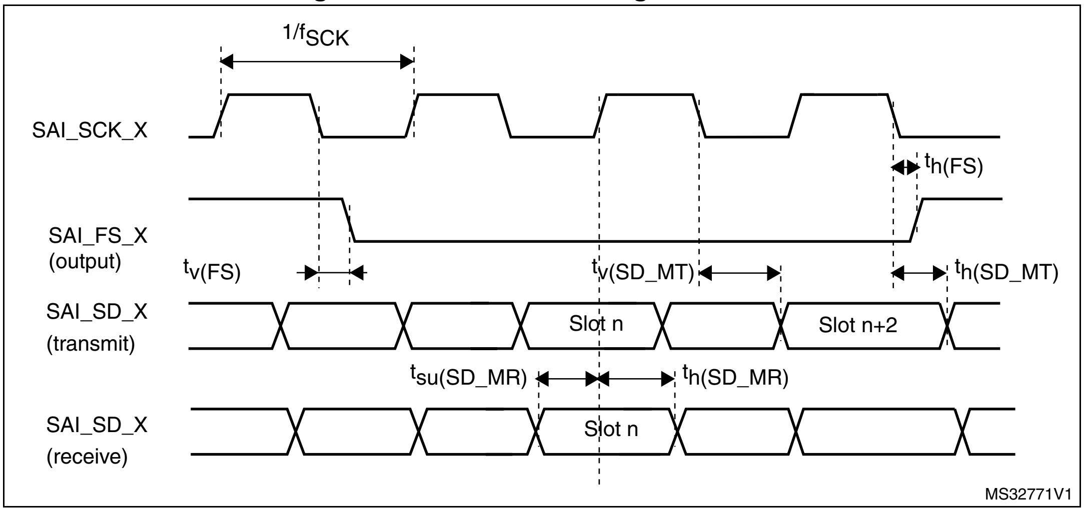
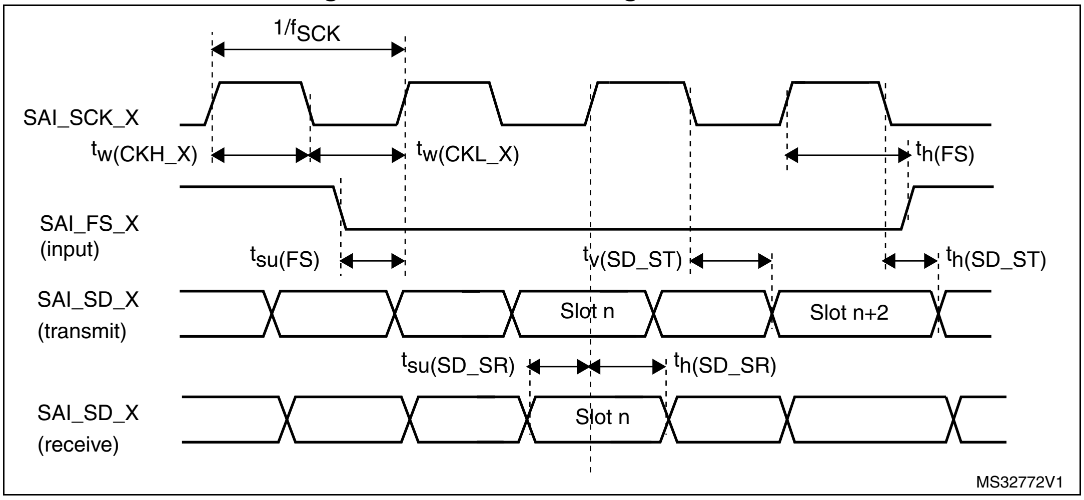


Figure 51. SAI slave timing waveforms



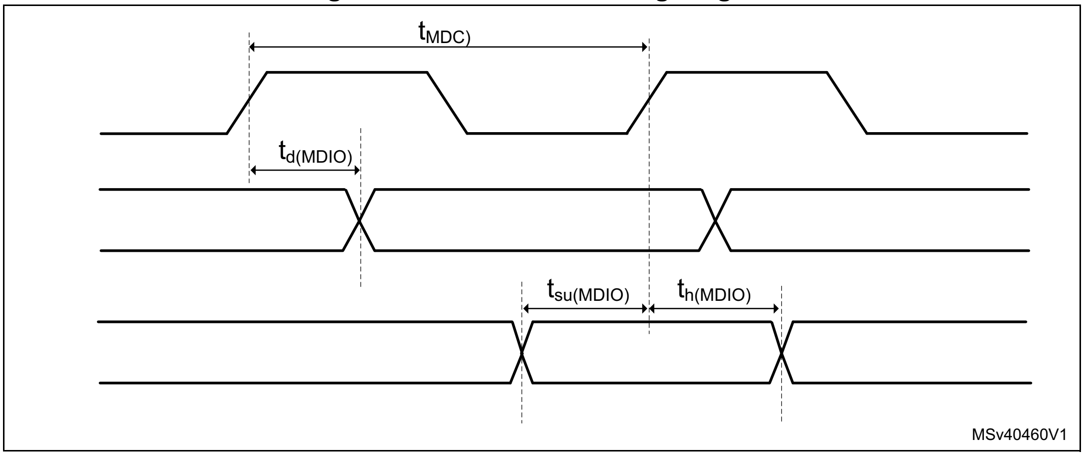
MDIO characteristics

Table 104. MDIO Slave timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{sDC}	Management data clock	-	-	40	MHz
$t_{d(MDIO)}$	Management data input/output **output valid time**	7	8	20	ns
$t_{su(MDIO)}$	Management data input/output **setup time**	4	-	-	ns
$t_{h(MDIO)}$	Management data input/output **hold time**	1	-	-	ns

The MDIO controller is mapped on APB2 domain. The frequency of the APB bus should at least 1.5 times the MDC frequency: $F_{PCLK2} \geq 1.5 * F_{MDC}$.

Figure 52. MDIO Slave timing diagram



SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 105* for the SDIO/MMC interface are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled
- HSLV activated when VDD ≤ 2.7 V

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 105. Dynamic characteristics: SD / MMC characteristics, V_{DD}=2.7V to 3.6V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	125	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS/SDR/DDR mode						
t_{ISU}	Input setup time HS	f_{PP} ≥ 50 MHz	2	-	-	ns
t_{IH}	Input hold time HS		1.5	-	-	
t_{IDW}(3)	Input valid window (variable window)		3	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS/SDR/DDR mode						
t_{OV}	Output valid time HS	f_{PP} ≥ 50 MHz	-	3.5	5	ns
t_{OH}	Output hold time HS		2	-	-	

Table 105. Dynamic characteristics: SD / MMC characteristics, V_{DD}=2.7V to 3.6V(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} =25 MHz	2	-	-	ns
t_{IHD}	Input hold time SD		1.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} =25 MHz	-	1	2	ns
t_{OHD}	Output hold default time SD		0	-	-	

1. Guaranteed by characterization results.
2. Above 100 MHz, C_L = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 106. Dynamic characteristics: eMMC characteristics, V_{DD}=1.71V to 1.9V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	120	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	$f_{PP} \geq$ 50 MHz	1.5	-	-	ns
t_{IH}	Input hold time HS		2	-	-	
t_{IDW}(3)	Input valid window (variable window)		3.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	$f_{PP} \geq$ 50 MHz	-	5	7	ns
t_{OH}	Output hold time HS		3	-	-	

1. Guaranteed by characterization results.
2. C_L = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Figure 53. SDIO high-speed mode

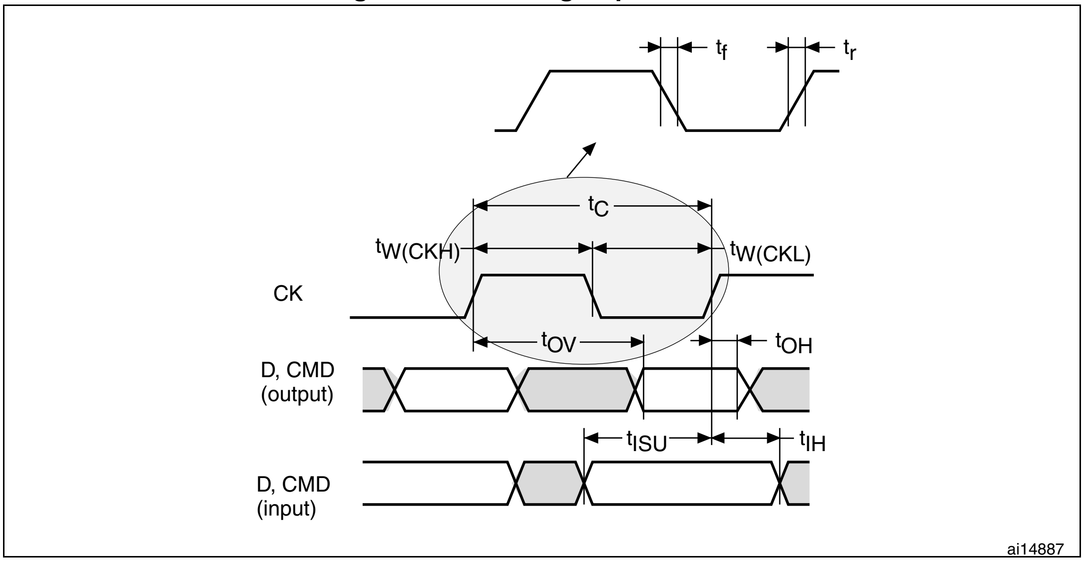


Figure 54. SD default mode

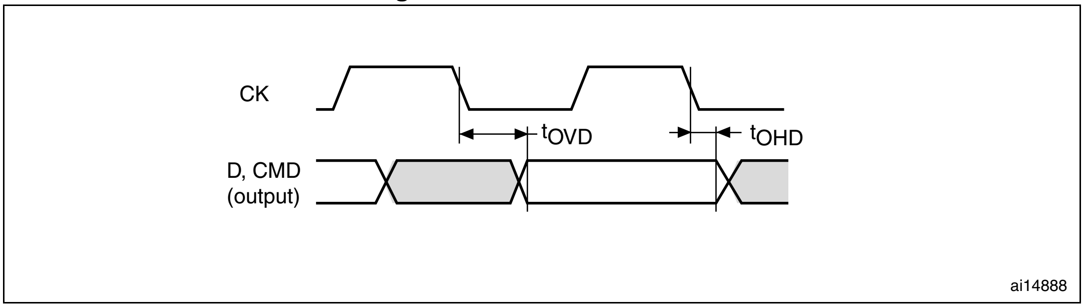
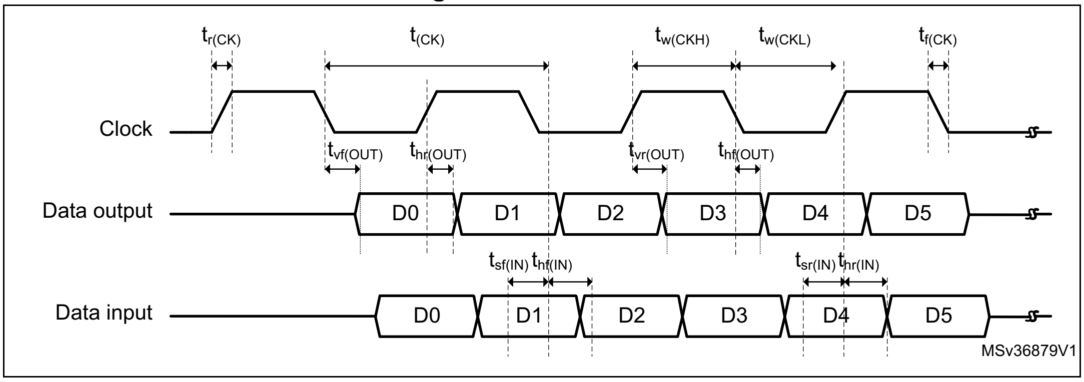


Figure 55. DDR mode



CAN (controller area network) interface

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).

USB OTG_FS characteristics

The USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 107. USB OTG_FS electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD33USB}$	USB transceiver operating voltage	-	3.0[1]	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}	Output driver impedance[2]	Driver high and low	28	36	44	

1. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V voltage range.
2. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

USB OTG_HS characteristics

Unless otherwise specified, the parameters given in *Table 108* for ULPI are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

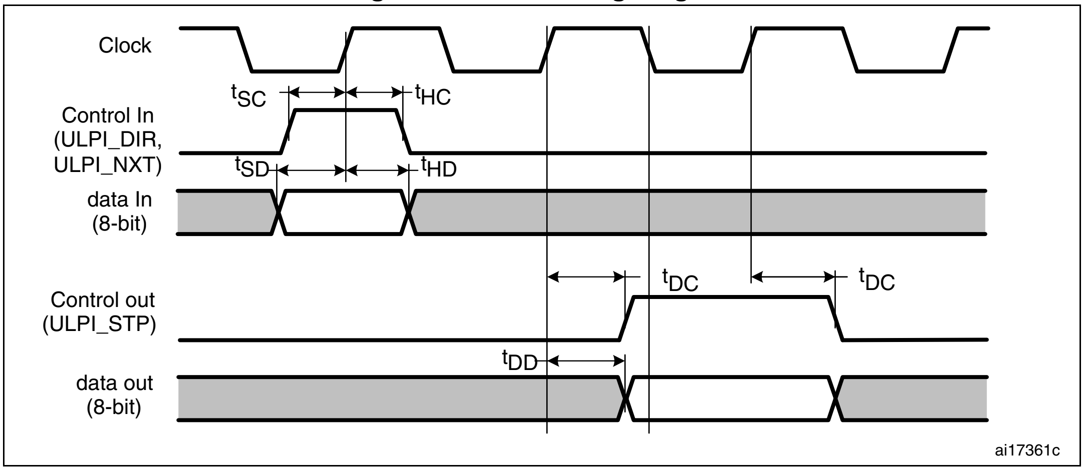
Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 108. Dynamic characteristics: USB ULPI[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	0.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	6.5	-	-	
t_{SD}	Data in setup time	-	2.5	-	-	
t_{HD}	Data in hold time	-	0	-	-	
t_{DC}/t_{DD}	Data/control output delay	$2.7\ V < V_{DD} < 3.6\ V$, $C_L = 20\ pF$	-	6.5	8.5	
		-	-	6.5	13	
		$1.7\ V < V_{DD} < 3.6\ V$, $C_L = 15\ pF$	-			

1. Guaranteed by characterization results.

Figure 56. ULPI timing diagram



Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 109*, *Table 110* and *Table 111* for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 109 gives the list of Ethernet MAC signals for the SMI and *Figure 57* shows the corresponding timing diagram.

Table 109. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	400	400	403	ns
$T_{d(MDIO)}$	Write data valid time	1	1.5	3	
$t_{su(MDIO)}$	Read data setup time	8	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Figure 57. Ethernet SMI timing diagram

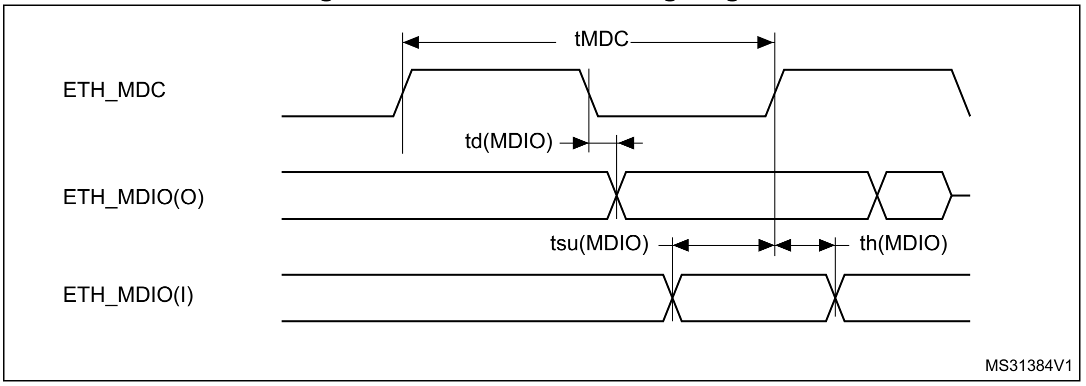


Table 110 gives the list of Ethernet MAC signals for the RMII and *Figure 58* shows the corresponding timing diagram.

Table 110. Dynamics characteristics: Ethernet MAC signals for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	3	-	-	
$t_{su(CRS)}$	Carrier sense setup time	2.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	4	4.5	7	
$t_{d(TXD)}$	Transmit data valid delay time	7	7.5	11.5	

1. Guaranteed by characterization results.

Figure 58. Ethernet RMII timing diagram

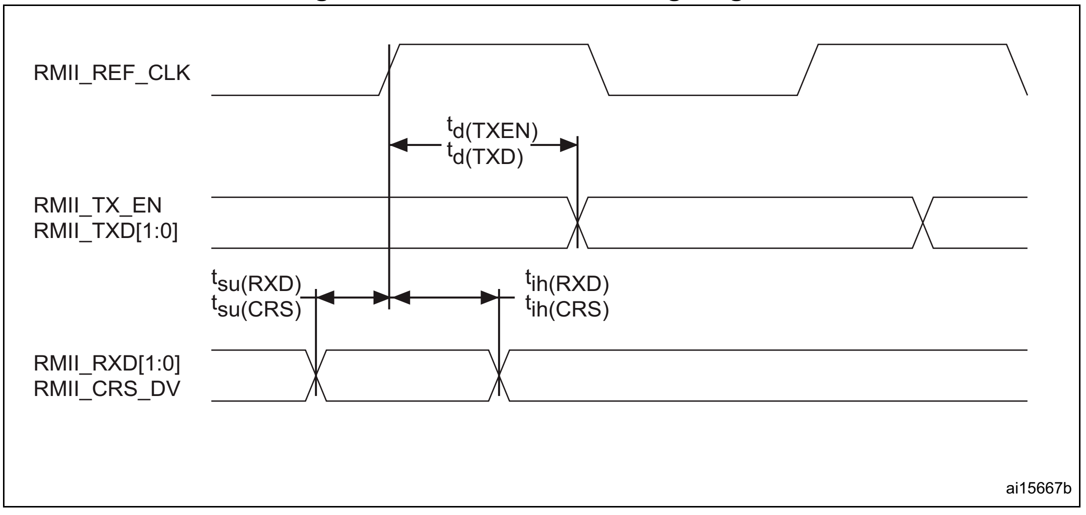


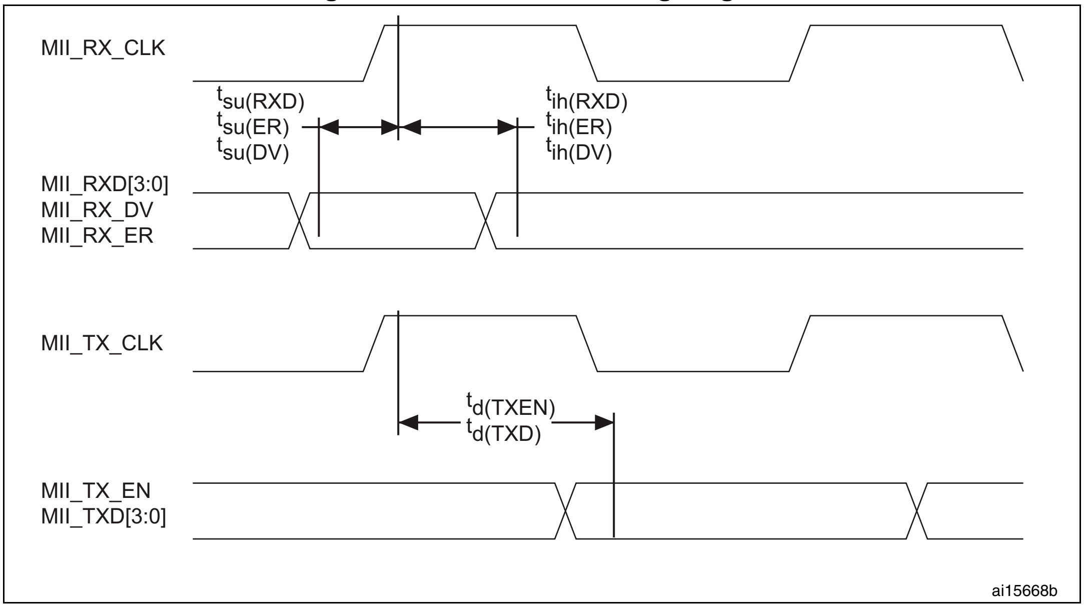
Table 111 gives the list of Ethernet MAC signals for MII and *Figure 59* shows the corresponding timing diagram.

Table 111. Dynamics characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	3	-	-	
$t_{su(DV)}$	Data valid setup time	1.5	-	-	
$t_{ih(DV)}$	Data valid hold time	1	-	-	
$t_{su(ER)}$	Error setup time	1.5	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	4.5	6.5	11	
$t_{d(TXD)}$	Transmit data valid delay time	7	7.5	15	

1. Guaranteed by characterization results.

Figure 59. Ethernet MII timing diagram



6.3.33 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 112* and *Table 113* for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 112. Dynamics characteristics: JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	T_{CK} clock frequency	2.7 V <V_{DD}< 3.6 V	-	-	37	MHz
$1/t_{c(TCK)}$		1.62 V <V_{DD}< 3.6 V	-	-	27.5	
$ti_{su(TMS)}$	TMS input setup time	-	2	-	-	
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1.5	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	1	-	-	
$t_{ov\ (TDO)}$	TDO output valid time	2.7 V <V_{DD}< 3.6 V	-	8	13.5	
		1.62 V <V_{DD}< 3.6 V	-	8	18	
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	

Table 113. Dynamics characteristics: SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	2.7 V <V_{DD}< 3.6 V	-	-	71	MHz
$1/t_{c(SWCLK)}$		1.62 V <V_{DD}< 3.6 V	-	-	55.5	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	
$ti_{h(SWDIO)}$	SWDIO input hold time	-	1	-	-	
$t_{ov\ (SWDIO)}$	SWDIO output valid time	2.7 V <V_{DD}< 3.6 V	-	8.5	14	
		1.62 V <V_{DD}< 3.6 V	-	8.5	18	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8	-	-	

Figure 60. JTAG timing diagram

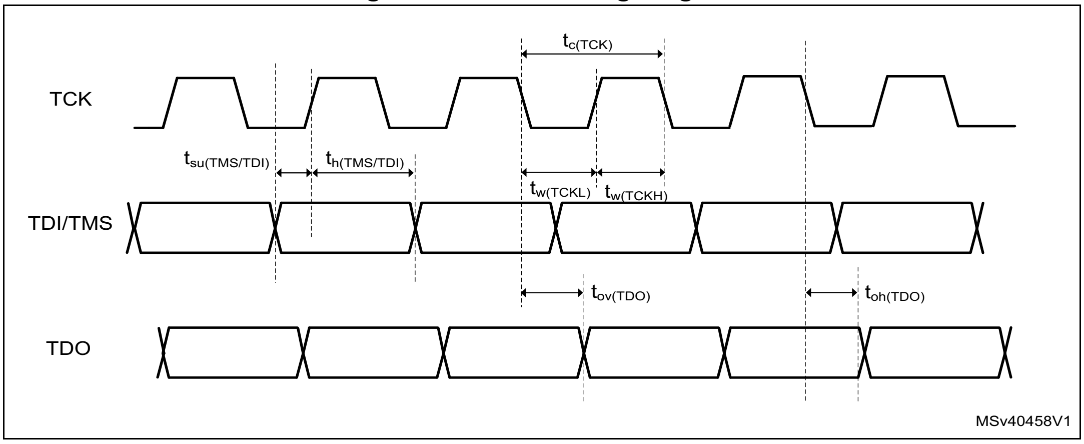
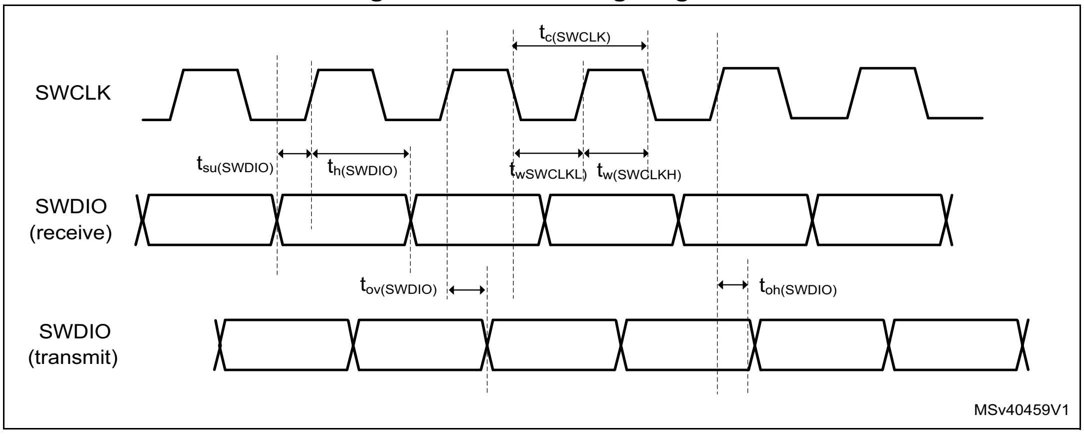


Figure 61. SWD timing diagram

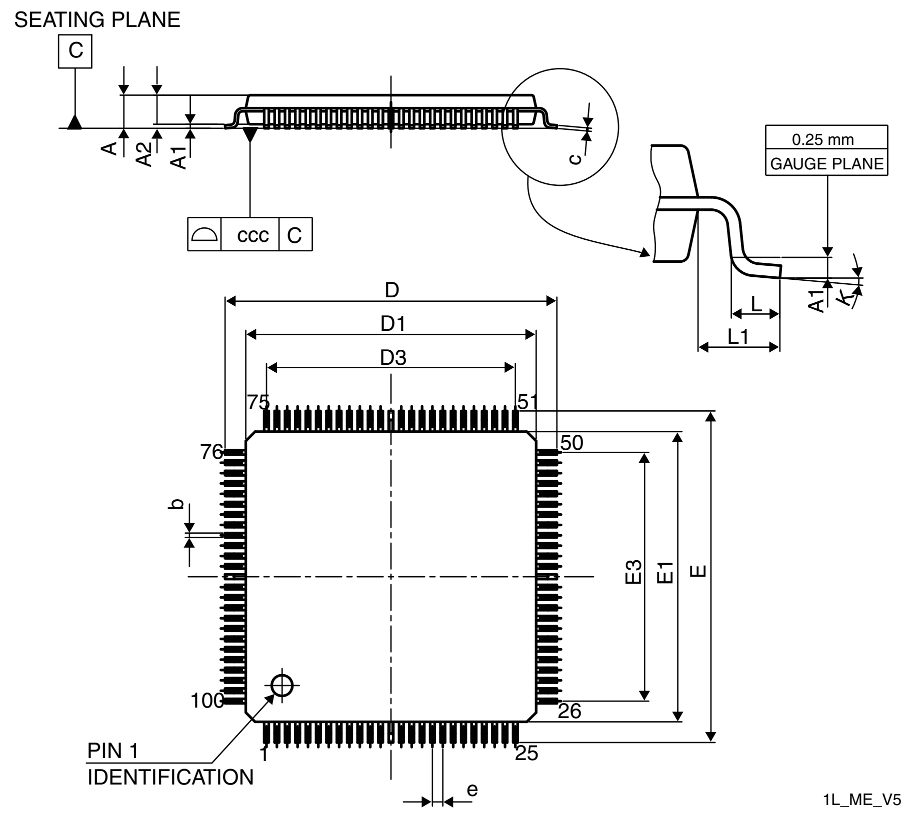


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at www.st.com.* ECOPACK® is an ST trademark.

7.1 LQFP100 package information

Figure 62. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



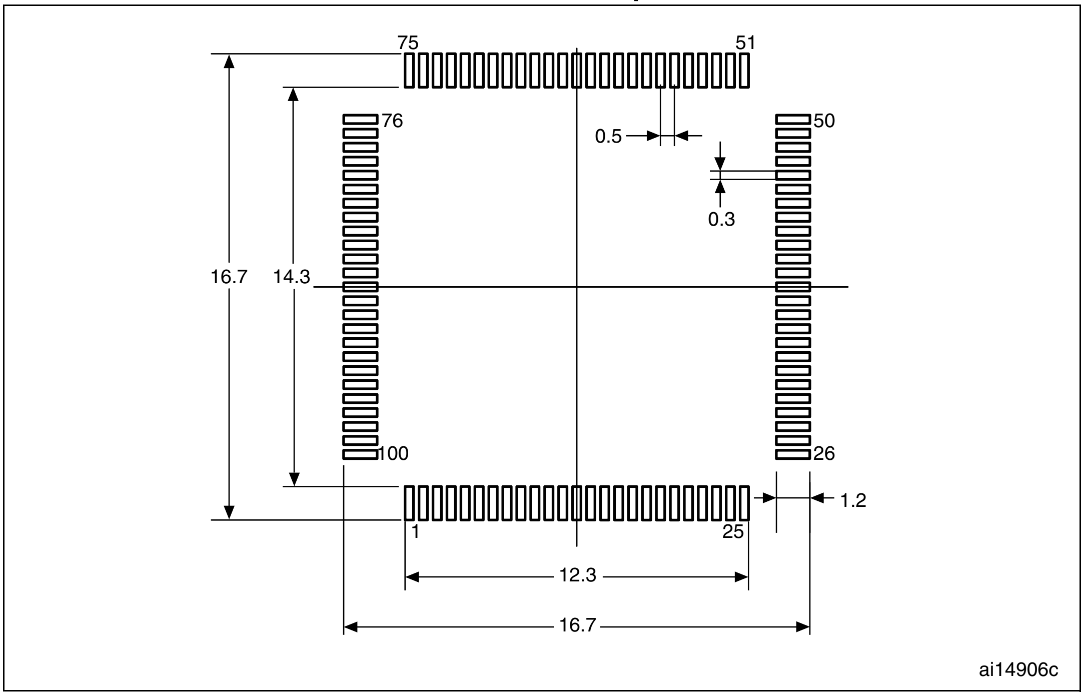
1. Drawing is not to scale.

Table 114. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 63. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



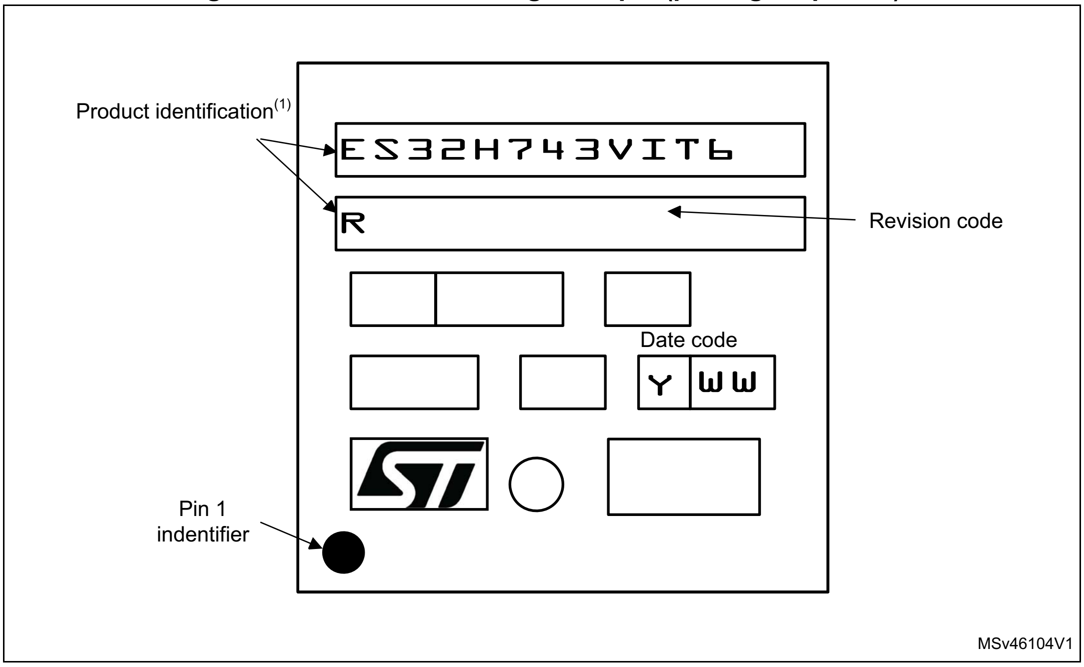
1. Dimensions are expressed in millimeters.*

Device marking for LQFP100

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

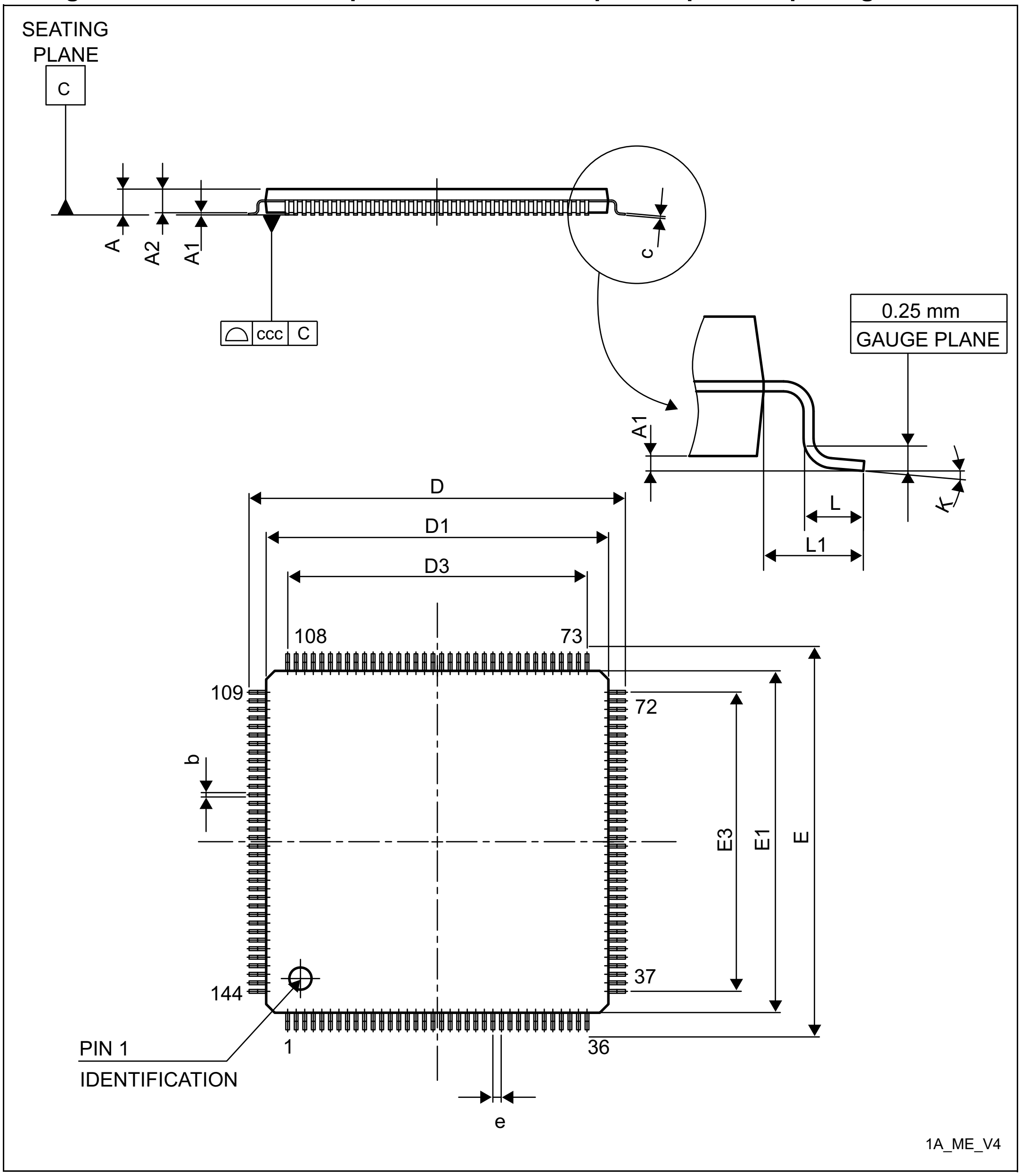
Figure 64. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 LQFP144 package information

Figure 65. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



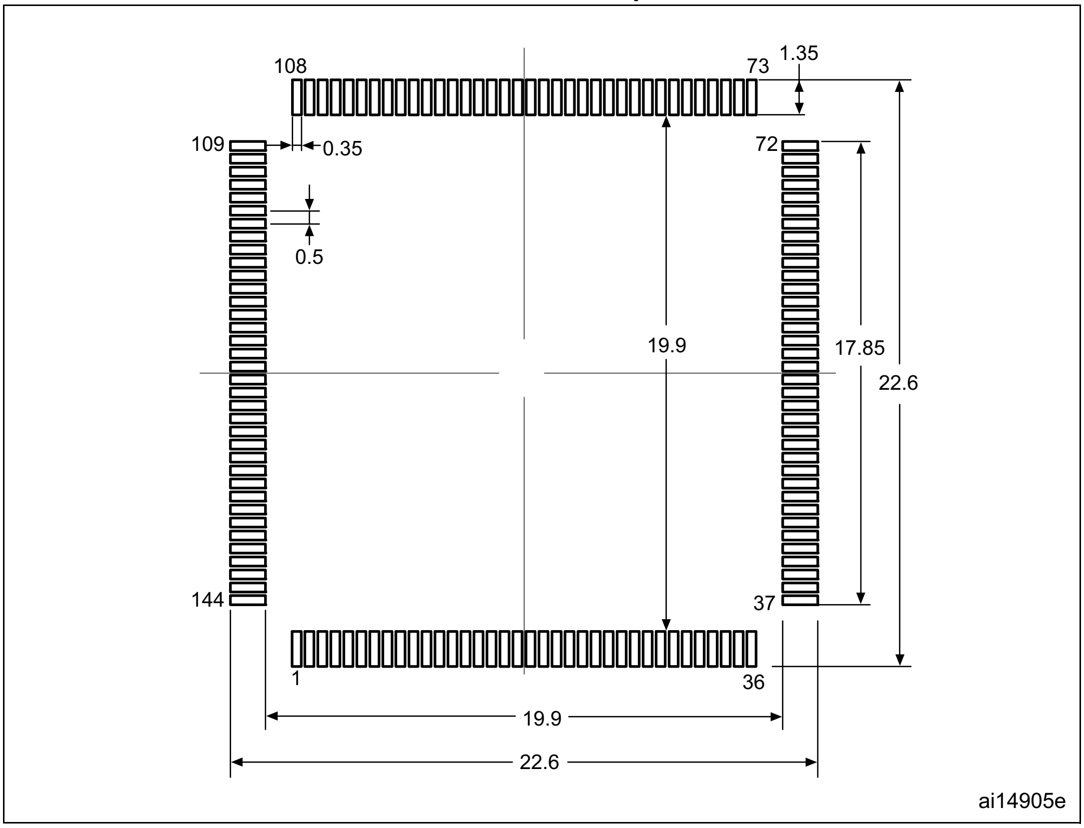
1. Drawing is not to scale.

Table 115. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 66. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



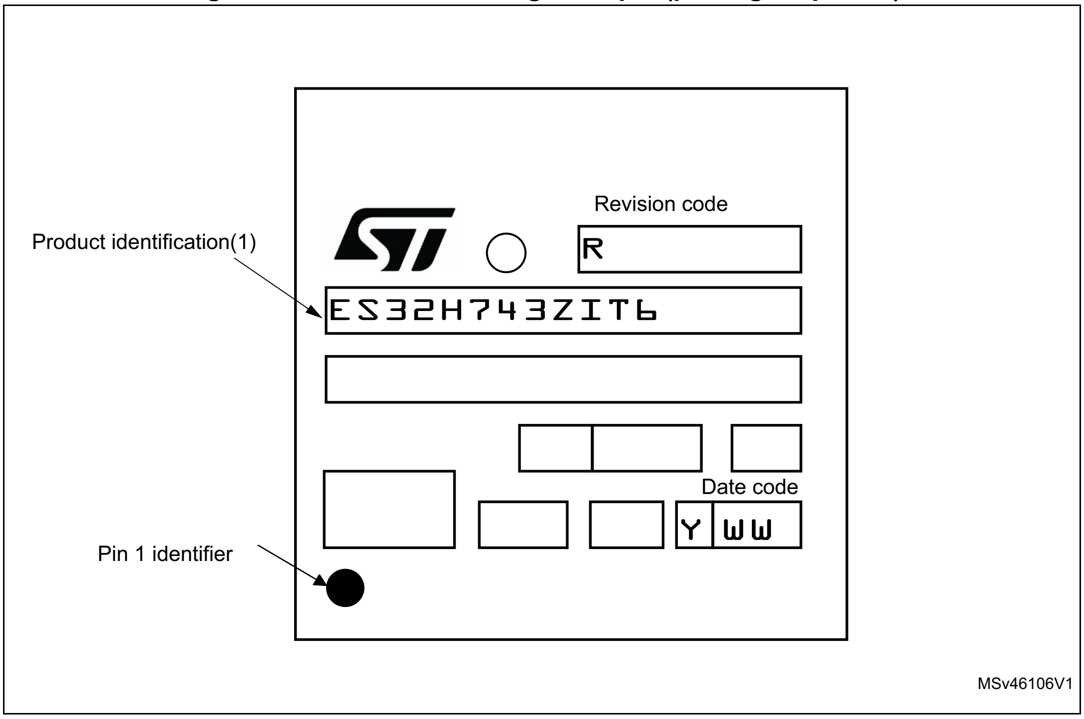
1. Dimensions are expressed in millimeters.

Device marking for LQFP144

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

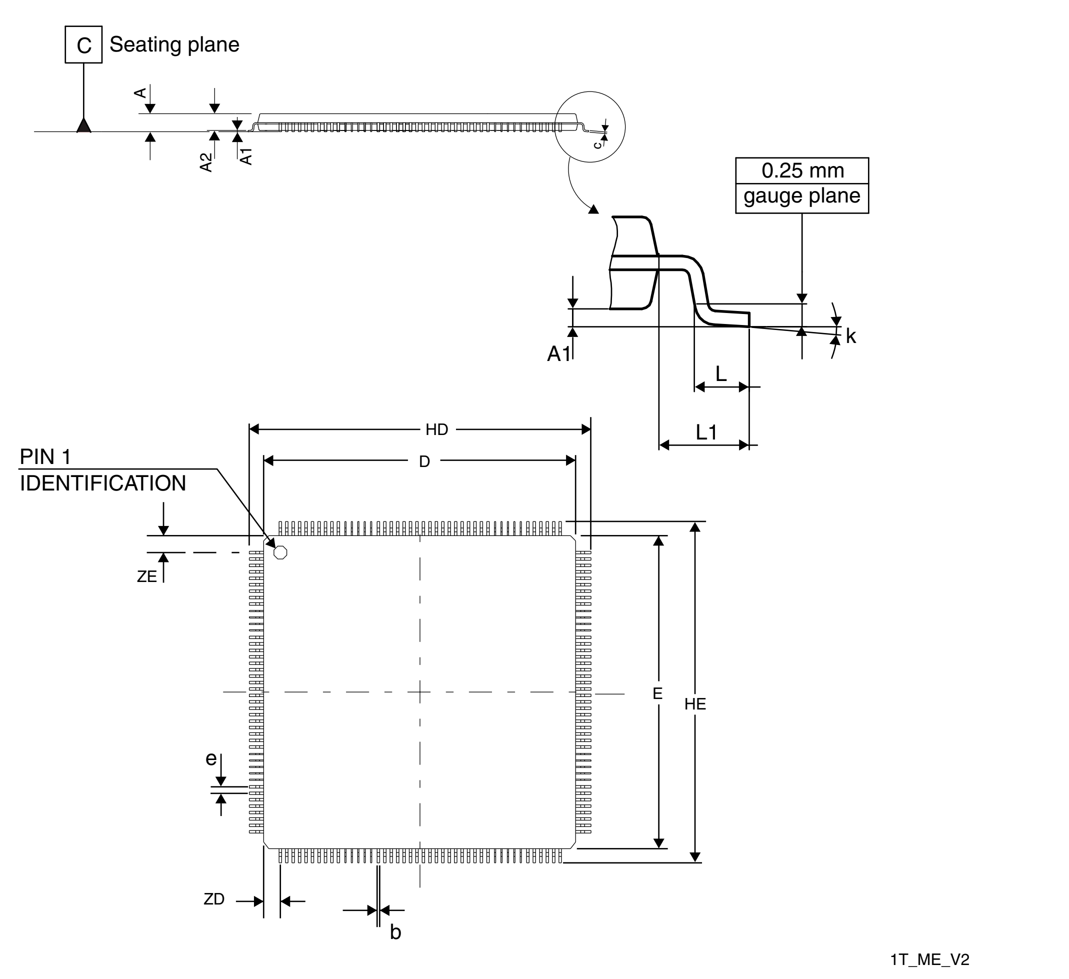
Figure 67. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 LQFP176 package information

Figure 68. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline



1. Drawing is not to scale.

Table 116. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data

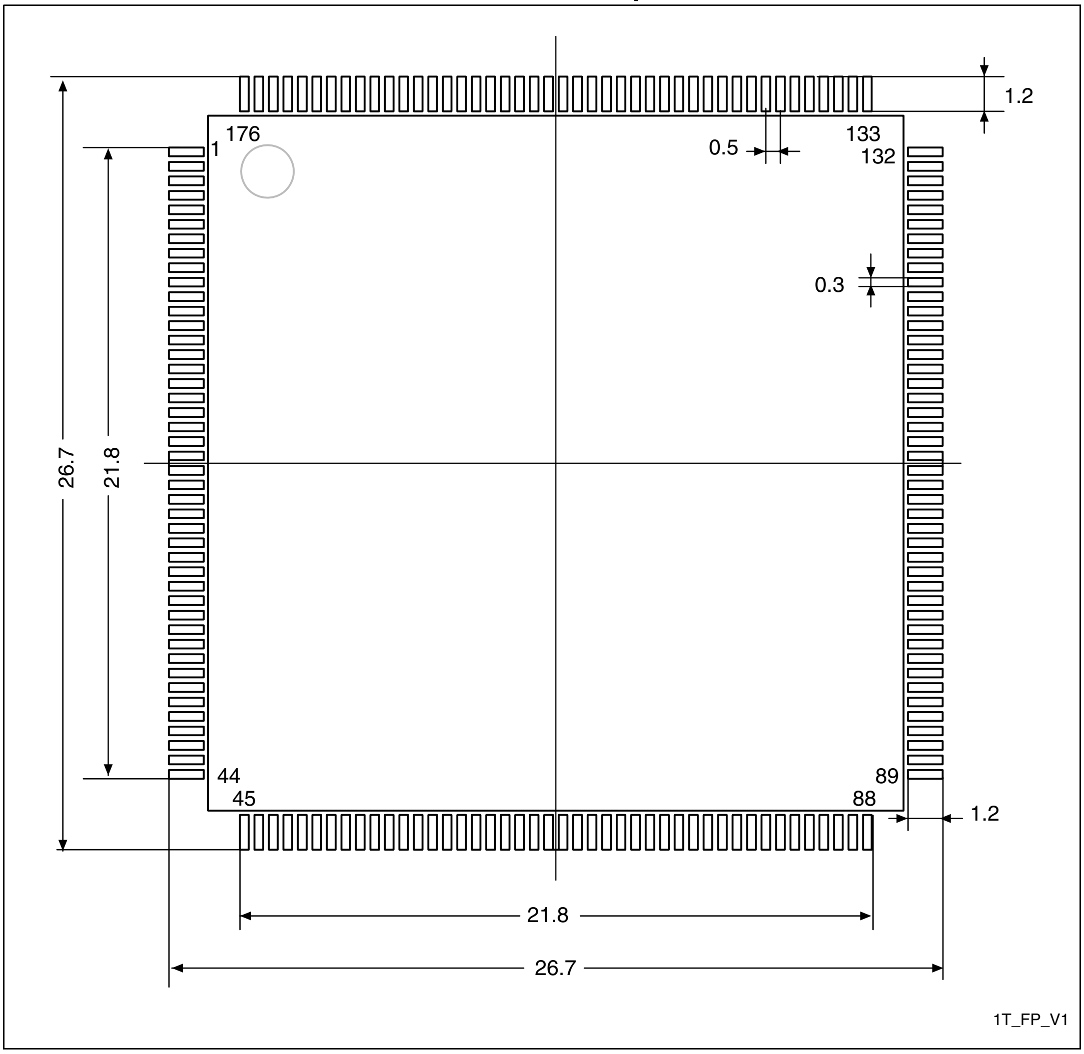
Ref.	Dimensions					
	Millimeters			Inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

Table 116. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data (continued)

Ref.	Dimensions					
	Millimeters			Inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
HD	25.900	-	26.100	1.0197	-	1.0276
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L(2)	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

Figure 69. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package recommended footprint



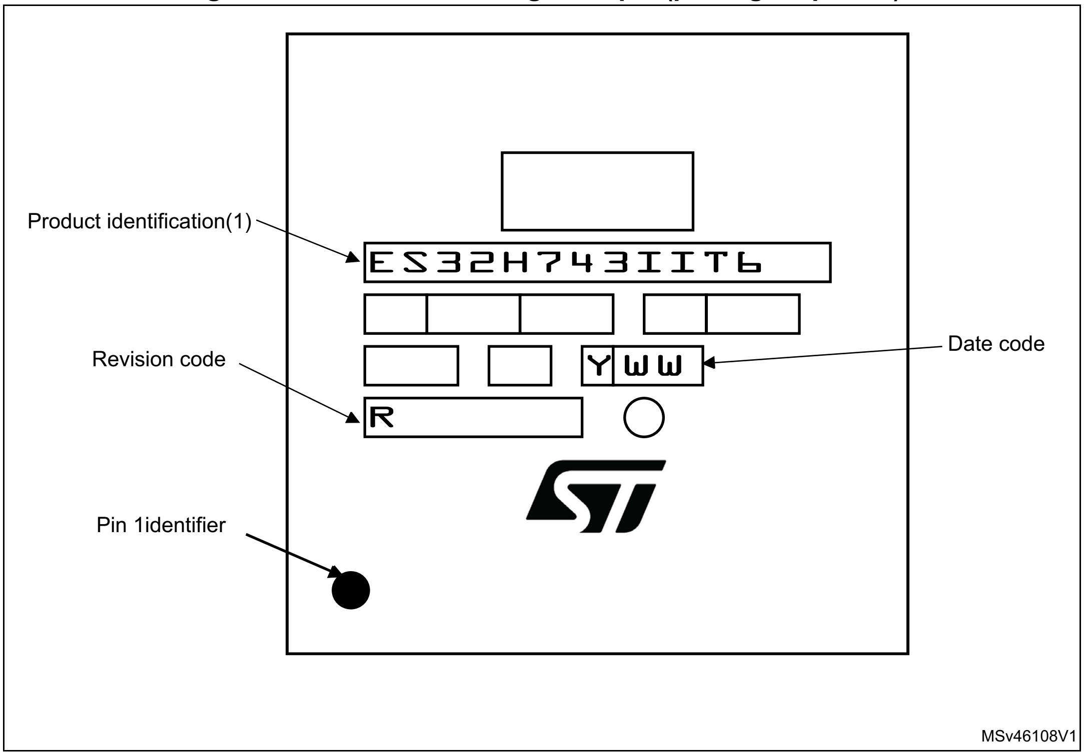
1. Dimensions are expressed in millimeters.

Device marking for LQFP176

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

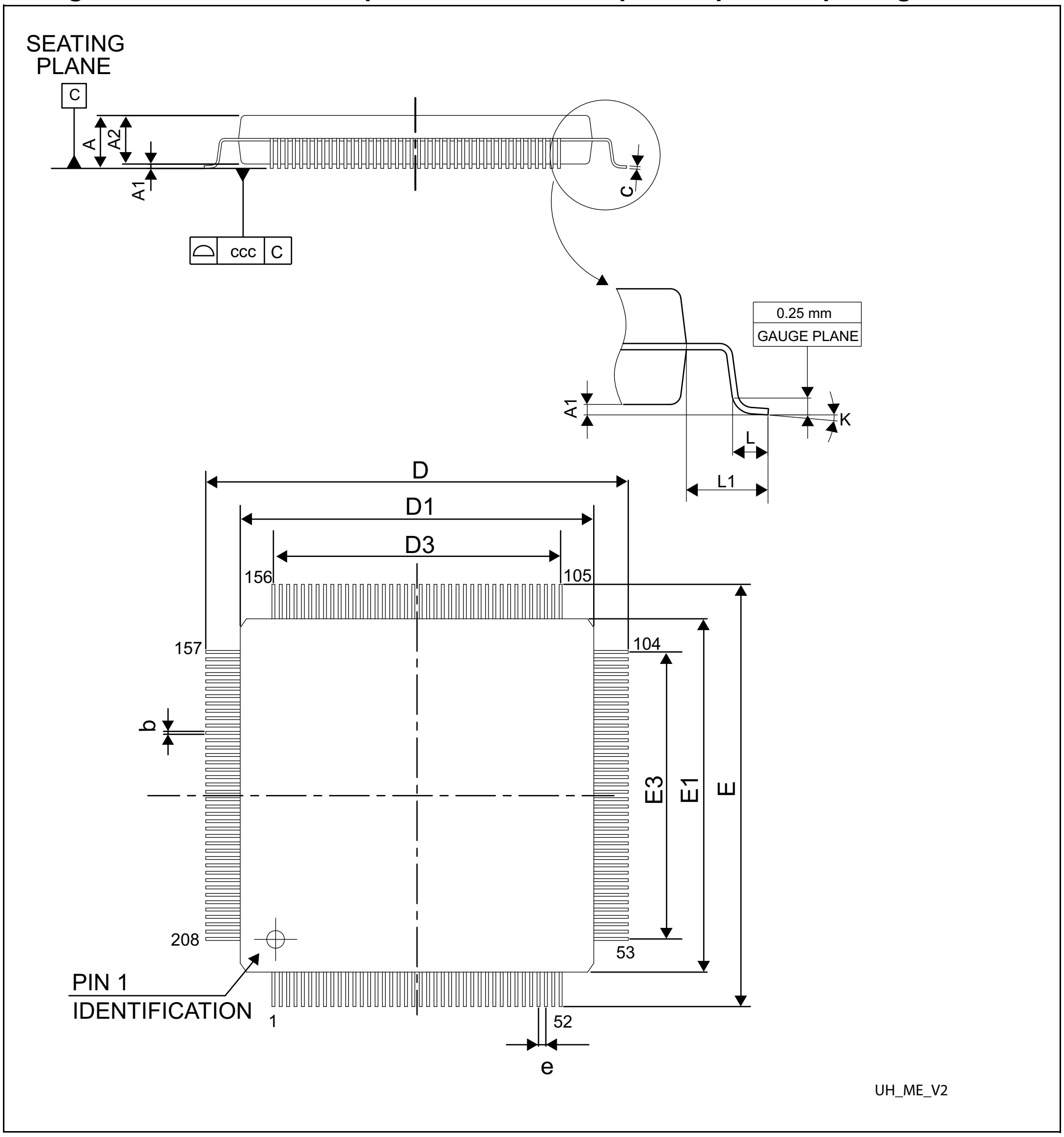
Figure 70. LQFP176 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 LQFP208 package information

Figure 71. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline



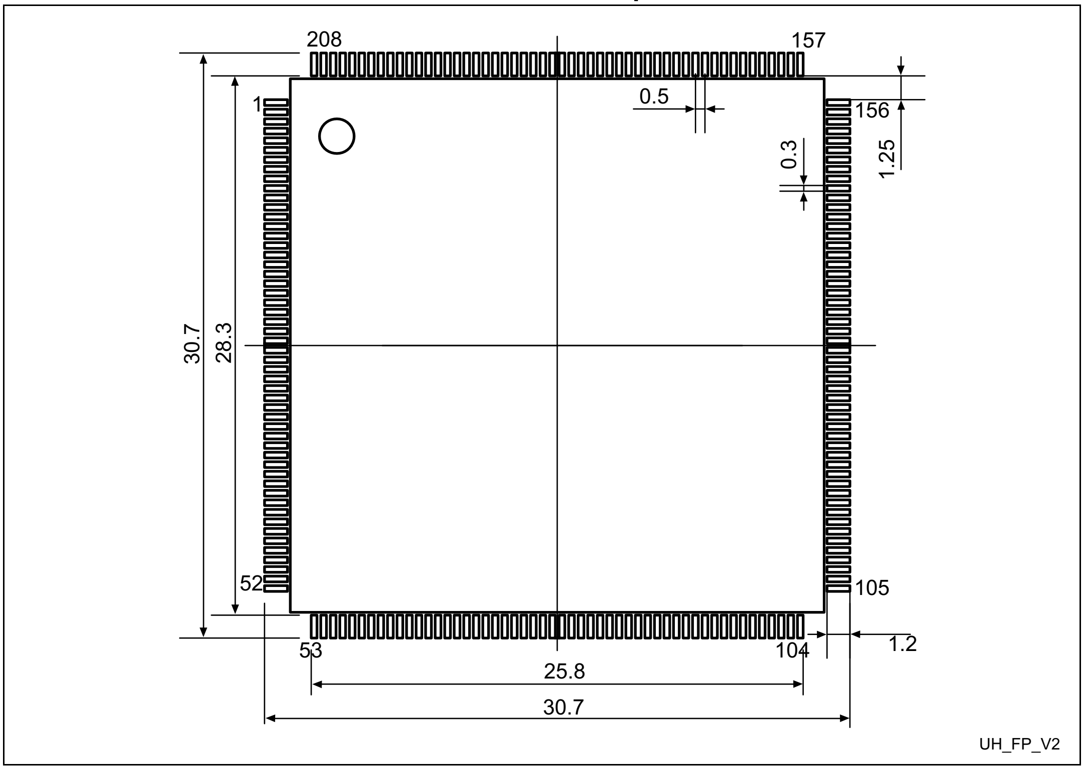
1. Drawing is not to scale.

Table 117. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1811	1.1732	1.1890
D1	27.800	28.000	28.200	1.1024	1.0945	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1811	1.1732	1.1890
E1	27.800	28.000	28.200	1.1024	1.0945	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 72. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package recommended footprint



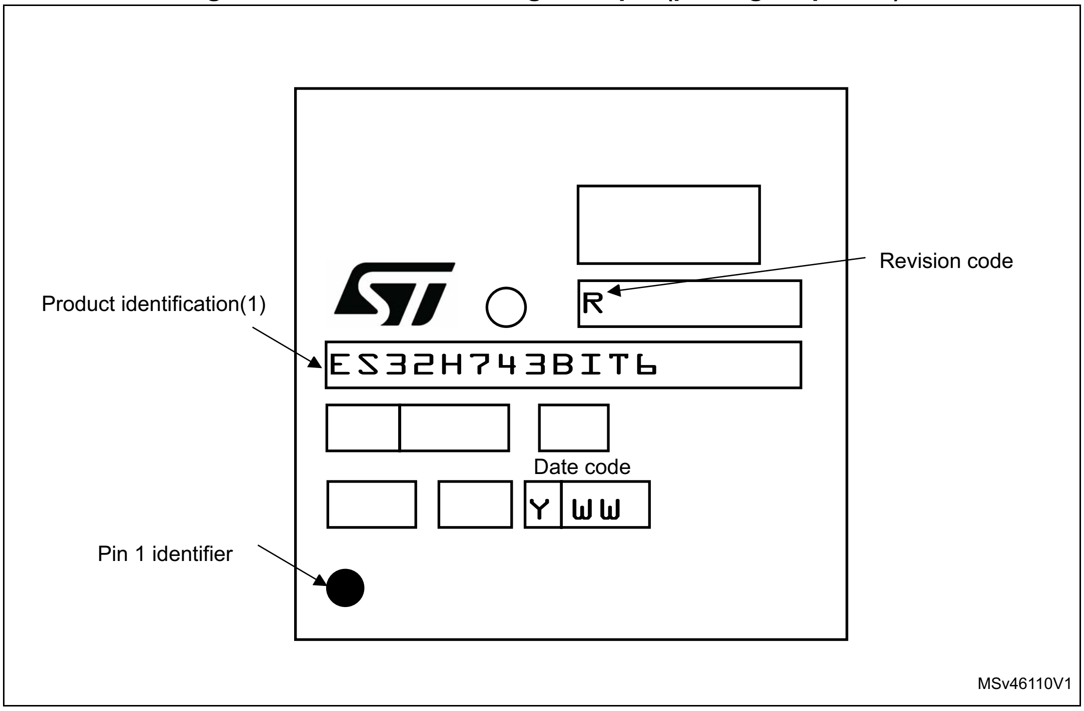
1. Dimensions are expressed in millimeters.

Device marking for LQFP208

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

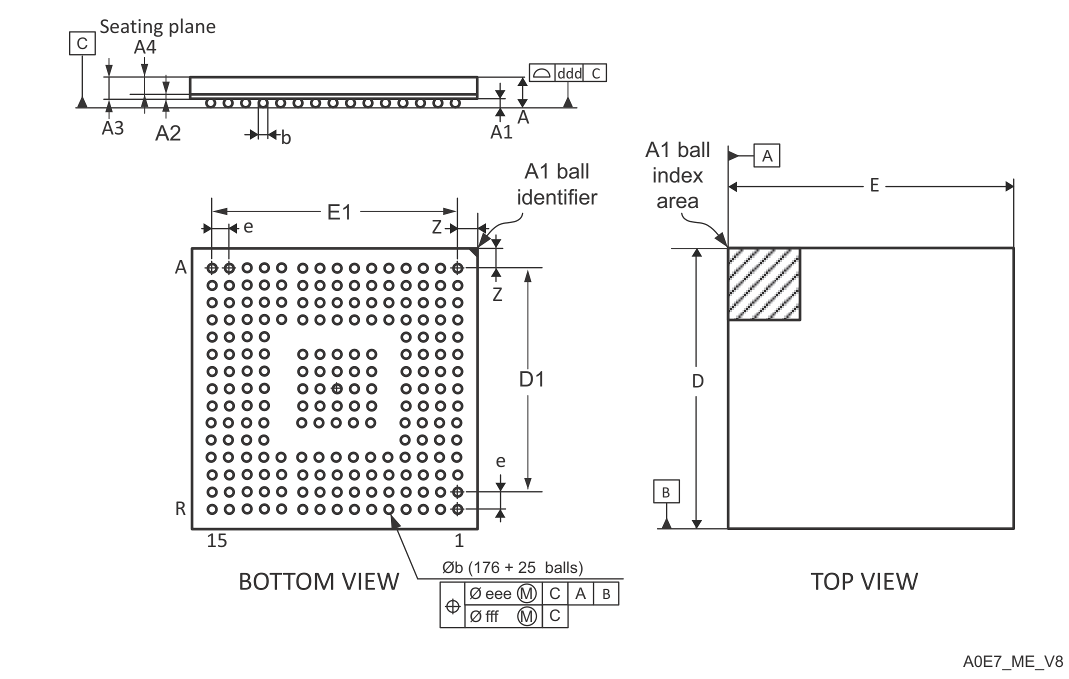
Figure 73. LQFP208 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.5 UFBGA176+25 package information

Figure 74. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 118. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[(1)]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 118. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 75. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint

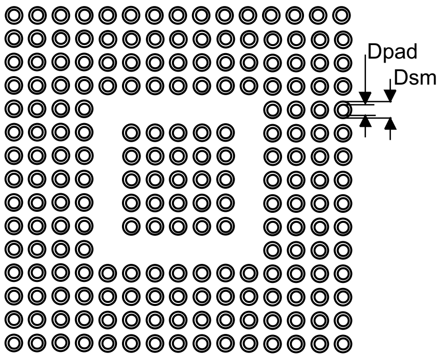


Table 119. UFBGA 176+25 recommended PCB design rules (0.65 mm pitch BGA)

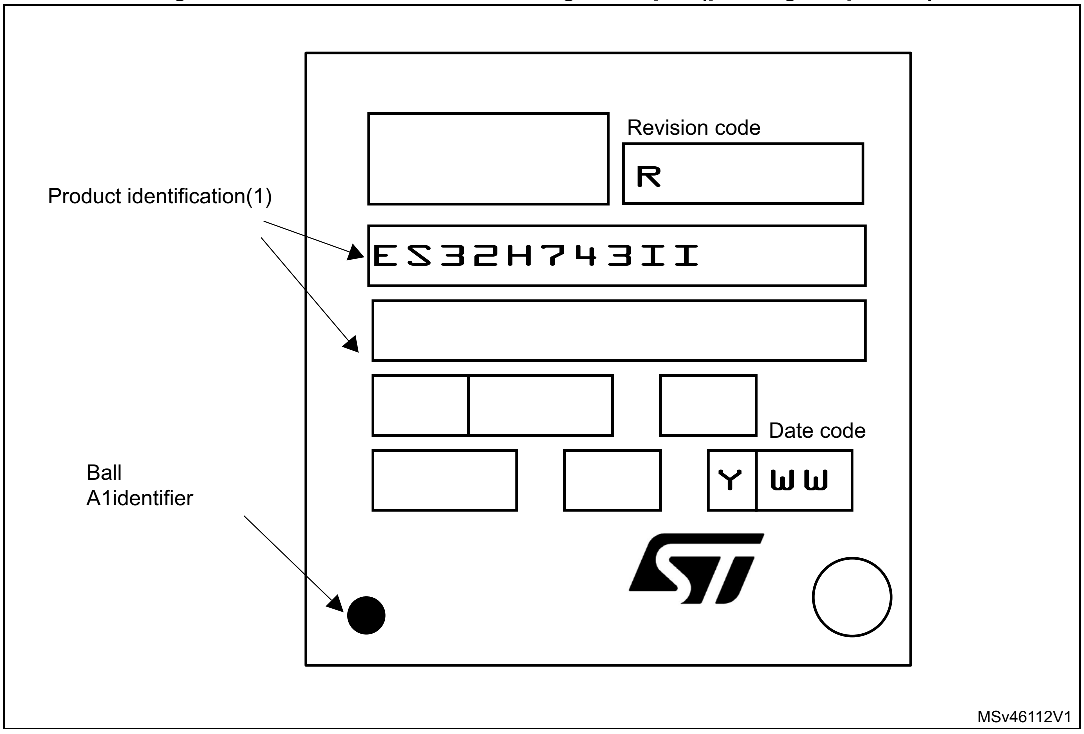
Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Device marking for UFBGA176+25

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 76. UFBGA176+25 marking example (package top view)

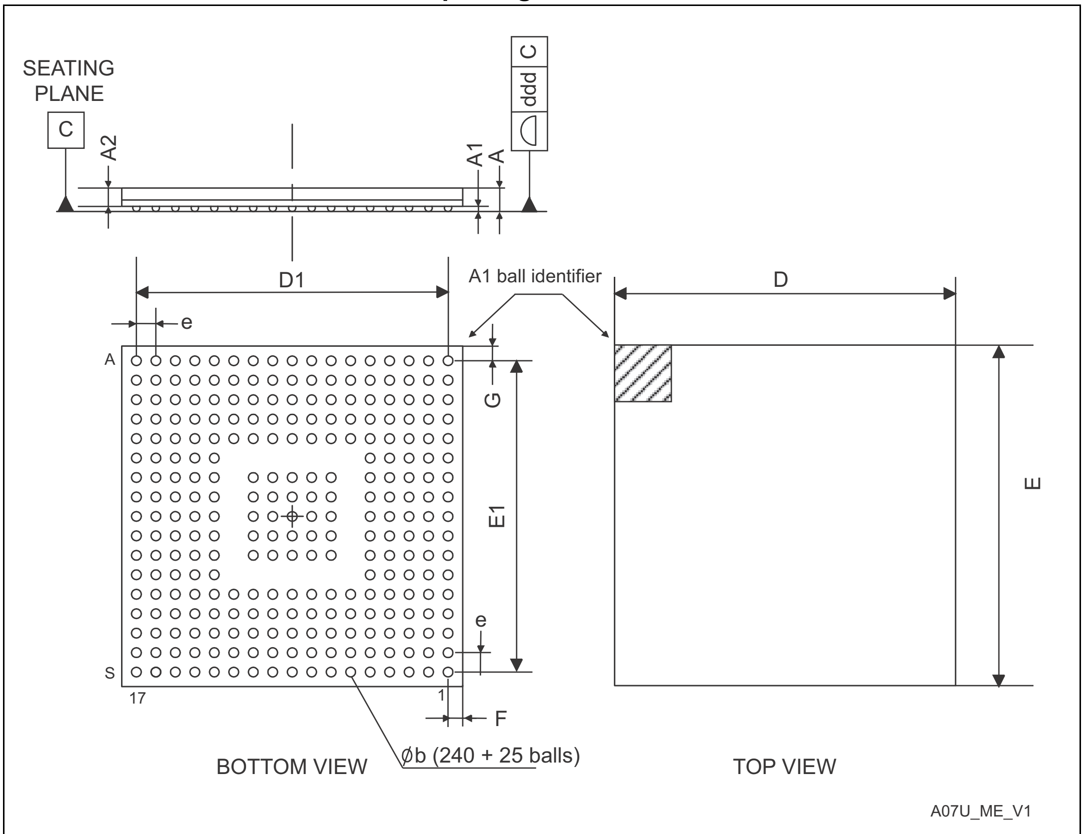


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.6 TFBGA240+25 package information

TFBGA265 package information is preliminary information which are subject to change.

Figure 77. TFBGA240+25 - 265 pin, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array package outline



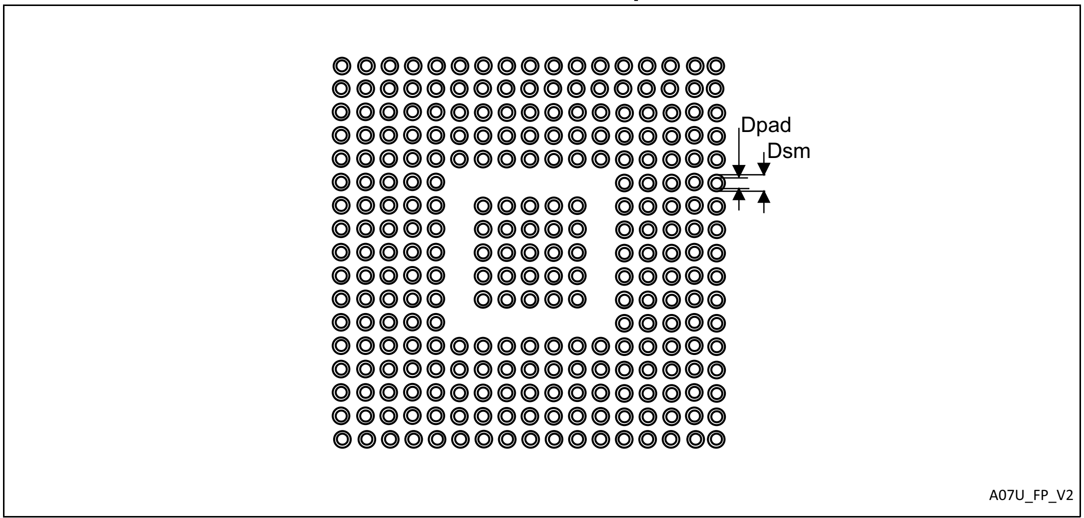
1. Dimensions are expressed in millimeters.

Table 120. TFBGA240+25 - 265 pin, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	13.850	14.000	14.150	0.5453	0.5512	0.5571
D1	-	12.800	-	-	0.5039	-
E	13.850	14.000	14.150	0.5453	0.5512	0.5571
E1	-	12.800	-	-	0.5039	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
G	-	0.600	-	-	0.0236	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 78. TFBGA240+25 - 265 pin pin, 14x14 mm 0.8 mm pitch recommended footprint



1. Dimensions are expressed in millimeters.

Table 121. TFBGA240+25, 265 pin recommended PCB design rules (0.8 mm pitch)

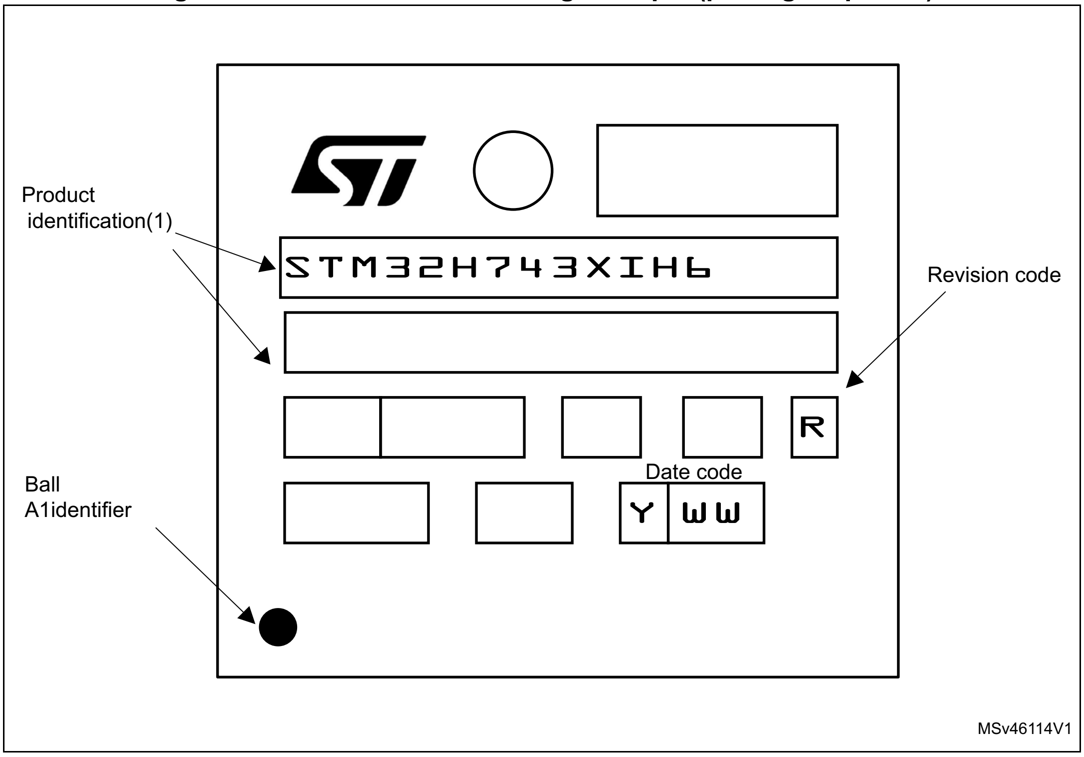
Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for TFBGA240+25

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 79. TFBGA240+25 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 122. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** TFBGA240+25 - 14 x 14 mm / 0.8 mm pitch	40.9	°C/W
	Thermal resistance junction-ambient LQFP208 - 28 x 28 mm /0.5 mm pitch	42.4	
	Thermal resistance junction-ambient LQFP176 - 24 x 24 mm /0.5 mm pitch	43.0	
	Thermal resistance junction-ambient UFBGA176+25 - 10 x 10 mm /0.65 mm pitch	37.4	
	Thermal resistance junction-ambient LQFP144 - 20 x 20 mm /0.5 mm pitch	43.7	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm /0.5 mm pitch	45.0	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

8 Ordering information

Table 123. STM32H743xI ordering information scheme

Example:	STM32	H	743	V	I	T	6	TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

H = High performance

Device subfamily

743 = STM32H7x3 line

Pin count

V = 100 pins

Z = 144 pins

I = 176 pins/balls

B = 208 pins

X = 240 balls

Flash memory size

I = 2 Mbytes

Package

T = LQFP

K = UFBGA pitch 0.65 mm

I = UFBGA pitch 0.5 mm

H = TFBGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Revision history

Table 124. Document revision history

Date	Revision	Changes
22-Jun-2017	1	Initial release.