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230-V, 400-W, 92% High Efficiency Battery Charger With PFC and LLC for 36-V Power Tools Reference Design

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Design Resources

TIDA-00355	Design Folder
UCC28180	Product Folder
UCC25600	Product Folder
UCC27714	Product Folder
UCC28722	Product Folder
TLV70450	Product Folder

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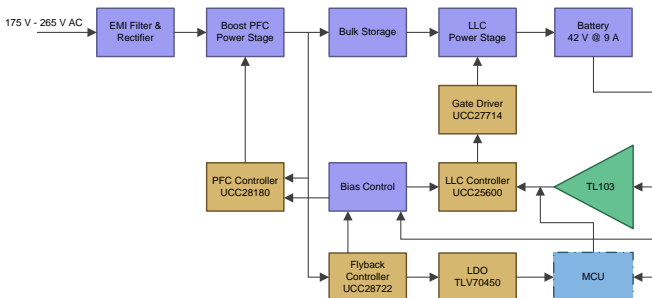
Design Features

- 400-W Battery Charger With Front-End PFC and Half-Bridge LLC Resonant Converter
- Designed to Charge Wide Range of Batteries in the Voltage Range of 20 to 42 V:
  - Li-Ion, Li-Poly, Ni-Cd and Lead-Acid
- Ideal Charger for 10-Cell Li-ion Battery Pack Used in Industrial Power Tools
- Delivers up to 9 A of Continuous Charging Current for Fast Charging of Batteries
- Overall Efficiency of 92% at Full Charging Current of 9 A and 230-V Input, Eliminating the Need for External Cooling
- High Power Factor > 0.99 and Meets PFC Regulations and Current THD as per IEC 61000-3-2 Class A
- Very Low Standby Power of < 200 mW When Battery is Not Connected
- Small PCB Form Factor of 230 × 80 mm Offers Portability in Usage
- Provides Flexibility for Charge Profiling Through an Additional External Microcontroller
- Charger is Protected for Overcurrent and Short Circuit at Output Terminals Ensuring Safety Needs
- Meets the Requirements of Conducted Emissions Standard – EN55011 Class A

Featured Applications

- Cordless Power Tools
- Cordless Garden Tools
- Battery Chargers for
  - Vacuum Cleaner
  - Robotic Mower
  - E-Bike, E-Cycle

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1 Introduction

Power tools are used in various industrial and household applications such as drilling, grinding, cutting, polishing, driving fasteners, various garden tools, and so on. The most common types of power tools use electric motors while some use internal combustion engines, steam engines, or compressed air.

Power tools can be either corded or cordless (battery-powered). Corded power tools use the mains power (the grid power) to power up the AC or DC motors. The cordless tools use battery power to drive DC motors. Most of the cordless tools use lithium-ion batteries, the most advanced in the industry. Lithium-ion batteries have high energy density, low weight, and greater life. These batteries have relatively low self-discharge (less than half that of nickel-based batteries) and can provide a very high current for applications like power tools. Cordless tools use brushed or BLDC motors. The brushless motors are more efficient and have less maintenance, low noise, and longer life.

This reference design is a complete battery charger for charging batteries used in battery-powered garden and power tools rated up to 400 W. The design can be used to charge Li-ion and Li-poly chemistry batteries with a voltage range from 36 to 42 V and maximum charging current of 9 A. The charger provides constant voltage and constant current controls with settable configuration as per charging requirements.

Power tool chargers have requirements of high efficiency at maximum charging current and low standby requirements when battery is not connected. This design demonstrates the high performance charging power stage in a small form factor (230 × 80 mm), operating from 175-V to 265-V AC and delivers up to 9-A continuous current output to charge battery at greater than 90% efficiency. The design meets low standby power of < 200 mW when battery is not connected. The design also provides flexibility for battery voltage and current level setting for charge profiling, through an additional external microcontroller.

2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
Input voltage range	175-V to 265-V AC
Output voltage	42 V ±2%, 0- to 9-A output current
Output current	9 A ±5%, 20- to 42-V output voltage
Board form factor	230 × 80 mm
Expected efficiency	> 90% at 230 V and full load
Standby power	< 500 mW at 230 V without battery connected on output
Power line harmonics	As per IEC61000-3-2
Conducted emissions	As per EN55022 Class A
Auxiliary power for MCU	5 V at 100 mA
Output voltage ripple	±1 V
Output current ripple	±0.5 A

www.ti.com										System Description

3   System Description

The design is a 42-V, 400-W battery charger power supply with boost PFC pre-regulator using UCC28180 as PFC controller and the main converter stage is realized using LLC configuration with UCC25600 as LLC controller and UCC27714 as gate driver. Internal auxiliary power supply for biasing controllers is implemented using simple low cost flyback controller UCC28722. The system design is done to meet high efficiency, low EMI, and low standby power consumption specifications.

The charger is designed for input voltage range of 175-V to 265-V AC and used to charge batteries up to 36 V at maximum current of 9 A. The design form factor (230 × 80 mm) is compact for the power level of 400 W. The design has an operating efficiency of around 92% at full load, with voltage and current regulation within ±3%.

The EMI filter at the front end of the circuit is designed to meet EN55022 Class-A conducted emission levels. This is followed by an active boost PFC stage operating in continuous conduction mode (CCM). This PFC stage regulates the DC bus voltage to 400 V, stabilized against line drop-outs with a bulk storage capacitor. The isolated power stage of the charger is an LLC-resonant converter operating very close to resonant frequency at full load. The operation will move to above resonance with lighter loads in both constant voltage and constant current regions of the charger. The constant current/constant voltage (CV/CC) feedback is achieved using the TL103W, which has an integrated dual op-amp and a 2.5-V reference. The system is designed to meet below 200 mW of standby power when no battery is connected. This goal is achieved by using a simple logic circuit that disables PFC and LLC power stages when battery is not present.

The ultra-low-cost flyback bias power supply is built using UCC28722 with a BJT as the switching element, resulting in very minimal cost impact. This bias power supply also provides the power needed for an external MCU, which can be optionally added as an add-on card to control the charging profile more precisely.

Various parameters of the design like regulation, efficiency, EMI signature, output ripple, startup, and switching stresses were tested and documented.

TIDU789C–March 2015–Revised January 2017   *230-V, 400-W, 92% High Efficiency Battery Charger With PFC and LLC for*   3
Submit Documentation Feedback   *36-V Power Tools Reference Design*
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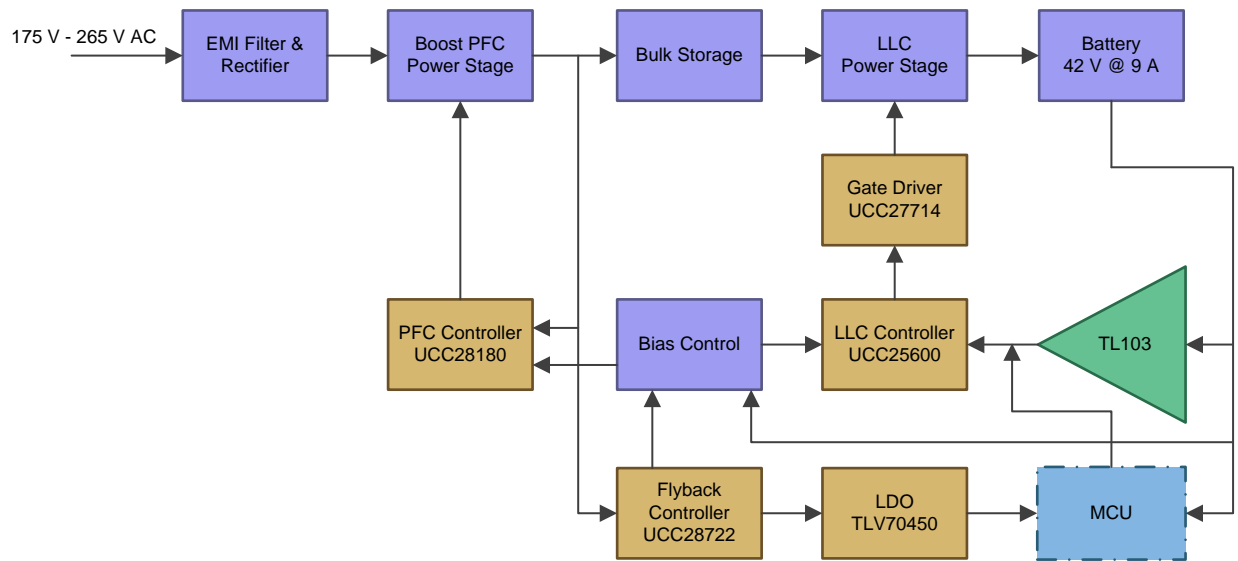
4 Block Diagram

Figure 1. Block Diagram of 400-W Power Supply With PFC and LLC

4.1 Highlighted Products and Key Benefits for 400-W Charger

The following are the highlighted products used in this reference design. Key features for selecting the devices for this reference design are elucidated in the following sections. Complete details of the highlighted devices can be referred in respective product datasheets.

4.1.1 UCC28180 – PFC Controller

To implement the high performance, small form factor PFC design at 400-W power, the UCC28180 is preferred controller as it offers series of benefits to address the next generation needs of low THD norms for power tools.

The UCC28180 is an extremely high performance, CCM compact, 8-pin programmable frequency PFC controller. Its wide and programmable operating frequency provides flexibility to design at a high frequency optimizing the components. Its trimmed current loop circuits helps achieve less than 5% THD from medium-to-full load (50 to 100%). Its reduced current sense threshold helps utilize a 50% smaller shunt resistor, resulting in lower power dissipation while maintaining low THD. Its integrated fast gate driver of 2-A/1.5-A drive current eliminates the need for an external gate driver.

The UCC28180 also has a complete set of system protection features such as soft overcurrent, cycle-by-cycle current limit, output overvoltage protection, VCC UVLO, and open pin protections (ISENSE, VSENSE). These features greatly improve reliability and further simplifies the design.

4.1.2 UCC25600 — LLC Controller

Power tool designs demand high frequency DC/DC conversion and high efficiency with small form-factor. The UCC25600 LLC controller is best fit for high wattage resonant power design as it offers all the key advantages for high performance and high efficiency DC/DC conversion at high power levels.

The UCC25600 is a simple 8-pin resonant mode controller designed for offline DC/DC applications. The UCC25600 controller works in the LLC resonant half bridge topology and operates with zero voltage switching (ZVS) to provide highly efficient voltage conversion operation, which nearly eliminates all switching losses. This controller uses frequency modulation control has programmable dead-time control with a precision 50-ns set point accuracy and tight tolerances on the frequency, which reduces the need for over-design saving system cost. The UCC25600 also has as complete set of system protection features such as overcurrent, over temperature and bias voltage OVP and UVLO, which greatly improves reliability and further simplifies the design. Its unique programmable independent minimum and maximum switching frequency settings prevents ZCS region operation and limits switching loss at light load condition. Its integrated burst mode operation helps maintain regulation at light load and no load conditions.

4.1.3 UCC27714 — Gate Driver

LLC converter implementation needs driving of two MOSFETs operated in half bridge configuration. The UCC27714 offers all the key features as needed for half-bridge LLC implementation. Its high operating voltage range up to 600 V, and 4-A driving currents helps in simple implementation of LLC half-bridge driver circuitry. Its best-in-class propagation delay (90 ns typ.) and delay matching (20 ns max.) between channel helps in minimizing pulse distortion in high frequency LLC applications.

4.1.4 UCC28722 — Flyback Controller

To achieve very low power consumption and optimize board space for the auxiliary power supply needs, the UCC28722 meets the bias supply needs. The main value of the UCC28722 solution is reduced total cost. The design offers advantage of elimination of feedback components and its increasing switching frequency and increasing the VDD range aids in the reduction in size of power stage components. In addition, this solution allows to easily meet <50-mW standby power at the lowest system solution cost.

5 System Design Theory

This reference design provides 400 W of power from a 230-V AC input with power factor correction. This design is intended for operation at country specific line voltages between 175-V to 265-V AC. The UCC28180 controls a PFC boost front end, while the UCC25600 LLC-resonant half-bridge converts the PFC output to isolated 42 V and 9 A. The total system efficiency is 92% with a 230-V AC input and over 90% with a 175-V AC input with full load. In addition, several protections are embedded into this design which includes input under-voltage protection and output short circuit protection.

Low EMI, high efficiency, high power factor, and a reliable power supply are the main focuses of this design for targeted applications.

5.1 PFC Regulator Stage Design

Power factor correction shapes the input current of the power supply to maximize the real power available from the mains. In addition, it is important to have PFC to comply with low harmonic (low THD) regulatory requirements such as IEC61000-3-2. Currently, two modes of operation have been widely utilized for PFC implementations. For higher power circuits, the topology of choice is the boost converter operating in CCM and with average current mode control. For lower power applications, typically the critical conduction mode (CrCM) boost topology is used.

For high power levels such as 400 W, it is advisable to use CCM operation as it has lower peak and RMS currents. Lower currents significantly reduce the stress in power MOSFET, diode, and inductor. In addition, the filtering is easier as the current through the boost inductor is more continuous. Finally, the switching frequency remains constant for the CCM operation, so the boost inductor design and EMI filter designs are easier.

The UCC28180 operates at fixed frequency in CCM and requires minimal external components for high wattage PFC pre-regulator implementation. The design process and component selection for this design are illustrated below. All design calculations are available in the Excel® file "TIDA00355_PFC.xls" available at http://www.ti.com/tool/TIDA-00355.

5.1.1 Circuit Component Design

5.1.1.1 Design Parameters

Table 2. Design Parameters for PFC Power Stage Design

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{IN}	Input voltage	175		265	V AC
f_{LINE}	Input frequency	47		63	Hz
OUTPUT					
V_{OUT}	Output voltage		397		V DC
P_{OUT}	Output power			400	W
	Line regulation			5%	
	Load regulation			5%	
PF	Targeted power factor		0.99		
η	Targeted efficiency		96%		

5.1.1.2   Current Calculations

The input fuse, bridge rectifier, and input capacitor are selected based upon the input current calculations. First, determine the maximum average output current, $I_{OUT(max)}$:

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT}}$$

$$I_{OUT(max)} = \frac{400}{397} = 1.0\,A \tag{1}$$

The maximum input RMS line current, $I_{IN\_RMS(max)}$, is calculated using the parameters from Table 2 and the efficiency and power factor initial assumptions:

$$I_{IN\_RMS(max)} = \frac{P_{OUT(max)}}{\eta \times V_{IN(min)} \times PF}$$

$$I_{IN\_RMS(max)} = \frac{400}{0.96 \times 175 \times 0.99} = 2.41\,A \tag{2}$$

$$I_{RIPPLE} = \Delta I_{RIPPLE} \times I_{IN(max)}$$

$$I_{RIPPLE} = 0.3 \times (\sqrt{2} \times 2.41) = 1.02\,A \tag{3}$$

Assuming ripple to be 1.5%,

$$V_{IN\_RIPPLE} = \Delta V_{RIPPLE\_IN} \times V_{IN\_RECTIFIED(min)}$$

$$V_{IN\_RIPPLE} = 0.015 \times (\sqrt{2} \times 175) = 3.71\,V \tag{4}$$

The recommended value for the input X-capacitor can now be calculated:

$$C_{IN} = \frac{I_{RIPPLE}}{8 \times f_{sw} \times V_{IN\_RIPPLE}}$$

$$C_{IN} = \frac{1.02}{8 \times 98 \times 7.43} = 0.360\,\mu F \tag{5}$$

A standard value 0.47-μF X2 film capacitor is used.

5.1.1.3   Boost Inductor

The duty cycle of operation is a function of the rectified input voltage and will be continuously changing over the half-line cycle. The duty cycle, $DUTY_{(max)}$, can be calculated at the peak of the minimum input voltage:

$$DUTY_{(max)} = \frac{V_{OUT} - V_{IN\_RECTIFIED(min)}}{V_{OUT}}$$

$$DUTY_{(max)} = \frac{397 - (1.414 \times 175)}{397} = 0.377 \tag{6}$$

The minimum value of the boost inductor is calculated based upon the acceptable ripple current, I_{RIPPLE}, at a worst case duty cycle of 0.377:

$$L_{BST(min)} \geq \frac{V_{OUT} \times D \times (1-D)}{f_{sw} \times I_{RIPPLE}}$$

$$L_{BST(min)} \geq \frac{397 \times 0.377 \times (1-0.377)}{(98 \times 1.02)} = 932\,\mu H \tag{7}$$

The actual value of the boost inductor used is 1000 μH.

5.1.1.4 Output Capacitor

The output capacitor, C_{OUT}, is sized to meet holdup requirements of the converter. Assuming the downstream converters require the output of the PFC stage to never fall below 280 V, $V_{OUT\_HOLDUP(min)}$, during one line cycle, $t_{HOLDUP} = 1/f_{LINE(min)}$, the minimum calculated value for the capacitor is:

$$C_{OUT(min)} \geq \frac{2 \times P_{OUT(max)} \times t_{HOLDUP}}{V_{OUT}^2 - V_{OUT\_HOLDUP(min)}^2}$$

$$C_{OUT(min)} \geq \frac{2 \times 400 \times 20 \text{ ms}}{(397^2 - 280^2)} = 202 \text{ } \mu F$$

(8)

The capacitor of 220 μF is selected, considering the capacitor tolerances.

5.1.1.5 Switching Element

The drain to source RMS current, I_{DS_RMS} through switching FET is calculated as

$$I_{DS\_RMS} = \frac{P_{OUT(max)}}{V_{IN\_RECTIFIED(min)}} \times \sqrt{2 - \frac{16 \times V_{IN\_RECTIFIED(min)}}{3 \times \pi \times V_{OUT}}}$$

$$I_{DS\_RMS} = \frac{400}{247} \times \sqrt{2 - \left(\frac{16 \times 247}{3 \times \pi \times 397}\right)} = 1.57 \text{ A}$$

(9)

An AOTF12T50P MOSFET of 500 V/12 A is selected for the current design. Consider using a higher voltage rating FET (600 V/650 V) based on the design de-rating needs of the end equipment.

The conduction losses of the switch MOSFET in this design are estimated using the $R_{DS(on)}$ at 100°C, found in the device datasheet, and the calculated drain to source RMS current, I_{DS_RMS}:

$$P_{COND} = I_{DS\_RMS}^2 \times R_{DS(on)}$$

$$P_{COND} = 1.568^2 \times (0.7) = 1.73 \text{ W}$$

(10)

The switching losses are estimated using the rise time, t_r, and fall time, t_f, of the MOSFET gate, and the output capacitance losses (C_{OSS}).

$$P_{SW} = f_{SW} \left[0.5 \times V_{OUT} \times I_{IN(max)} \times (t_r + t_f) + 0.5 \times C_{OSS} \times V_{OUT}^2 \right]$$

$$P_{SW} = 98 \times \left[0.5 \times 397 \times 3.4 \times (12 \text{ ns} + 6 \text{ ns}) + 0.5 \times 68 \text{ pF} \times 397^2 \right] = 1.71 \text{ W}$$

(11)

Total FET losses:
$$P_{COND} + P_{SW} = 1.73 + 1.71 = 3.44 \text{ W}$$

(12)

An appropriately sized heat sink is used for MOSFET.

5.1.1.6 Boost Diode

The output diode should have a blocking voltage that exceeds the output over voltage of the converter and average current same as $I_{OUT(max)}$. BYV25FX-600, a 600-V/5-A diode, is selected as output diode.

The diode losses are estimated based upon the forward voltage drop, V_F, at 125°C and the reverse recovery charge, Q_{RR}, of the diode:

$$P_{DIODE} = V_{F\_125C} \times I_{OUT(max)} + 0.5 \times f_{SW} \times V_{OUT} \times Q_{RR}$$

$$P_{DIODE} = 1.5 \times 1.0 + 0.5 \times 98 \times 397 \times 13 \text{ nC} = 1.75 \text{ W}$$

(13)

5.1.1.7   Sense Resistor

To accommodate the gain of the non-linear power limit, the sense resistor, R_{SENSE}, is sized such that it triggers the soft overcurrent at 10% higher than the maximum peak inductor current using the minimum soft over current threshold of the ISENSE pin, V_{SOC}, of ISENSE equal to 0.265 V.

$$R_{SENSE} = \frac{V_{SOC(min)}}{I_{L\_PEAK(max)} \times 1.1}$$

$$R_{SENSE} = \frac{0.259\ V}{3.91\ A \times 1.1} = 0.06\ \Omega \tag{14}$$

R_{SENSE} selected is 0.05 Ω.

The power dissipated across the sense resistor, P_{RSENSE}, must be calculated:

$$P_{RSENSE} = I_{IN\_RMS(max)}^2 \times R_{SENSE}$$

$$P_{RSENSE} = 2.41^2 \times 0.05 = 0.29\ W \tag{15}$$

The peak current limit, PCL, protection feature is triggered when current through the sense resistor results in the voltage across R_{SENSE} to be equal to the V_{PCL} threshold. For a worst case analysis, the maximum V_{PCL} threshold is used:

$$I_{PCL} = \frac{V_{PCL(max)}}{R_{SENSE}}$$

$$I_{PCL} = \frac{0.438\ V}{0.05} = 8.76\ A \tag{16}$$

To protect the ISENSE pin from inrush-surge current, a 220-Ω resistor, R_{ISENSE}, is placed in series with the ISENSE pin. A 1000-pF capacitor is placed close to the device to improve noise immunity on the ISENSE pin.

5.1.1.8 Output Voltage Set Point

For low power dissipation and minimal contribution to the voltage set point, 9.96 MΩ is used for the top voltage feedback divider resistor, R_{FB1}. Multiple resistors in series are used due to the maximum allowable voltage across each. Using the internal 5-V reference, V_{REF}, the bottom divider resistor, R_{FB2}, is selected to meet the output voltage design goals.

$$R_{FB2} = \frac{V_{REF} \times R_{FB1}}{V_{OUT} - V_{REF}}$$

$$R_{FB2} = \frac{5\,V \times 9.96\,M\Omega}{397\,V - 5\,V} = 127\,k\Omega \tag{17}$$

An output overvoltage is detected when the output voltage exceeds its nominal set-point level by 5%, as measured when the voltage at VSENSE is 105% of the reference voltage, V_{REF}.

$$V_{OUT(ovd)} = V_{OVD} \times \left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}} \right)$$

$$V_{OUT(ovd)} = (1.05 \times 5) \times \frac{9.96\,M\Omega + 127\,k\Omega}{127\,k\Omega} = 417\,V \tag{18}$$

An output undervoltage is detected when the output voltage falls below 5% below its nominal set-point as measured when the voltage at VSENSE is 95% of the reference voltage, V_{REF}:

$$V_{OUT(uvp)} = V_{UVD} \times \left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}} \right)$$

$$V_{OUT(uvp)} = (0.95 \times 5) \times \frac{9.96\,M\Omega + 127\,k\Omega}{127\,\Omega} = 377.3\,V \tag{19}$$

Add a small capacitor on VSENSE to filter out noise. Limit the value of the filter capacitor such that the RC time constant is limited to approximately 10 μs so as not to significantly reduce the control response time to output voltage deviations.

$$C_{VSENSE} = \frac{10\,\mu s}{R_{FB2}} = 82\,pF \tag{20}$$

5.1.1.9 Control Loop Compensation

The voltage error amplifier is compensated with a zero, f_{ZERO}, at the f_{PWM_PS} pole and a pole, f_{POLE}, placed at 20 Hz to reject high frequency noise and roll off the gain amplitude. The overall voltage loop crossover, f_V, is desired to be at 10 Hz. The compensation components of the voltage error amplifier are selected accordingly.

5.2 LLC Converter Stage Design

Increased demands for high power density power supplies have resulted in the increase in switching frequency of the converters designed. While component sizes tend to decrease with an increase in the switching frequency, device switching losses (which are proportional to frequency) have significantly increased contributing significant efficiency loss. Resonant converters use soft-switching techniques to alleviate switching loss problems and attain high efficiencies. Furthermore, soft-switching helps attain low losses during light load conditions, very low device stress, and reduced EMI.

The three main classes of resonant converters are series resonant converter (SRC), parallel resonant converter (PRC) and a combination of the two, the series-parallel resonant converter (SPRC). Among these the simplest and most popular resonant converter is the LLC series resonant converter.

The LLC resonant converter is based on the SRC. By using the transformer magnetizing inductor, zero-voltage switching can be achieved over a wide range of input voltage and load. As a result of multiple resonances, zero-voltage switching can be maintained even when the switching frequency is higher or lower than the resonant frequency. The converter achieves the best efficiency when operated close to its resonant frequency at a nominal input voltage. As the switching frequency is lowered, the voltage gain is significantly increased. This allows the converter to maintain regulation when the input voltage falls low. These features make the converter ideally suited to operate from the output of a high-voltage boost PFC pre-regulator, allowing it to hold up through brief periods of ac line-voltage dropout.

The UCC25600 is low-pin count and low cost LLC controller and requires minimal components to deliver optimum system performance. In addition, controller delivers complete system protection functions including overcurrent, UVLO, bias supply OVP and over temperature protection. The design process and component selection for this design are illustrated below. All design calculations are available in the Excel file "TIDA00355_LLC.xlsx" available at http://www.ti.com/tool/TIDA-00355.

5.2.1 Design Parameters

Table 3. Design Parameters for LLC Power Stage Design

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{INDC}	Input voltage	375	397	410	V DC
OUTPUT					
V_{OUT}	Output voltage		42		V DC
P_{LIMIT}	Output power limit			400	W
P_{OUT}	Max output power		390		W
f_{swnom}	Nominal switching frequency		98.5		kHz
	Line regulation		1		%
	Load regulation		1		%
PF	Targeted power factor		0.99		
η	Targeted efficiency		0.95		

5.2.2 Design Steps

5.2.2.1 *Flow Chart for LLC Resonant-Network Design*
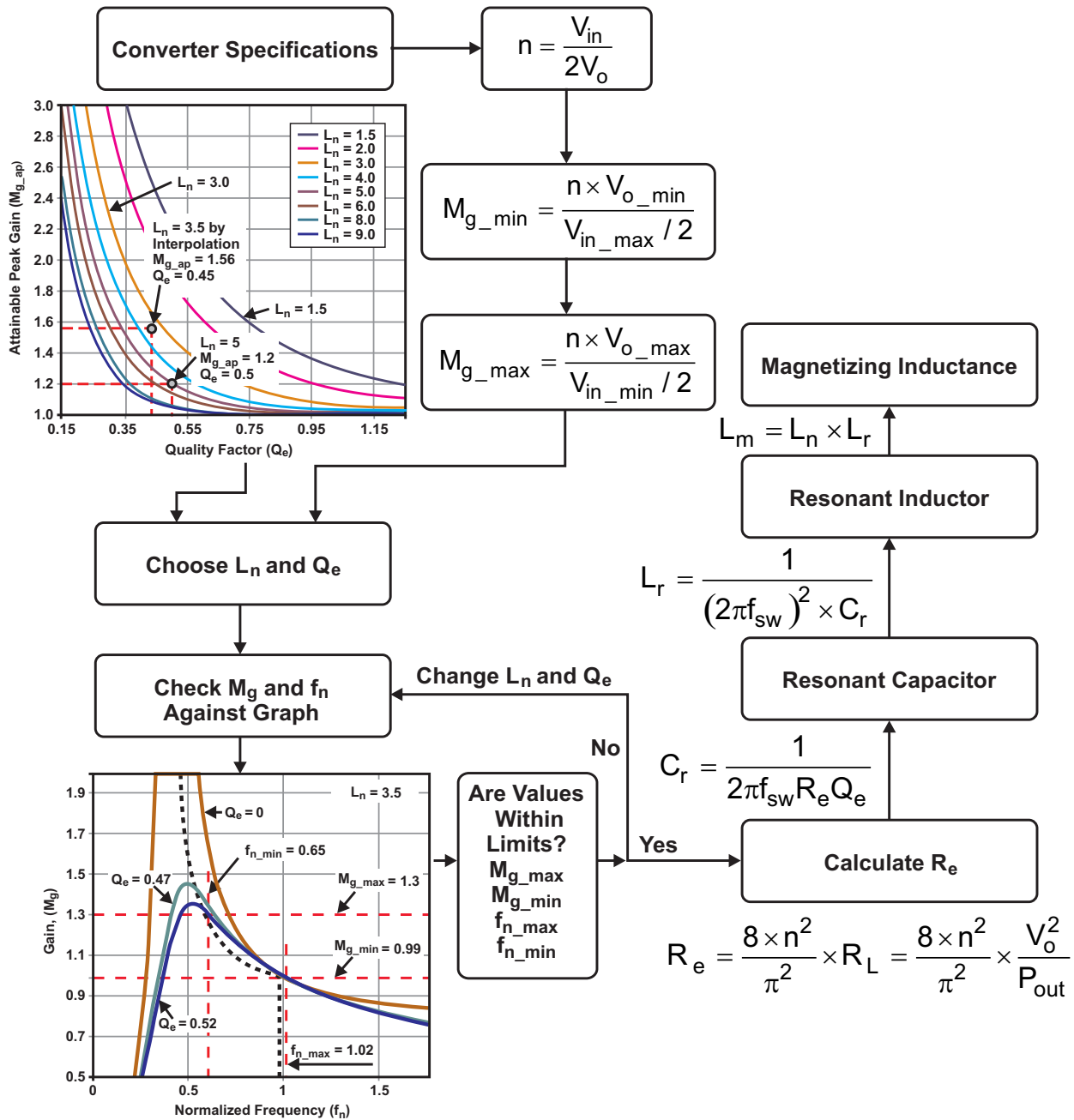
Figure 2. Flow Chart for LLC Resonant-Network Design

5.2.2.2   Determine Transformer Turns Ratio (n)

The transformer turns ratio is determined by Equation 21:

$$n = M_g \times \frac{V_{DCIN\_NOM} / 2}{V_O} : M_g = 1 \qquad (21)$$

Where Mg is the voltage gain.

From the specifications, the nominal values for input voltage and output voltage are 397 V and 42 V, respectively, so the turns-ratio can be calculated as

$$n = \frac{\left(V_{DCIN\_NOM} / 2\right)}{V_O} = \frac{(397 / 2)}{42} = 4.72 \Rightarrow 5 \qquad (22)$$

5.2.2.3   Determine M_{g_min} and M_{g_max}

M_{g_min} and M_{g_max} can be determined by using Equation 23 and Equation 24, respectively:

$$M_{g\_min} = n \times \left(\frac{V_{O\_min} + V_F}{V_{DCIN\_max} / 2} \right)$$

$$M_{g\_min} = 5 \times \left(\frac{42\ V \times (1-1\%) + 0.7\ V}{410\ V / 2} \right) = 1.03 \qquad (23)$$

In these calculations, 1% is used to adjust output voltage from the line and load regulation. V_F = 0.7 V is assumed for the secondary side diode's forward-voltage drop.

$$M_{g\_max} = n \times \left(\frac{V_{O\_max} + V_F}{V_{DCIN\_min} / 2} \right)$$

$$M_{g\_max} = 5 \times \left(\frac{42\ V \times (1+1\%) + 0.7\ V}{375\ V / 2} \right) = 1.15 \qquad (24)$$

To keep operation within the inductive region with an overload current capability of 110%, M_{g_max} is increased to 1.15 × 110% = 1.26.

5.2.2.4 Select L_n and Q_e

From Figure 3, if the values $L_n = 5$ and $Q_e = 0.45$ are selected, the corresponding $M_{g\_ap} = 1.3$, which is greater than $M_{g\_max} = 1.26$. Any other L_n curve which is not shown in Figure 3, for example $L_n = 3.5$, can be obtained by interpolating the curves of $L_n = 3$ and $L_n = 4$.
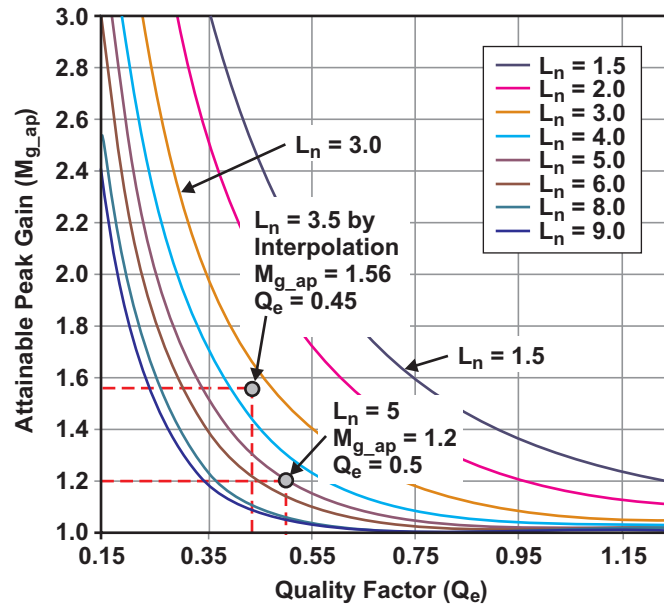
Figure 3. Peak Gain Curves

5.2.2.5 Determine Equivalent Load Resistance (R_e) of Resonant Network

R_e is determined from Equation 25. At full load,

$$R_e = \frac{8 \times n^2}{\pi^2} \times \left(\frac{V_O}{I_O} \right)$$

$$R_e = \frac{8 \times 5^2}{\pi^2} \times \left(\frac{42}{9} \right) = 94.6 \ \Omega$$

(25)

5.2.2.6 Determine Resonant Circuit Parameters

A switching frequency of 98 kHz is selected initially for the series resonant frequency. The resonant circuit's parameters at full load are determined from Equation 26, Equation 27, and Equation 28.

$$C_r = \frac{1}{2 \times \pi \times Q_e \times f_o \times R_e}$$

$$C_r = \frac{1}{2 \times \pi \times 0.45 \times 98 \ k \times 94.6} = 38.2 \ nF$$

(26)

$$L_r = \frac{1}{(2 \times \pi \times f_o)^2 \times C_r}$$

$$L_r = \frac{1}{(2 \times \pi \times 98 \ k\Omega)^2 \times 38.2 \ nF} = 69 \ \mu H$$

(27)

$$L_m = L_n \times L_r$$

$$L_m = 5 \times 69 \ \mu H = 345 \ \mu H$$

(28)

5.2.2.7   Verify the Resonant — Circuit Design With Selected Values

The standard values selected for the resonant circuit are L_r = 75 μH, C_r = 39 nF , L_m = 400 μH.

The design parameters are

- Series resonant frequency:

$$f_o = \frac{1}{2 \times \pi \times \sqrt{L_r \times C_r}}$$

$$f_o = \frac{1}{2 \times \pi \times \sqrt{39 \text{ nF} \times 75 \text{ μF}}} = 93 \text{ kHz}$$

(29)

- Inductance ratio:

$$L_n = \frac{L_m}{L_r}$$

$$L_n = \frac{400 \text{ μH}}{75 \text{ μH}} = 5.33$$

(30)

- Quality factor at full load:

$$Q_e = \frac{\sqrt{L_r / C_r}}{R_e}$$

$$Q_e = \frac{\sqrt{75\mu / 39 \text{ n}}}{94.6} = 0.463$$

(31)

Plot the gain curves corresponding to the design parameters (Figure 4). The following are operating frequency specifications:

- The frequency at series resonance is f_0 = 93 kHz.
- The frequency at M_{g_min} is f_{sw_max} = 110 kHz.
- The frequency at M_{g_max} is f_{sw_min} with an overload (110%) = ~ 70 kHz.
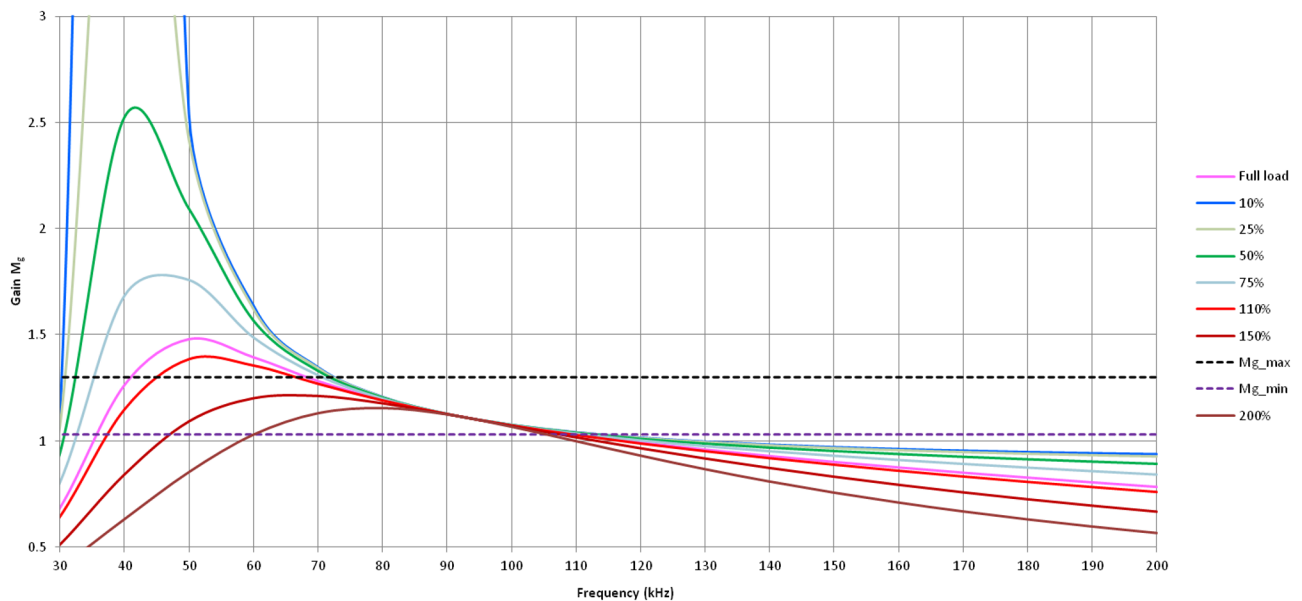
Figure 4. Verification of Resonant-Circuit Design

5.2.2.8   Determine the Primary-Side Currents

The primary-side RMS load current (I_{pri}) with a 110% overload is determined from Equation 32:

$$I_{pri} = \frac{\pi}{2\sqrt{2}} \times \left(\frac{I_O \times 110\%}{n} \right)$$

$$I_{pri} = 1.11 \times \left(\frac{9 \times 1.1}{5} \right) = 2.2 \text{ A}$$

(32)

The RMS magnetizing current (I_m) at f_{sw_min} = 70 kHz is determined from Equation 33:

$$I_m = 0.901 \times \left(\frac{n \times V_o}{\omega \times L_m} \right)$$

$$I_m = 0.901 \times \left(\frac{5 \times 42}{2 \times \pi \times 70 \text{ kHz} \times 400 \text{ }\mu\text{H}} \right) = 1.08 \text{ A}$$

(33)

The resonant circuit's current (I_r) is determined from Equation 34:

$$I_r = \sqrt{I_m^2 + I_{pri}^2}$$

$$I_r = \sqrt{2.2^2 + 1.08^2} = 2.45 \text{ A}$$

(34)

This is also the transformer's primary winding current at f_{sw_min}.

5.2.2.9   Determine the Secondary-Side Currents

The total secondary-side RMS load current is the current referred from the primary-side current (I_{pri}) to the secondary side:

With a 110% overload,

$$I_{sec} = n \times I_{pri}$$

$$I_{sec} = 5 \times 2.2 \text{ A} = 11 \text{ A}$$

(35)

Because the transformer's secondary side has a center-tapped configuration, this current is equally split into two transformer windings on the secondary side. The current of each winding is then calculated as

$$I_{sec\_sw} = \frac{\sqrt{2}}{2} \times I_{sec}$$

$$I_{sec\_sw} = \frac{\sqrt{2}}{2} \times 11 \text{ A} = 7.8 \text{ A}$$

(36)

The corresponding half-wave average current is

$$I_{sec\_avg} = \frac{\sqrt{2}}{\pi} \times I_{sec}$$

$$I_{sec\_avg} = \frac{\sqrt{2}}{\pi} \times 11 \text{ A} = 4.95 \text{ A}$$

(37)

5.2.2.10 Select the Transformer

The transformer can be built or purchased from a catalog. The specifications for this example are:

- Turns ratio (n): 5
- Primary terminal voltage: 450-V AC
- Primary winding's rated current, I_{wp}: 2.5 A
- Secondary terminal voltage: 100-V AC
- Secondary winding's rated current, I_{ws}: 7.8 A (center-tapped configuration)
- Frequency at no load: 110 kHz
- Frequency at full load: 70 kHz
- Insulation between primary and secondary sides: IEC60950 reinforced insulation

5.2.2.11 Select the Resonant Inductor

The inductor can be built or purchased from a catalog, with these specifications:

- Series resonant inductance, L_r: 75 μH
- Rated current, I_{Lr}: 2.5 A
- Terminal AC voltage:

$$V_{Lr} = \omega \times L_r \times I_r$$
$$V_{Lr} = 2 \times \pi \times 110 \text{ kHz} \times 75 \text{ }\mu\text{H} \times 2.45 \text{ A} = 127 \text{ V} \qquad (38)$$

- Frequency range: 70 to 110 kHz

5.2.2.12 Select the Resonant Capacitor

The resonant capacitor (Cr) must have a low dissipation factor (DF) due to its high-frequency, high-magnitude current. Capacitors often used for LLC converters are made with metalized polypropylene film. These capacitors present very low DF and are capable of handling high-frequency current.

Before a capacitor is selected, its voltage rating has to be de-rated with regard to the switching frequency in use.

The selected capacitor (Cr) must meet these additional specifications:

- Rated current, I_{Cr}: 2.5 A
- AC voltage across capacitor

$$V_{Cr} = \frac{I_r}{\omega \times C_r}$$
$$V_{Cr} = \frac{2.45 \text{ A}}{2\pi \times 70 \text{ kHz} \times 39 \text{ nF}} = 143 \text{ V} \qquad (39)$$

- RMS voltage:

$$V_{Cr\_RMS} = \sqrt{(V_{DCIN\_max} / 2)^2 + V_{Cr}^2}$$
$$V_{Cr\_RMS} = \sqrt{(410 / 2)^2 + 145^2} = 251 \text{ V} \qquad (40)$$

5.2.2.13 Select the Primary Side MOSFETs

Each MOSFET sees the input voltage as its maximum applied voltage:

$$V_{DS} = 1.2 \times V_{INDC\_max}$$
$$V_{DS} = 1.2 \times 410 = 492 \text{ V} \Rightarrow 500 \text{ V} \tag{41}$$

Each MOSFET conducts half of the resonant network's current in steady state after the resonant capacitor's voltage has been established. However, during the initial start-up and transient, the current in each MOSFET can be as high as the resonant current (I_r) with a 110% overload:

$$I_{DS\_RMS} = I_r = 2.45 \text{ A} \tag{42}$$

MOSFET switching losses are minimized by ZVS; therefore, the conduction losses from the MOSFETs may become the main concern for the design. This suggests that MOSFETs with a low R_{DS_on} should be used.

The MOSFET selected for this design is FDPF18N50, a 500-V/18-A device. Consider using a higher voltage rating FET (600 V/650 V) based on the design de-rating needs of the end equipment.

5.2.2.14 Select Dead Time to Ensure ZVS Operation

The condition under which the converter has sufficient switching dead time for ZVS is described by Equation 43:

$$t_{dead} \geq 16 \times C_{eq} \times f_{sw} \times L_m \tag{43}$$

C_{eq} is mainly from the MOSFET C_{ds}. The MOSFET C_{ds} for FDPF18N50 is approximately 315 pF.

$$t_{dead} \geq 16 \times 315 \text{ pF} \times 120 \text{ kHz} \times 400 \text{ μH}$$
$$t_{dead} \geq 242 \text{ ns} \tag{44}$$

5.2.2.15 Select Diode Rectifier

The rectifier voltage rating of the diode is determined as

$$V_{diode} = \frac{V_{DCIN\_max} / 2}{2} \times 2 \tag{45}$$

The current rating of the diodes is determined as

$$I_{sec\_avg} = \frac{\sqrt{2}}{\pi} \times I_{sec}$$
$$I_{sec\_avg} = \frac{\sqrt{2}}{\pi} \times 11 \text{ A} = 4.95 \text{ A} \tag{46}$$

The rectifier diode selected for this design is the STPS20M120.

5.2.2.16 Output Filter Design

In an LLC converter, the output filter may consist of capacitors alone instead of the LC filter seen in most pulse-width-modulated converters, although a small second-stage LC filter can be an option. If the filter has only capacitors, they should be chosen to allow conduction of the rectifier current through all AC components.

For the load current (I_o), the capacitor's RMS current rating at about 100 kHz is calculated as

$$I_{Co\_RMS} = \sqrt{\left(\frac{\pi}{\sqrt{2}} \times I_O\right)^2 - I_O^2}$$

$$I_{Co\_RMS} = 0.482 \times I_O = 0.482 \times 9.0 = 4.34 \text{ A}$$

(47)

Usually, a single capacitor will not allow such a high RMS current, so several capacitors connected in parallel are often used and may offer a lower profile.

The ripple voltage is a function of the amount of AC current that flows in and out of the capacitors with each switching cycle, multiplied by the capacitors' ESR. Because all electric current, including the load's DC current, can be assumed to flow in and out of the filter capacitors, this is a very good estimate of the ripple voltage. To meet the specification for a 120-mV ripple voltage, the maximum ESR should be

$$ESR_{max} = \frac{V_{O\_pk\_pk}}{I_{rect\_pk}} = \frac{V_{O\_pk\_pk}}{\left(\frac{\pi}{4} \times I_O\right) \times 2}$$

$$ESR_{max} = \frac{0.12 \text{ V}}{\left(\frac{\pi}{2} \times 9\right)} = 8.5 \text{ m}\Omega$$

(48)

Capacitance value is selected based on

*   Voltage rating: 63 V
*   Ripple-current rating: 4.5 A at 100 kHz
*   ESR: < 8.5 mΩ

The design uses four numbers of C3225X7S2A475M200AB (4.7 µF, 100 V) capacitors to meet the RMS rating.

5.2.3 Components for UCC25600 Controller

Each of the components for the controller is selected as per the datasheet recommendations. The values can also be obtained from "TIDA00355_LLC.xls" available at http://www.ti.com/tool/TIDA-00355.

5.2.3.1 Dead Time

A dead time of 350 ns is selected as per Equation 49. The resistor needed at the DT pin to GND is calculated with

$$t_d = 20 \text{ ns} + R_{dt} \times 24 \text{ ns} / \text{k}\Omega$$

$$R_{td} = \frac{350 - 20}{24} = 13.75 \text{ k}\Omega \tag{49}$$

A standard value of 13.7 kΩ is used.

5.2.3.2 Frequency Setting Resistor

The frequency limiting resistor can be calculated based on following equations:

$$I_{fmax} = \frac{6 \text{ ns}}{\left(\dfrac{1}{2 \times f_{max}}\right) - 150 \text{ ns}} \tag{50}$$

A maximum frequency of 400 kHz is selected to enable burst mode of operation for light load conditions. Burst mode gets enabled when the control loop demands a switching frequency higher than 350 kHz.

$$I_{fmax} = \frac{6 \text{ ns}}{\left(\dfrac{1}{2 \times 400 \text{ kHZ}}\right) - 150 \text{ ns}} = 5.46 \text{ mA} \tag{51}$$

$$I_{fmin} = \frac{6 \text{ ns}}{\left(\dfrac{1}{2 \times f_{min}}\right) - 150 \text{ ns}} \tag{52}$$

With a minimum frequency of 65 kHz selected considering overload conditions,

$$I_{fmin} = \frac{6 \text{ ns}}{\left(\dfrac{1}{2 \times 70 \text{ kHz}}\right) - 150 \text{ ns}} = 0.86 \text{ mA} \tag{53}$$

Minimum frequency limiting resistor is calculated as

$$R_{fmin} = \frac{2.5 \text{ V}}{I_{fmin}}$$

$$R_{fmin} = \frac{2.5 \text{ V}}{0.86 \text{ mA}} = 2.9 \text{ k}\Omega \tag{54}$$

Selected value is 2.34 kΩ, to avoid lower frequency operation.

$$R_{fmax} = \frac{2.5 \text{ V}}{I_{fmax} - I_{fmin}}$$

$$R_{fmax} = \frac{2.5 \text{ V}}{5.46 \text{ mA} - 0.86 \text{ mA}} = 0.54 \text{ mA} \tag{55}$$

5.2.3.3   *Overcurrent Protection*

The current can be indirectly sensed through the voltage across resonant capacitor by using the sensing network shown in Figure 5.
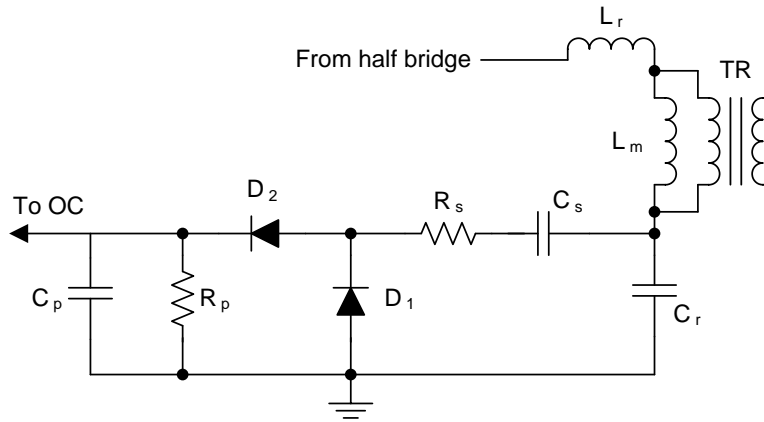
Figure 5. Current Sensing for LLC Resonant Converter

Current sensing network components are calculated as

Transfer AC voltage across resonant S capacitor into current source R_s is given by

$$R_s = \frac{V_{Crpk}^2}{2 \times P_{rs}}$$

$$V_{Crpk} = \frac{4 \times V_{Cr}}{\pi} = \frac{4 \times 143}{\pi} = 182 \text{ V}$$

$$R_s = \frac{182^2}{2 \times 0.05 \text{ W}} = 331 \text{ k}\Omega \tag{56}$$

A standard value of 316 kΩ is selected.

The blocking DC voltage on resonant capacitor is given by

$$C_s = \frac{10}{R_s \times f_{min}}$$

$$C_s = \frac{10}{316 \text{ k} \times 70 \text{ kHz}} = 0.45 \text{ nF} \tag{57}$$

A standard value of 470 pF is selected.

The load resistor of the current source is given by

$$R_p = \frac{R_s}{V_{Crpk}} \times \pi$$

$$R_p = \frac{316 \text{ k}}{182} \times \pi = 5.45 \text{ k}\Omega \tag{58}$$

A standard value of 5.49 kΩ is selected.

For the filter capacitor for noise suppression,

$$C_p = \frac{10}{R_p \times f_{min}}$$

$$C_p = \frac{10}{5.49 \text{ k} \times 70 \text{ k}} = 26 \text{ nF} \tag{59}$$

A standard value of 33 nF is selected.

5.2.4 CC-CV Feedback

The charging cycle of a Li-ion battery (or a similar battery) consists of a constant-current phase and a constant-voltage phase. To reflect this behavior, this reference design contains two feedback paths, implemented with the highly integrated op-amp, TL103W. The TL103W integrates two precision op-amps and a 2.5-V voltage reference — both of which ease out CC-CV control loop circuitry implementation.

The first feedback path regulates the voltage in the constant-voltage phase through the resistor divider network formed by R27 and R46. The voltage obtained is compared with the internal reference of 2.5 V to regulate the loop.

The second feedback path regulates the current in the constant-current phase once the output current reaches the output-current limit. The output-current limit is set by the value of the two parallel shunt resistors, R18 and R20. These resistors determine the current regulation set point and must be adequately rated in terms of power dissipation. The voltage across those resistors is compared with the reference set by R29 and R30.

The designer can change the output voltage by changing the value of R27 and R46. The designer can change the output current limit by changing R18 and R20. If the temperature dissipated by the shunt resistors is too high, the designer may either increase the number of shunt resistors in parallel or tune the voltage reference set by R29 and R30.

5.3 Bias Power Supply

The PFC, LLC controllers, and gate driver need auxiliary power supply for start-up and operation. An auxiliary power supply of 1.3 W is produced on board by using a quasi-resonant/discontinuous current mode flyback controller with primary-side control, the UCC28722. This controller offers a low part count and relatively low-cost solution eliminating the need for opto-coupler and TL431 feedback circuitry. In addition, quasi-resonant topology ensures high efficiency, optimizing the losses.

The converter is powered from the output of the PFC pre-regulator stage and must be able to start up prior to the PFC stage being operational. For this reason, the circuit is designed to operate over a wide input voltage, 100-V to 450-V DC. The flyback transformer has two output windings, which are isolated to each other and supply different circuits on the board. The design specifications of these outputs are shown in Table 4:

Table 4. Design Specifications of Bias Supply

PARAMETER	SPECIFICATION
Input voltage range	160-V AC to 265-V AC
Output voltages	13 V at 50 mA All circuits on the primary side: PFC controller, LLC controller, gate driver UCC27714
	6.5 V at 100 mA Internal circuit needs and external microcontroller power

Design of power stage components (flyback transformer, output filter capacitor, and feedback circuitry) is explained in detail in the UCC28722/UCC28720 application report (SLUA700).

All design calculations are available in the Excel file "TIDA00355_Bias_Supply.xlsx" available at http://www.ti.com/tool/TIDA-00355.

6   Getting Started Hardware

6.1   Test Conditions

Input conditions:
- V_{IN}: 175-V to 265-V AC
- Set the input current limit to 3.5 A

Output:
- Variable simulated battery load, 20 to 42 V, 0 to 9 A

6.2   Equipment Needed

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multi-meters
- Electronic load to simulate battery

6.3   Procedure

1. Connect input terminals (connector J1) of the reference board to the AC power source.
2. Connect output terminals (connector J3) to electronic load, maintaining correct polarity.
3. Set the minimum load of about 100 mA, and minimum voltage of 25 V.
4. Gradually increase the input voltage from 0 V to turn on voltage of 175-V AC.
5. Turn on the load to apply voltage to the output terminals of the charger.
6. Observe the startup conditions for smooth switching waveforms.

7 Test Data

7.1 Efficiency and Regulation

7.1.1 Standby Power With Battery Disconnected

The standby power was noted at various input voltages with no load conditions (that is, when the battery is disconnected). The results are tabulated in Table 5 and are in accordance with the target specifications.

Table 5. Standby Test Results

AC INPUT	INPUT POWER (BATTERY DISCONNECTED)
175-V AC	140 mW
230-V AC	150 mW
265-V AC	170 mW

7.1.2 Performance Data of Charger

Table 6. At 175-V AC

V_{IN} (VAC)	P_{IN} (W)	PF	I_{THD}	V_O (V)	I_O (A)	P_O (W)	EFFICIENCY (%)
175	0.14	–	–	0.00	0.000	0.00	0.00
175	2.80	–	–	42.37	0.000	0.00	0.00
175	8.59	0.804	44.7	42.35	0.100	4.24	49.31
175	27.28	0.939	23.1	42.35	0.500	21.18	77.63
175	50.74	0.977	15.8	42.35	1.000	42.35	83.46
175	141.90	0.997	1.3	42.33	3.000	127.00	89.50
175	233.70	0.998	2.0	42.32	5.000	211.58	90.53
175	327.20	0.999	3.2	42.30	7.000	296.10	90.50
175	422.30	0.990	13.9	42.28	9.000	380.55	90.11
175	429.80	0.989	14.9	42.28	9.150	386.90	90.02
175	410.90	0.997	7.2	40.00	9.210	368.40	89.66
175	363.00	0.998	5.9	35.00	9.220	322.70	88.90
175	314.80	0.998	4.5	30.00	9.210	276.30	87.77
175	266.50	0.998	3.5	25.00	9.200	230.00	86.30
175	218.30	0.998	2.5	20.00	9.200	184.00	84.29

Table 7. At 230-V AC

V_{IN} (VAC)	P_{IN} (W)	PF	I_{THD}	V_O (V)	I_O (A)	P_O (W)	EFFICIENCY (%)
230	0.17	–	–	0.00	0.000	0.00	0.00
230	1.90	–	–	42.39	0.000	0.00	0.00
230	8.77	0.723	54.1	42.37	0.100	4.24	48.31
230	26.82	0.907	24.3	42.37	0.500	21.18	78.98
230	49.77	0.942	21.1	42.36	1.000	42.36	85.11
230	140.30	0.992	2.8	42.34	3.000	127.03	90.54
230	231.20	0.996	1.9	42.32	5.000	211.62	91.53
230	323.60	0.997	2.7	42.30	7.000	296.13	91.51
230	416.00	0.994	9.4	42.28	9.000	380.56	91.48
230	423.30	0.993	9.9	42.28	9.180	388.10	91.69
230	405.10	0.997	4.0	40.00	9.250	370.00	91.34

Table 7. At 230-V AC (continued)

V$_{IN}$ (VAC)	P$_{IN}$ (W)	PF	I$_{THD}$	V$_O$ (V)	I$_O$ (A)	P$_O$ (W)	EFFICIENCY (%)
230	358.30	0.997	3.3	35.00	9.245	323.58	90.31
230	310.70	0.997	2.7	30.00	9.235	277.05	89.17
230	263.20	0.996	2.4	25.00	9.230	230.75	87.67
230	215.80	0.996	2.0	20.00	9.220	184.40	85.45

Table 8. At 265-V AC

V$_{IN}$ (VAC)	P$_{IN}$ (W)	PF	I$_{THD}$	V$_O$ (V)	I$_O$ (A)	P$_O$ (W)	EFFICIENCY (%)
265	0.18	–	–	0.00	0.000	0.00	0.00
265	2.00	–	–	42.39	0.000	0.00	0.00
265	8.33	0.625	97.0	42.37	0.100	4.24	50.86
265	26.29	0.880	34.0	42.36	0.500	21.18	80.57
265	49.22	0.911	23.0	42.36	1.000	42.36	86.06
265	138.64	0.987	8.1	42.34	3.000	127.02	91.62
265	229.60	0.994	2.4	42.32	5.000	211.61	92.16
265	321.40	0.996	2.6	42.30	7.000	296.11	92.13
265	413.90	0.996	3.6	42.28	9.000	380.51	91.93
265	422.30	0.995	6.3	42.26	9.180	387.93	91.86
265	404.20	0.997	3.2	40.00	9.250	370.00	91.54
265	357.30	0.996	2.9	35.00	9.245	323.58	90.56
265	309.90	0.996	2.6	30.00	9.235	277.05	89.40
265	262.30	0.995	2.4	25.00	9.230	230.75	87.97
265	215.10	0.993	2.5	20.00	9.220	184.40	85.73

7.1.3 Efficiency of Overall System
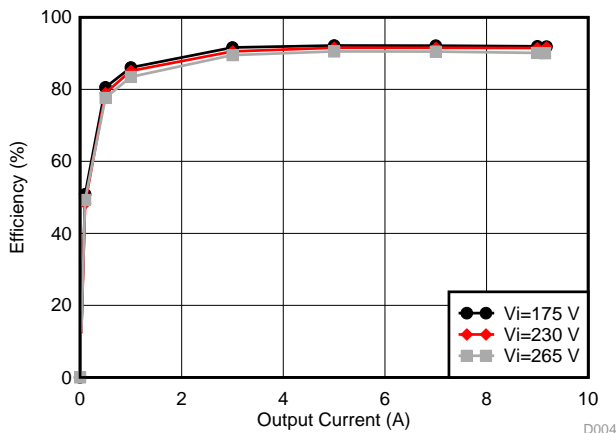
Figure 6. Efficiency in CV Operation
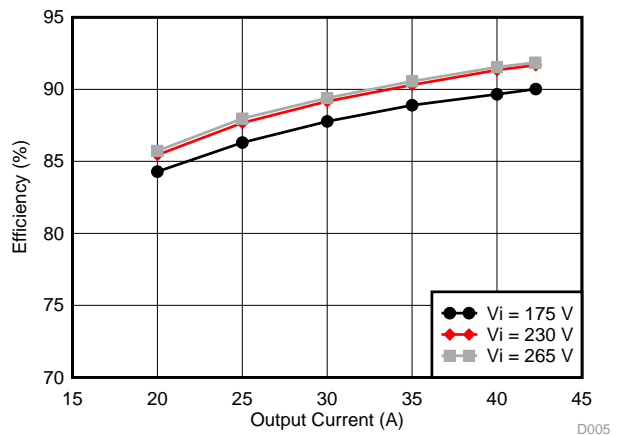
Figure 7. Efficiency in CC Operation

7.1.4 Load Regulation
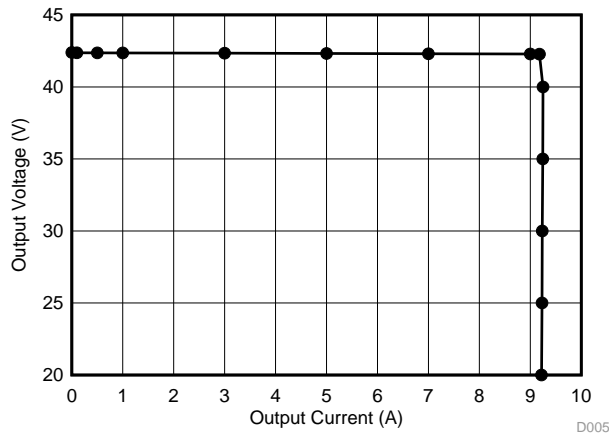
Figure 8. Load Regulation

7.1.5 Efficiency of PFC Power Stage
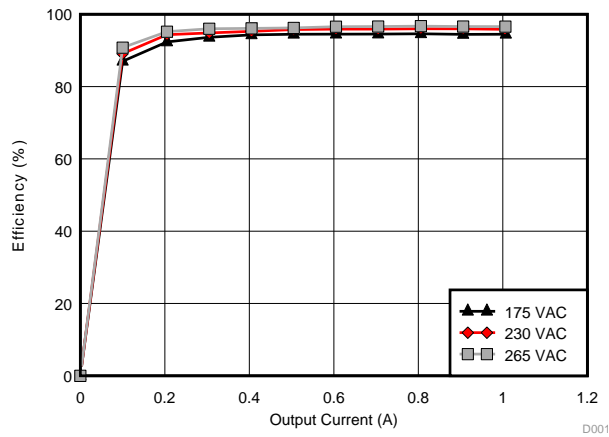
Figure 9. PFC Power Stage Efficiency

7.1.6 Efficiency of LLC Power Stage
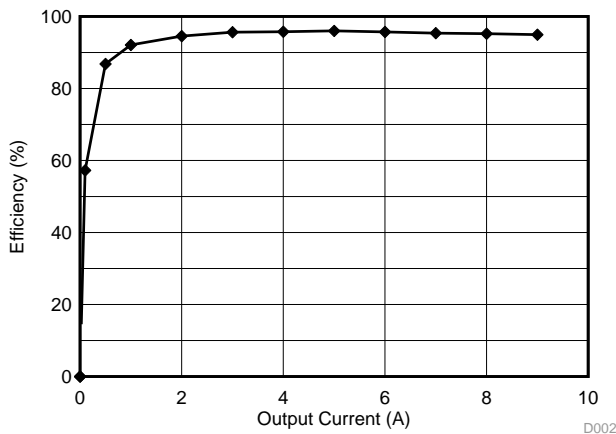
Figure 10. LLC Converter Efficiency in CV Operation
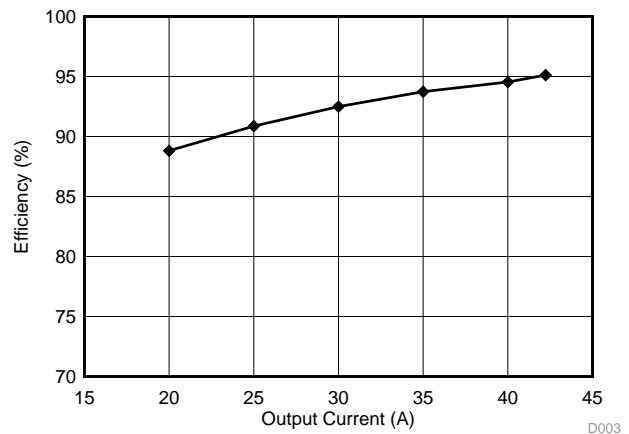
Figure 11. LLC Converter Efficiency in CC Operation

7.2 Waveforms

7.2.1 PFC Switching Waveforms
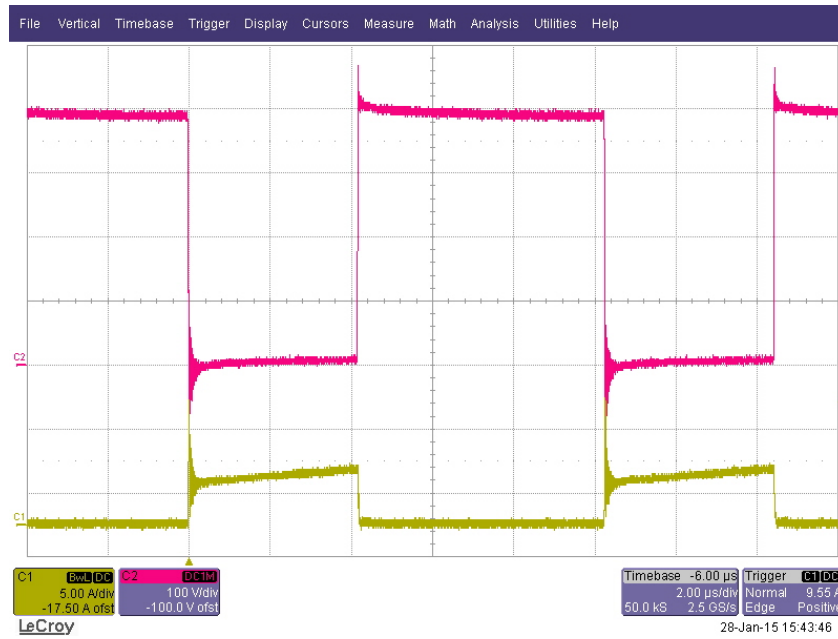
Figure 12. V$_{IN}$ = 175-V AC, Full Load

NOTE: Red trace: Drain voltage, 100 V/div; Yellow trace: Drain current, 5 A/div

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Figure 13. V$_{IN}$ = 265-V AC, Full Load

NOTE: Red trace: Drain voltage, 100 V/div; Yellow trace: Drain current, 5 A/div

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7.2.2   LLC Waveforms
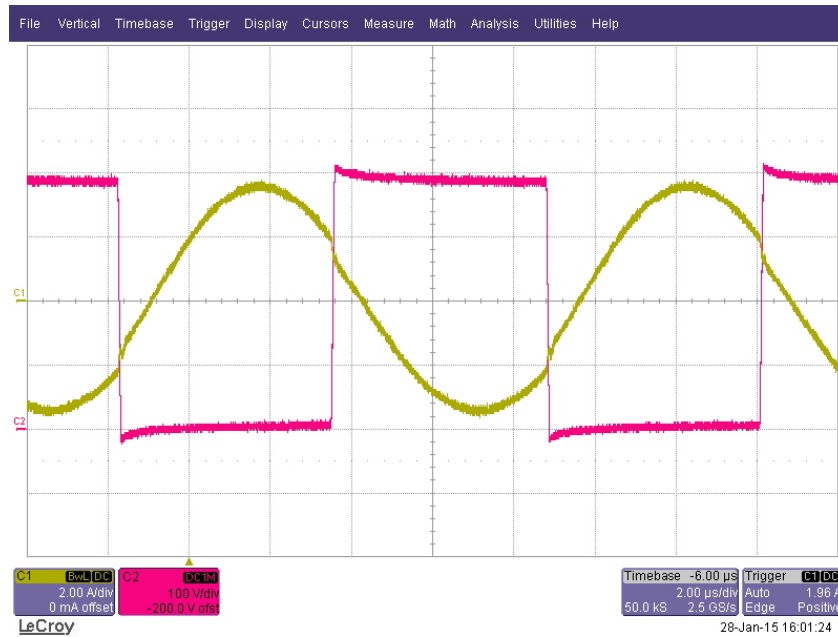
Figure 14. Full Load, CV/CC Transition Point

NOTE: Red trace: Switch node voltage, 100 V/div; Yellow trace: Resonant tank current, 2 A/div

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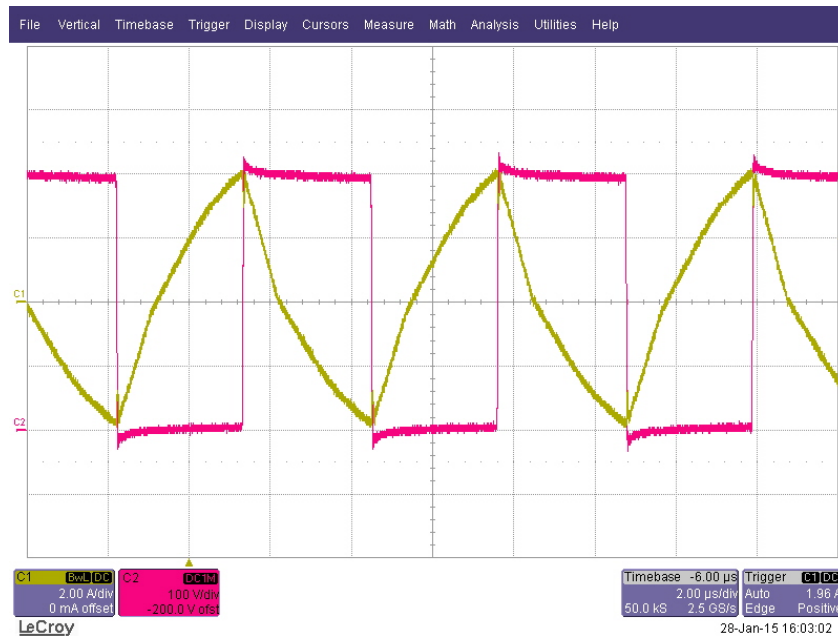
Figure 15. Deep CC Operation, V_O = 20 V

NOTE: Red trace: Switch node voltage, 100 V/div; Yellow trace: Resonant tank current, 2 A/div

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7.2.3 Output Diode Stress
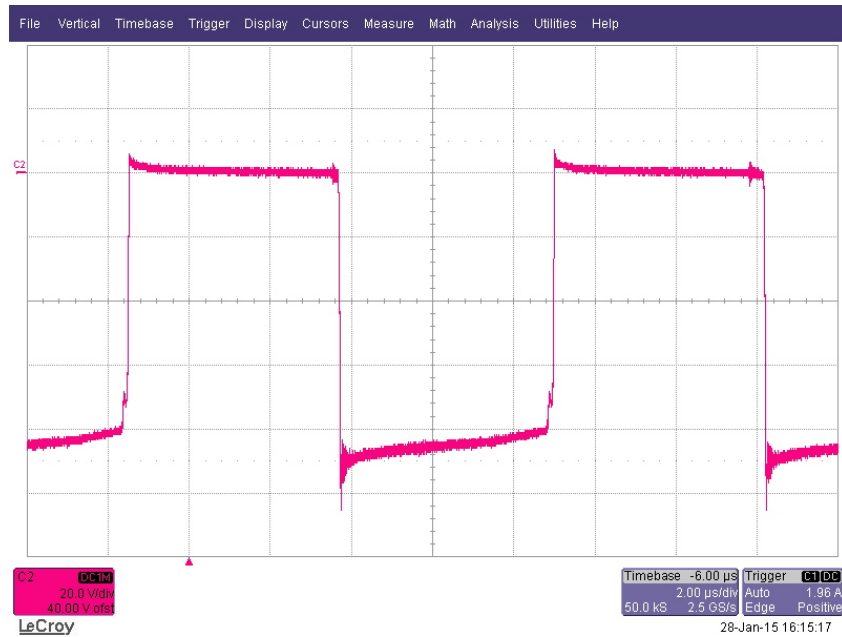
Figure 16. Full Load, CV/CC Transition Point

NOTE: Red trace: Output diode reverse voltage, 20 V/div
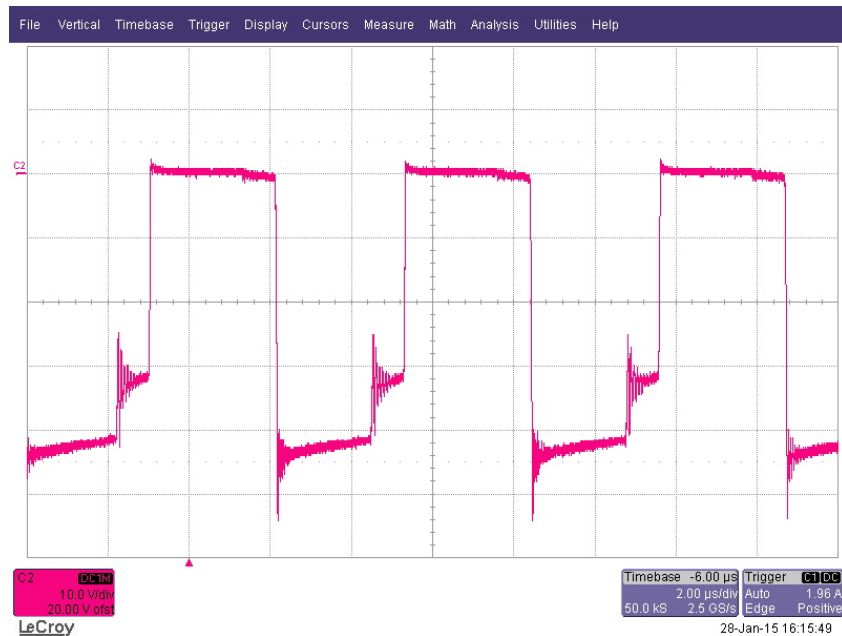
Figure 17. Deep CC Operation, V_O = 20 V

NOTE: Red trace: Output diode reverse voltage, 10 V/div

7.2.4   Bias Supply Switching Waveforms
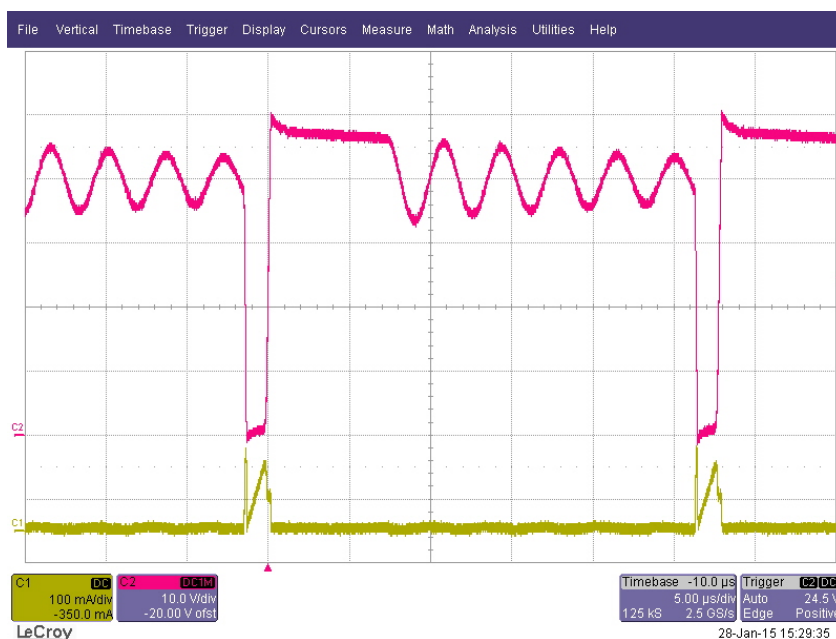
Figure 18. Auxiliary Output (5 V) Loaded to 100 mA

NOTE: Red trace: Collector voltage, 100 V/div; Yellow trace: Collector current, 100 mA/div

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7.2.5 Output Ripple and Noise
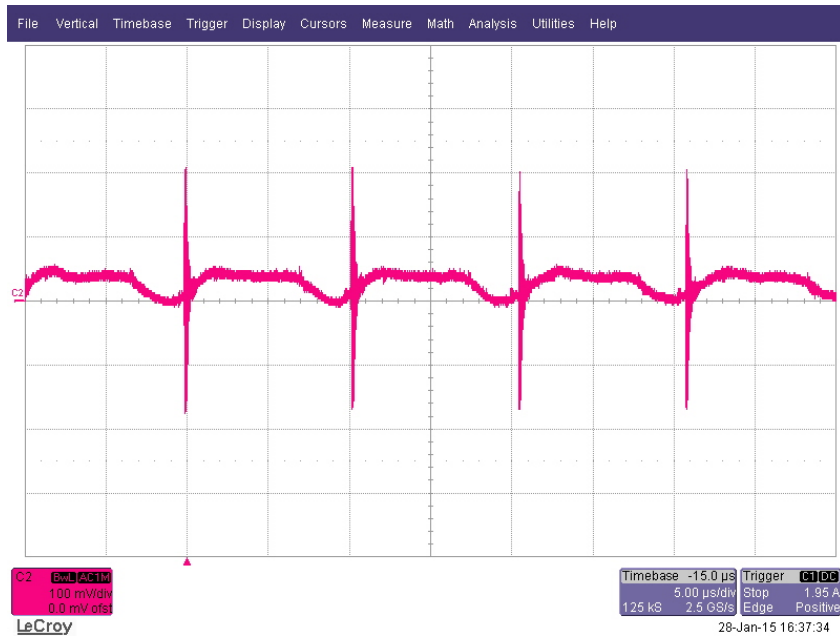
Figure 19. Full Load, CV/CC Transition Point

NOTE: Red trace: Output voltage ripple and noise, 100 mV/div
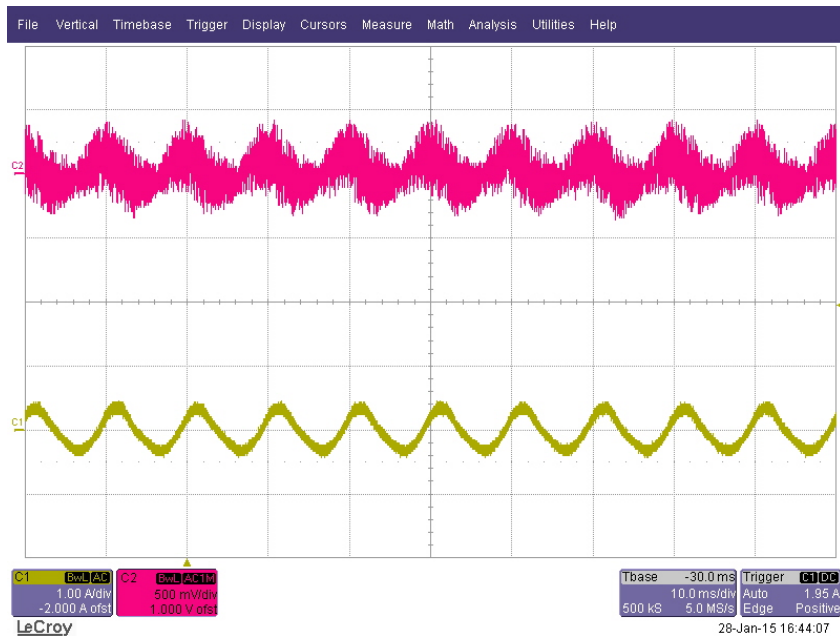
Figure 20. CC Operation, V$_O$ = 40 V

NOTE: Red trace: Output voltage ripple and noise, 500 mV/div;
Yellow trace: Output current ripple, 1 A/div

7.2.6 Start-Up
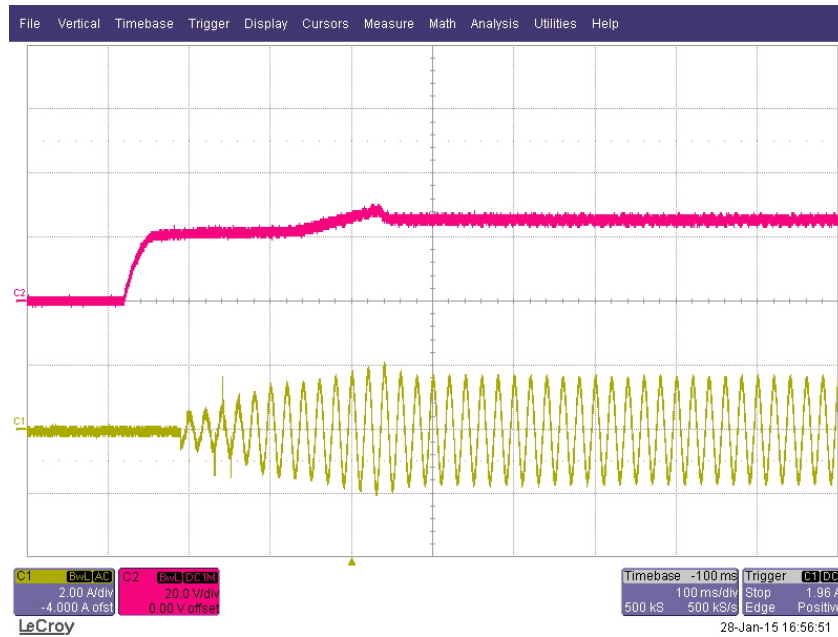
Figure 21. Deep CC Operation, V$_O$ = 20 V

NOTE: Red trace: Output voltage, 20 V/div; Yellow trace: Input current, 2 A/div

7.2.7 Inrush
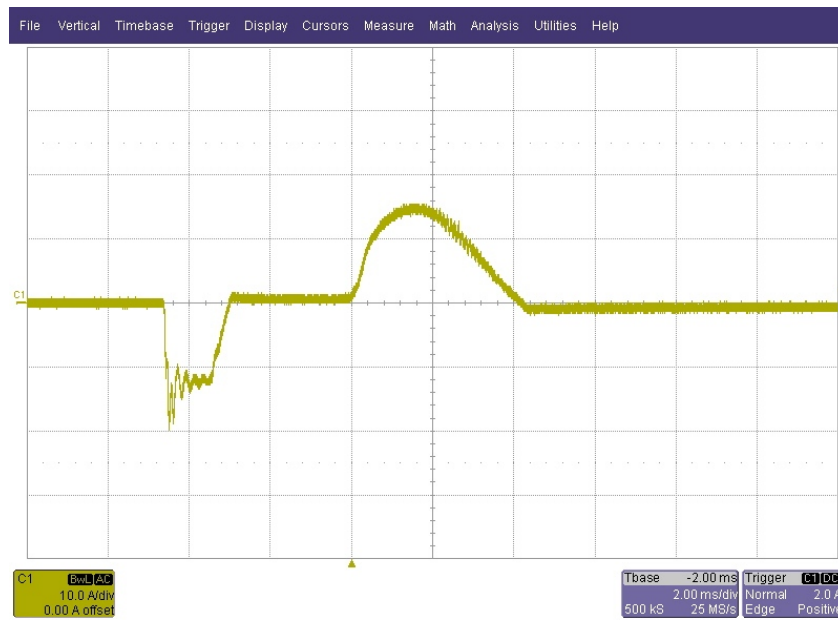
Figure 22. V$_{IN}$ = 265-V AC, Full Load

NOTE: Yellow trace: Input current, 10 A/div

7.3 Conducted Emissions

7.3.1 Emissions at Full Load

Generally conducted emissions will be more at full load. So, this operating point is chosen for measuring conducted EMI.

230-V AC input, 42-V, 9-A simulated battery load connected to PSU output with short leads.

The conducted peak emissions in a pre-compliance test set-up were compared against EN55022 Class-A quasi-peak limits and found to be meeting them comfortably so the quasi-peak emissions can also meet them easily.
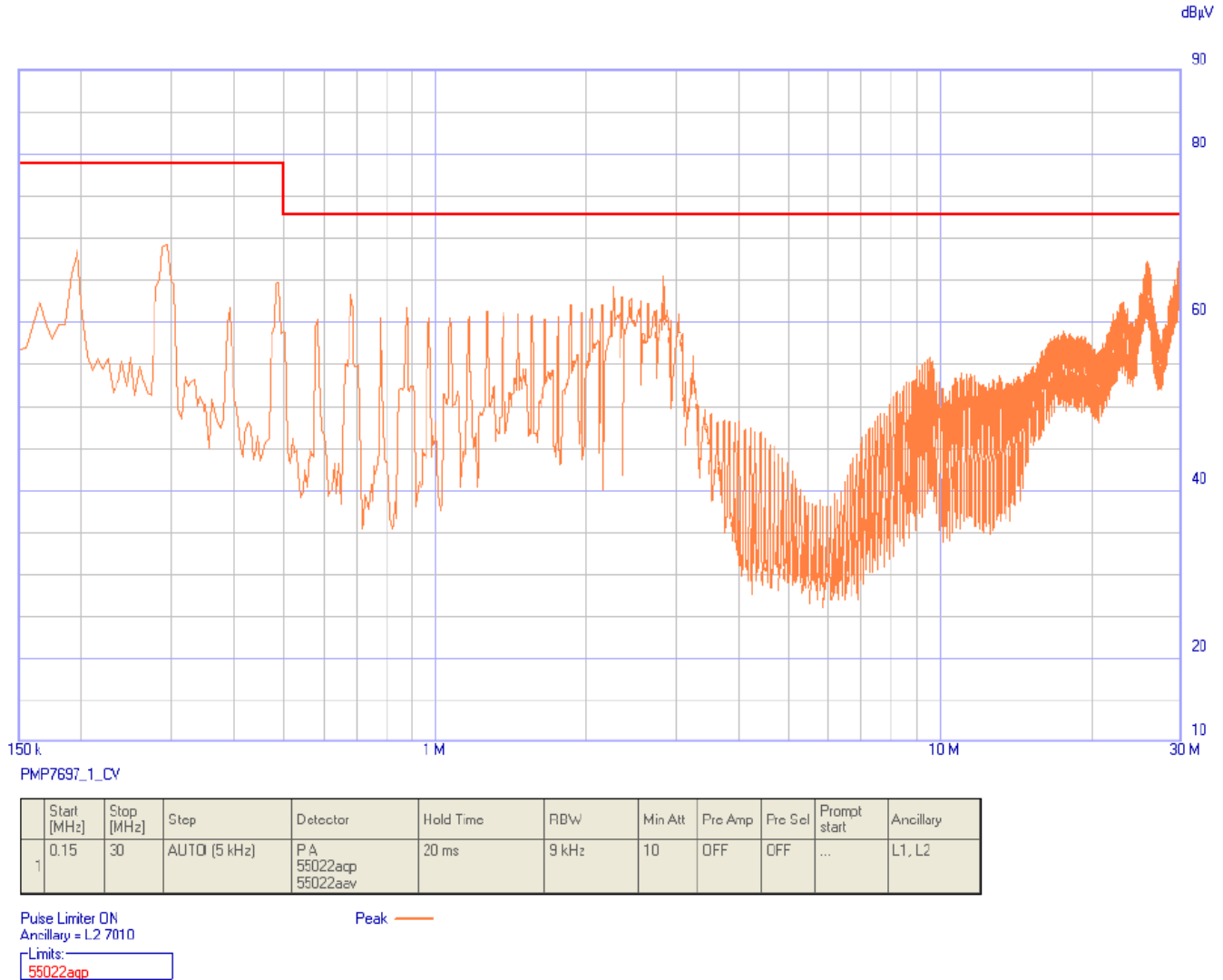
Figure 23. Conducted Peak Emissions at Full Load

230-V AC input, 42-V, 9-A simulated battery load connected to PSU output with short leads.

The conducted average emissions in a pre-compliance test setup were compared against EN55022 Class-A average limits and found to be meeting them.

PMP7697_1_CV

	Start [MHz]	Stop [MHz]	Step	Detector	Hold Time	RBW	Min Att	Pre Amp	Pre Sel	Prompt start	Ancillary
1	0.15	30	AUTO (5 kHz)	P A 55022acp 55022aav	20 ms	9 kHz	10	OFF	OFF	...	L1, L2

Pulse Limiter ON
Ancillary = L2 7010   Avg ———
┌Limits:──────
│ 55022aav
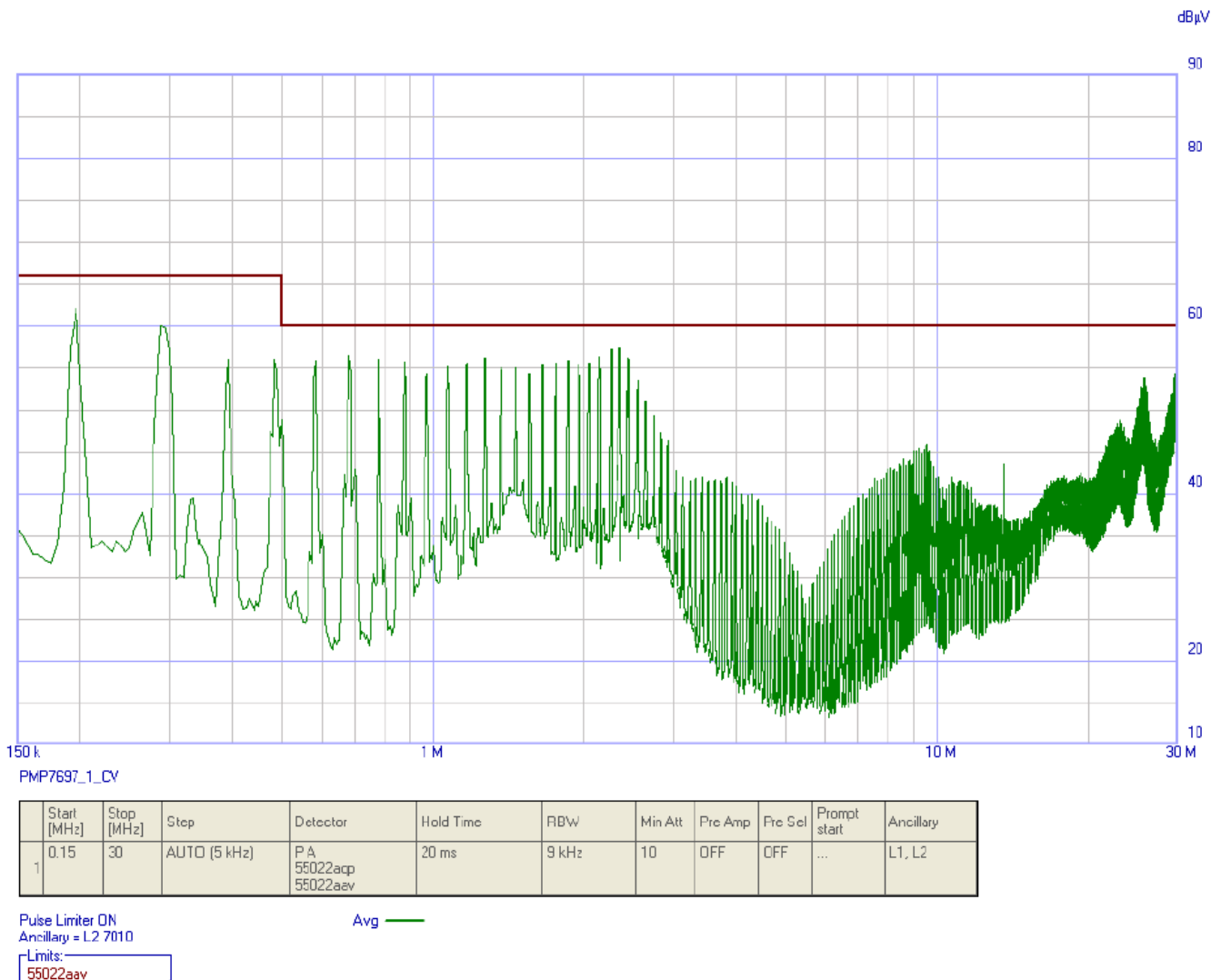
Figure 24. Conducted Average Emissions at Full Load

7.3.2 Emissions at Deep CC Load

Generally conducted emissions will be more at full load. However, the LLC-stage operating frequency is at its maximum in deep CC operating point. So this operating point is also chosen for measuring conducted EMI to verify if the increased operating frequency causes increased EMI.

230-V AC input, 25-V, 9-A simulated battery load connected to PSU output with short leads.

The conducted peak emissions in a pre-compliance test set-up were compared against EN55022 Class-A quasi-peak limits and found to be meeting them comfortably. So the quasi-peak emissions can also meet them easily.
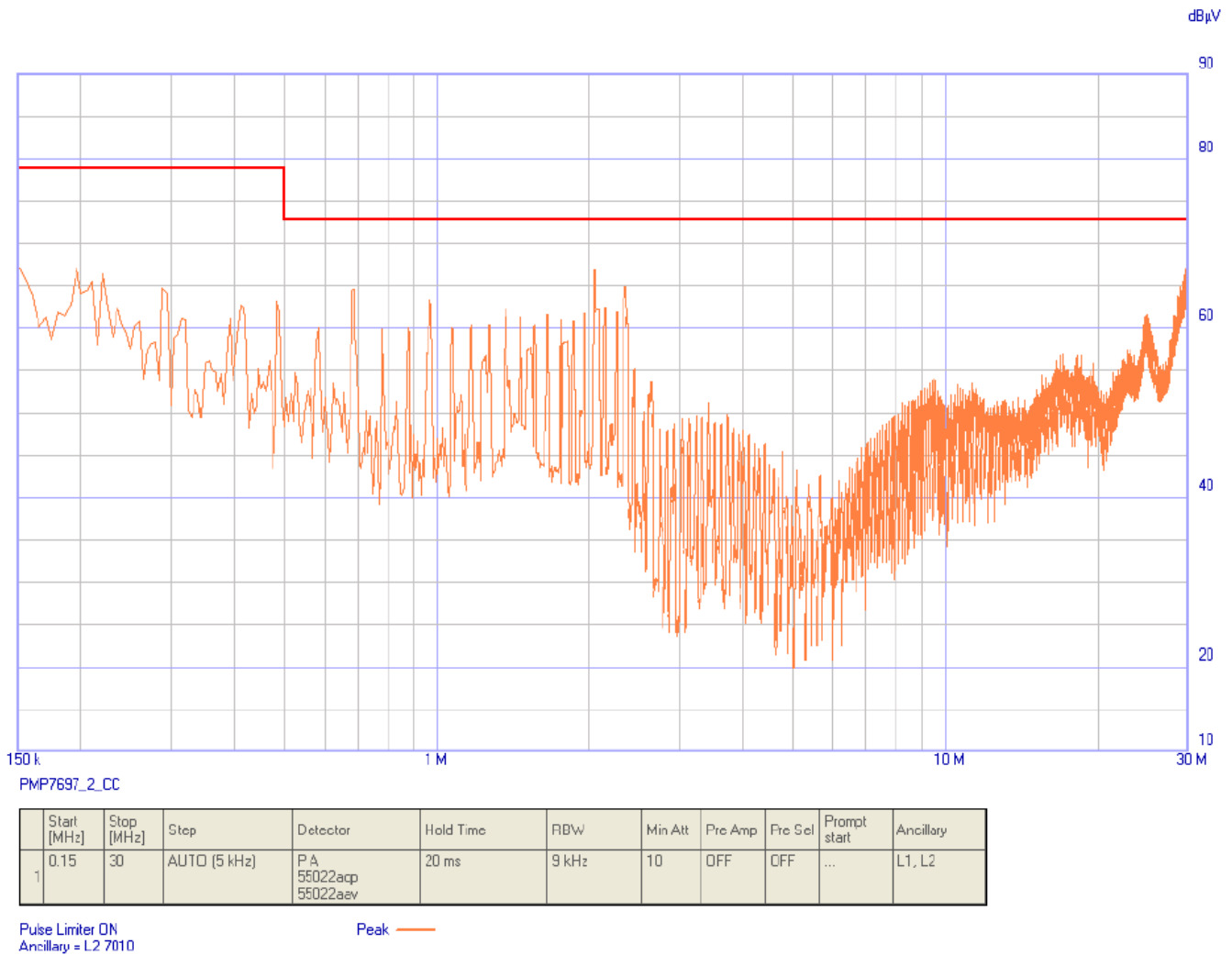
Figure 25. Conducted Peak Emissions at Deep CC Load

230-V AC input, 25-V, 9-A simulated battery load connected to PSU output with short leads.

The conducted average emissions in a pre-compliance test set-up were compared against EN55022 Class-A average limits and found to be meeting them.

	Start [MHz]	Stop [MHz]	Step	Detector	Hold Time	RBW	Min Att	Pre Amp	Pre Sel	Prompt start	Ancillary
1	0.15	30	AUTO (5 kHz)	P A 55022aqp 55022aav	20 ms	9 kHz	10	OFF	OFF	...	L1, L2

Pulse Limiter ON
Ancillary = L2 7010   Avg ——
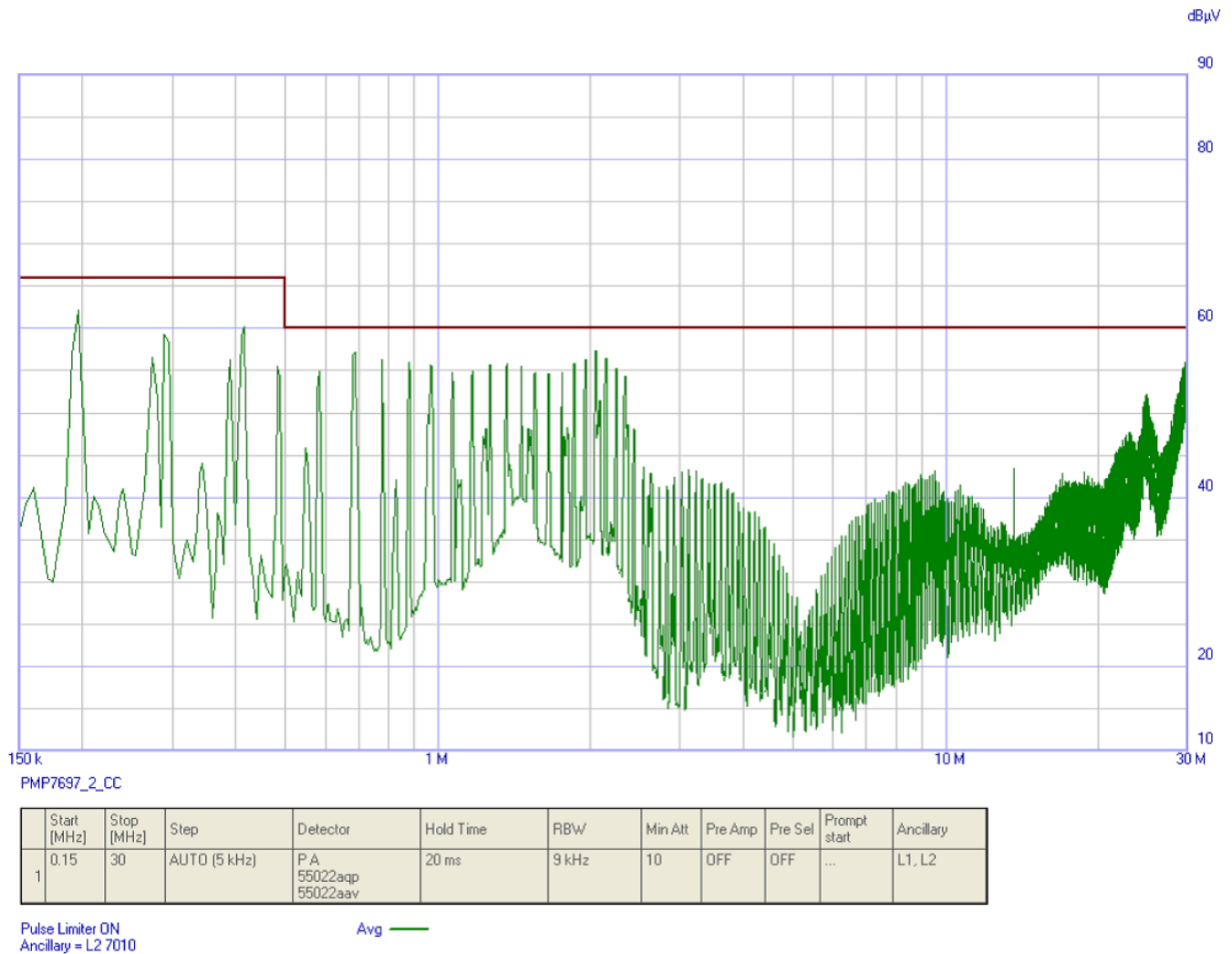
Figure 26. Conducted Average Emissions at Deep CC Load

8   Design Files

8.1   *Schematics*

To download the most recent schematics, see the design files at TIDA-00355.

8.2   *Bill of Materials*

To download the most recent bill of materials (BOM), see the design files at TIDA-00355.

8.3   *PCB Layout Recommendations*

A careful PCB layout is critical for proper operation of power electronics devices. As with all switching power supplies, attention to detail in the layout can save much time in troubleshooting later on.

8.3.1   Power Stage Specific Guidelines

Key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents, on both the primary and secondary sides of the converter. This will help reduce EMI and improve converter overall performance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces.
- Keep power ground and control ground separately for each power supply stage. If they are electronically connected, tie them together in one point near DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, layout should be symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher peak currents and become hotter (i^2R).
- Tie the heat-sinks of all the power switching components to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and routed with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current per IPC2152 as well as acceptable DC and AC impedances. Also, the traces should withstand the fault currents (such as short circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various circuits according to the requirements of applicable standards, such as UL60950.
- Adapt thermal management to fit the end-equipment requirements.

8.3.2   Controller Specific Guidelines

Key guidelines for routing of controller components and signal circuits:

- The optimum placement of decoupling capacitor is closest to the VCC and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection and the GND terminal of the IC.
- The reference ground for the device, a low current signal ground (SGND), should be a copper plane or island.
- Locate all controller support components at specific signal pins (VSENSE, VCOMP, ISENSE, ICOMP, FREQ) close to their connection pin. Connect the other end of the component to the SGND with shortest trace length.
- The trace routing for the voltage sensing and current sensing circuit components to the device should be as short as possible to reduce parasitic effects on the current limit and current/voltage monitoring accuracy. These traces should not have any coupling to switching signals on the board.
- The SGND plane must be connected to high current ground (main power ground) at a single point that is at the negative terminal of DC input or output capacitor respectively.

8.3.3   Layer Plots

To download the most recent layer plots, see the design files at TIDA-00355.

8.4   Altium Project

To download the most recent Altium project files, see the design files at TIDA-00355.

8.5   Gerber Files

To download the most recent Gerber files, see the design files at TIDA-00355.

8.6   Assembly Drawings

To download the most recent assembly drawings, see the design files at TIDA-00355.

9   References

1. Texas Instruments, *Designing an LLC Resonant Half-Bridge Power Converter*, Power Supply Design Seminar: SEM1900, Topic 3 (SLUP263)
2. Texas Instruments, *Feedback Loop Design of an LLC Resonant Power Converter*, Application Report (SLUA582)
3. Texas Instruments, *A Design Review of a Full-Featured 350-W Offline Power Converter*, SEM2000, Topic 2, (TIDU186)
4. Texas Instruments, *Exposing the Inner Behavior of a Quasi-Resonant Flyback Converter*, SEM2000, Topic 3 (SLUP302)
5. Texas Instrument, *Snubber Circuits: Theory, Design and Applications* (SLUP100)
6. Texas Instruments, *UCC28722/UCC28720 5W USB BJT Flyback Design Example*, Application Report (SLUA700)
7. S. Y. R. Hui and H. Chung, *Resonant and Soft-Switching Converters*, In: M. H. Rashid, Ed., Power Electronics Handbook, Academic Press, Cambridge, 2000, pp. 271 – 304.

9.1   Trademarks

10   About the Author

SALIL CHELLAPPAN is a lead engineer, member, and group technical staff at Texas Instruments, where he is responsible for developing customized power solutions as part of the Power Design Services group. Salil brings to this role his extensive experience in power electronics, power conversion, EMI/EMC, power and signal integrity, and analog circuits design spanning many high-profile organizations. Salil holds a bachelor of technology degree from the University of Kerala.

LATIF AMEER BABU is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Latif brings to this role his extensive experience in power electronics, high-frequency DC-DC converter, and analog circuit design. Latif earned his master of technology in power electronics and power systems from Indian Institute of Technology, Mumbai; IN. Latif is a member of the Institute of Electrical and Electronics Engineers (IEEE).

Revision History A and B

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2015) to B Revision   **Page**

- Changed title from *230-V, 400-W High Efficiency Battery Charger With PFC and LLC for 36-V Power Tools* to *230-V, 400-W, 92% High Efficiency Battery Charger With PFC and LLC for 36-V Power Tools Reference Design* 1

Revision History C

Changes from B Revision (May 2016) to C Revision **Page**