TI Designs
330-W, >93% Efficiency, Cost Optimized, 20- to 32-V Storage Battery Bank Charger Reference Design

Description

The TIDA-00704 is a compact, universal input, 20- to 30-V DC, 330-W output, AC/DC storage battery bank charger for 8-cell LiFePO4 batteries. The circuit consists of a front-end continuous conduction mode (CCM) power factor correction (PFC) circuit, followed by an LLC stage for isolated DC/DC conversion. The design uses the UCC29950 combo controller, which controls both the PFC stage and LLC stage, to achieve a compact and robust control structure. For high efficiency needs, synchronous rectification is done using the UCC24610 and low $R_{DS(on)}$ MOSFETs. The board is able to gain an MCU interface for programmable battery charge profiling. This TI Design can be used as a AC/DC supply in many applications demanding efficient power conversion.

Resources

TIDA-00704	Design Folder
UCC29950	Product Folder
UCC24610	Product Folder
LM258	Product Folder
TLV1117	Product Folder
CSD19501KCS	Product Folder

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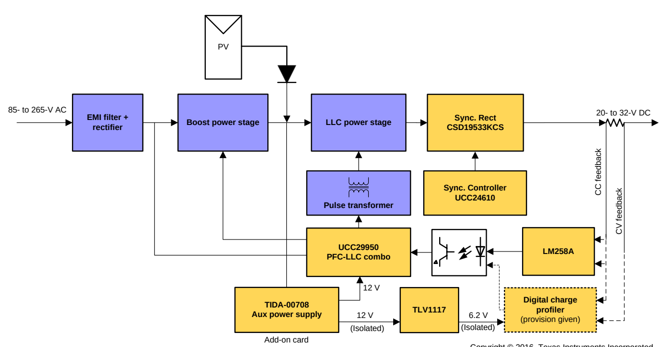
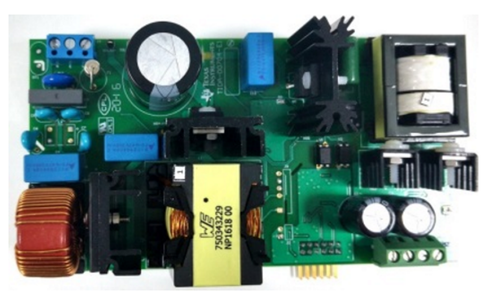
Features

- Ideal Charger for 8-Cell LiFePO4 Battery Pack Used in Storage Battery Banks
- Delivers Full Charging Current Over Entire AC Input Range: –85- to 25-V AC
- Very Low Standby Power of < 100 mW When Battery is Not Connected
- Provision to Connect an Additional External Power Source From Renewable Energy Sources
- Peak Overall Efficiency of > 93% at 230-V AC and > 90% at 115-V AC With No Force Cooling Needed Under 60°C Ambient
- High Power Factor > 0.99 and Meets PFC Regulations and Current THD as per IEC 61000-3-2 Class A
- Provision for Battery Charge Profiling Control Through a Small Add-on Card
- True Input Power Limit, Independent of Line Converter Stage
- Compact form-factor: 150 mm × 80 mm

Applications

- Energy Storage Systems
- Battery Chargers
- Single-Phase UPS
- Industrial Power Supplies
- Power Tools
- High Bay Lighting
- E-Bikes





1 System Overview

1.1 System Description

This design is a compact, universal AC input, 20- to 32-V DC, 320-W output, AC/DC storage battery bank charger for 8-cell LiFePO4 batteries. The circuit consists of a front-end continuous conduction mode (CCM) power factor correction (PFC) circuit, followed by an LLC-based second stage. The design uses the UCC29950 combo controller, which controls both the PFC stage and LLC stage, to achieve a compact and robust control structure. Synchronous rectification based on the UCC24610 and low $R_{DS(on)}$ FETs from Texas instruments help in achieving higher efficiencies. The board comes with an option for customizable battery charge profiling, by means of a small daughter card based on the MSP430 controller. Apart from the input mains supply, the design also supports an additional power source connected to the DC link through a diode. This can be used for drawing power from any local renewable energy sources like PV panels.

Although primarily intended for battery chargers, this TI Design can be used for all applications demanding efficient AC/DC power conversion from universal AC input mains to 20- to 32-V isolated DC output. The system design is done to meet high efficiency, low EMI, and low standby power consumption specifications.

The charger is designed for an input voltage range of 85- to 265-V AC and used to charge batteries up to 32 V at a maximum current of 11 A. The design form factor (150 mm × 80 mm) is compact for the power level of 320 W. The design has an operating peak efficiency of around 94% at full load with voltage and current regulation within ±2%.

The EMI filter at the front end of the circuit is designed to meet EN55022 class-A conducted emission levels. This is followed by an active boost PFC stage operating in CCM. This PFC stage regulates the DC bus voltage to 400 V, stabilized against line drop-outs with a bulk storage capacitor. The isolated power stage of the charger is an LLC resonant converter operating very close to resonant frequency at a 28-V output. The operation will move to above or below resonance according to the voltage and current requirements of the charger. The CV/CC feedback is achieved using LM258 op-amp circuit, which has integrated dual op amps. A TL431 device generates the required reference levels for the feedback circuitry. There is provision to alter the voltage and current references by means of a small external add-on-card for battery charge profiling. The system is designed to meet below 100 mW of standby power when no battery is connected. This is achieved using a simple logic circuit that disables PFC and LLC power stages when battery is not present.

The design uses a 5-W housekeeping power supply board (TIDA-00708), which is designed to meet the auxiliary needs of a general power supply. It supports an input voltage range from 100- to 450-V DC and provides a 3.5-V DC (1.5-W) and 12-V DC (2.5-W) non-isolated outputs. In addition, a 12-V DC (1-W) isolated output is also provided to support isolated auxiliary power needs. The features of the power supply board include easy pluggability, compact size, high efficiency, low no-load power consumption, and low cost. Find more details of this power supply in the design guide of the power supply, the TIDA-00708 (TIDUBK7).

This TI Design meets the key challenges of battery chargers to provide safe and reliable battery charging with all protections built in, while delivering high performance with low power consumption and a low bill-of-material (BOM) cost. Various parameters of the design like regulation, efficiency, EMI signature, output ripple, startup and switching stresses were tested and documented.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage (V_{INAC})	—	85	230	270	VAC
Frequency (f_{LINE})	—	47	50	63	Hz
Standby power (P_{SB})	Battery not connected	—	100	—	mW
OUTPUT CONDITIONS					
Output voltage	—	20	—	32	V
Output current	—	—	10	11	A
Line regulation	Both current and voltage	—	—	0.5	%
Load regulation	Both current and voltage	—	—	2	%
Output voltage ripple	Peak to peak	—	200	—	mV
Output power (P_O)	—	—	—	330	W
SYSTEM CHARACTERISTICS					
Efficiency (η)	$V_{IN} = V_{NOM}$ and full load at 29-V output	—	92.1	—	%
	$V_{IN} = V_{NOM}$ and 230-W load at 29-V output	—	93.2	—	%
Protections	Output overcurrent	—	—	—	—
	Output overvoltage	—	—	—	—
	Output undervoltage	—	—	—	—
Operating ambient	Open frame	–10	25	55	°C
Standards and norms	Power line harmonics	As per EN55011 / EN55022 Class A			
	EFT	As per IEC-61000-4-4			
Board form factor (FR4 material, 2 layer)	Length × Breadth × Height	150 × 85 × 40			mm

1.3 Block Diagram

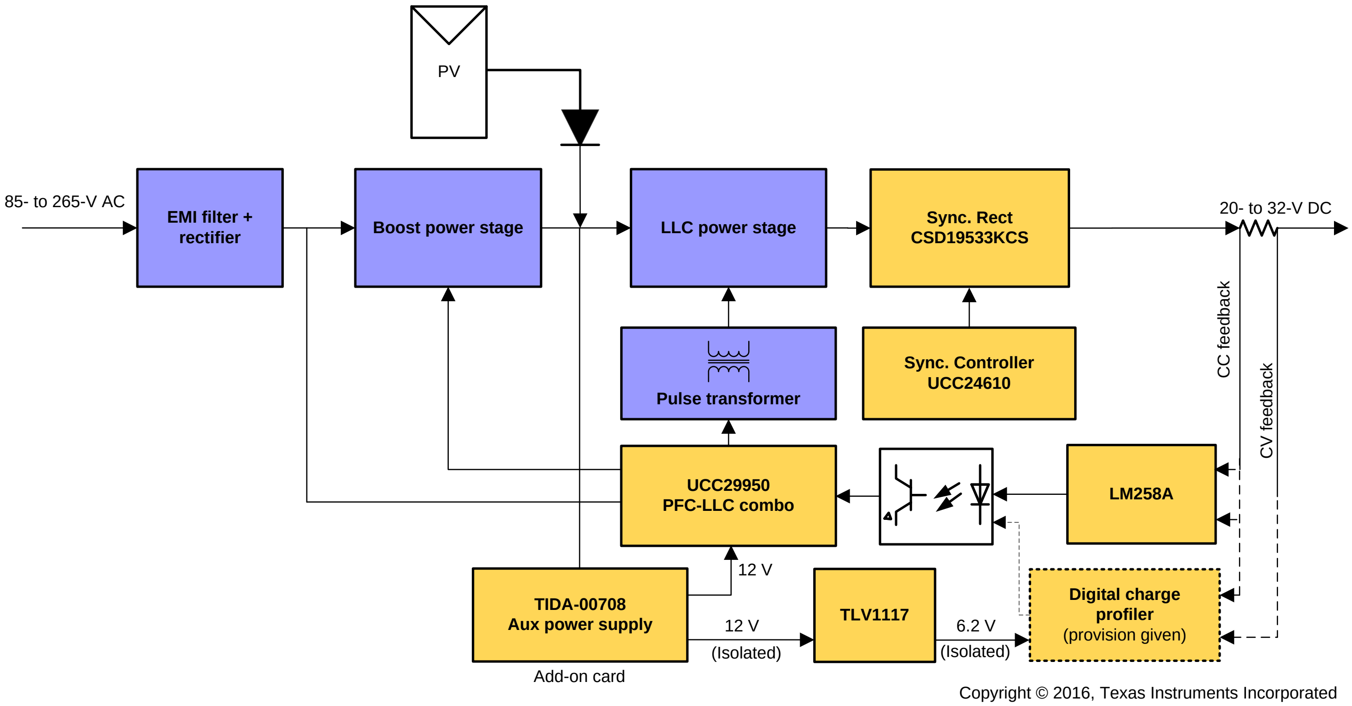


Figure 1. Block Diagram of Battery Charger

1.4 Highlighted Products

The following highlighted products are used in this reference design. Key features for selecting the devices for this reference design are revealed in the following sections. Find more details of the highlighted devices in their respective product datasheets.

1.4.1 UCC29950—CCM PFC and LLC Combo Controller

To implement a high-performance PFC plus LLC-based power supply, the UCC29950 is the preferred controller as it offers a series of benefits to address the next generation needs. The UCC29950 provides all the control functionality for an AC-to-DC converter with a CCM boost PFC stage followed by an LLC converter stage. The controller is optimized to allow ease of use. Proprietary CCM PFC algorithms enable the system to achieve high efficiency and smaller converter size with high power factor. The integrated LLC controller enables a high-efficiency DC-to-DC conversion stage using soft switching for low EMI noise. Integration of PFC control and LLC control in a combo controller allows the control algorithms to take advantage of information from both stages.

The controller includes a control circuit for start-up using a depletion mode MOSFET with internal device power management that minimizes external component requirements and helps lower system implementation costs. To further reduce the standby power, an X-Cap discharge circuit is integrated. The UCC29950 implements a complete suite of system protection functions, including AC line brownout, PFC bus undervoltage PFC and LLC, overcurrent, and thermal shutdown.

Some of the key features of the UCC29950 controller are:

- CCM boost PFC
- Supports self-bias or auxiliary (external) bias mode of operation
- PFC loops fully internally compensated
- Fixed 100-kHz PFC frequency with dithering for ease of EMI compliance
- True input power limit, independent of line voltage
- Fixed LLC frequency operating range of 70 to 350 kHz

- Dead-time varied across load range for LLC half-bridge power stage to extend ZVS range
- Three-level LLC overcurrent protection
- Hiccup mode operation for continuous overload and short-circuit power protection
- Low standby power consumption enabled by active control of high-voltage start-up MOSFET and X-Cap discharge function
- Built-in soft-start and converter sequencing to simplify design
- AC line brownout protection with fail indicator
- PFC bus overvoltage and undervoltage protection
- Over-temperature protection

1.4.2 UCC24610—Secondary Side Synchronous Rectifier Controller

To achieve higher efficiencies at low output voltages, synchronous rectification is inevitable. In order to achieve high reliability and avoid false triggering and related failures of synchronous rectifiers, it requires a highly reliable, proven, and fail-proof controller. The UCC24610 is an ideal choice as it meets all the requirements of a synchronous rectifier controller for LLC converters.

The UCC24610 is a high-performance controller and driver for standard and logic-level N-channel MOSFET power devices used for low-voltage secondary-side synchronous rectification. The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier but also indirectly reduces primary-side losses as well, due to compounding of efficiency gains. Using drain-to-source voltage sensing, the UCC24610 is ideal for LLC-resonant power supplies.

The UCC24610 offers a programmable false-triggering filter, a programmable timer to automatically switch to light-load mode at light load, and a SYNC input for optional use in CCM systems. Protection features on TON and EN/TOFF pins prevent run-away on-time due to open-circuit or short-circuit fault conditions. This device is available in an 8-pin SOIC package and an 8-pin, 3.0-mm × 3.0-mm SON package with an exposed thermal pad.

Other key features include:

- Up to 600-kHz operating frequency
- VDS MOSFET sensing
- 1.6-Ω sink, 2.0-Ω source gate-drive impedances
- Micro-power sleep current for 90+ designs
- Automatic light-load management
- Synchronous wake-up from sleep and light-load modes
- Protection features on programming inputs
- 20-ns typical turnoff propagation delay
- Improved efficiency and design flexibility over traditional diode solution

1.4.3 LM258A—Operational Amplifiers

Both voltage and current control loop compensation is performed using the widely proven and cost effective LM258 dual op amp. Some key features that make it extremely suitable for loop compensation in the present design include:

- Also works on single supply: 3 to 32 V
- Low supply-current drain, independent of supply voltage: 0.7 mA typical
- Wide unity gain bandwidth : 0.7 MHz
- Low input bias and offset parameters input offset voltage: 2 mV typical
- Input offset current: 2 nA typical
- Input bias current: 15 nA typical
- Differential input voltage range equal to maximum-rated supply voltage: 32 V
- Open-loop differential voltage gain: 100 dB typical
- Internal frequency compensation

1.4.4 TLV1117—Linear Regulator

This design uses the TLV1117 linear regulator to generate regulated 6.1-V DC output for supplying the UCC24610 synchronous rectifier controller and the LM258 op amp. Input to the TLV1117 circuit is the 12-V isolated output generated by the TIDA-00708 board and output is adjusted to be 6.1-V DC to support the UCC24610 for efficiently driving non-logic level FETS. The 6.1-V DC output generated by the TLV1117 circuit is also used as the bias supply for the battery charge profiling add-on card (not part of the TIDA-00704). Some of the key features of the TLV1117 that make it suitable for use in this design include:

- 15-V maximum input voltage
- 0.2% line regulation maximum
- Adjustable output
- –40°C to 125°C specified junction temperature range

1.4.5 CSD19501KCS—80-V, 5.5-mΩ, TO-220 NexFET Power MOSFET

In order to achieve high-efficiency synchronous rectification, TI’s power MOSFET CSD19501KCS has been employed in this design. This is an 80-V rated FET with an extremely low on-state resistance of 5.5 mΩ. Some additional features that make this FET suitable for the present design include:

- Ultra-low Qg and Qgd
- Low thermal resistance
- Avalanche rated
- TO-220 plastic package

1.4.6 Bias Power

An auxiliary housekeeping power supply is needed to power the ICs on the board. An add-on auxiliary power supply board (TIDA-00708) of 5 W is used for this purpose. This board is based on a flyback design using the high-voltage off-line switcher UCC28881. The TIDA-00708 provides one 12-V non-isolated and one 12-V isolated output for the auxiliary power needs of the TIDA-00704 board. For more details, see the TIDA-00708 design guide (TIDUBK7). Note that the auxiliary power supply TIDA-00708 is already mounted on the TIDA-00704 board and hence is an integral part of it.

2 System Design Theory

The design process starts by deciding on the component values in the LLC power train and then moving to the PFC stage.

2.1 LLC Design Goal Parameters

Table 2 shows the design goal parameters for the LLC stage.

Table 2. Design Parameters for LLC Power Stage Design

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{INDC}	Input voltage	375	400	410	VDC
OUTPUT					
V_{OUT}	Output voltage	20	30	32	VDC
P_{LIMIT}	Output power limit	—	—	320	W
P_{OUT}	Max output power	—	—	320	W
f_{SWNOM}	Nominal switching frequency	70	120	250	kHz
—	Line regulation	—	1	—	%
—	Load regulation	—	1	—	%
η	Targeted efficiency	—	0.95	—	%

2.2 LLC Circuit Component Design

One of the reasons that LLC topology is so popular is that it can achieve zero voltage switching (ZVS) over a wide range of operating conditions. ZVS is important because it reduces switching losses in the power devices. The schematic for a basic LLC is shown in Figure 2.

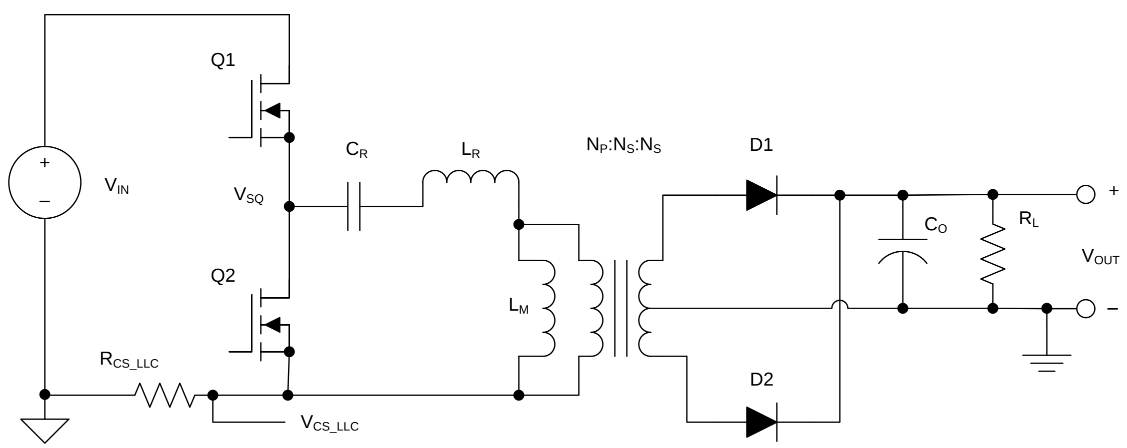


Figure 2. Schematic for Basic LLC Circuit

2.2.1 Design Approach for Battery Charger Application

LLC topology has been widely used in telecom and server power supplies. LLC topology needs to generate a constant output voltage for a wide input DC voltages ranging from 400- to 200-V DC. For battery charging applications, the situation is different; the output voltage needs to be variable while the input voltage is almost constant (390- to 410-V DC). Hence the design procedure also needs to be slightly modified. As stated previously, the output voltage requirement ranges from 20- to 32-V DC. Therefore, the converter will be designed to operate at resonance (second resonance) when generating 26 V. The converter will operate above and below the resonant frequency when generating voltages below and above 26-V DC, respectively.

2.2.2 Switching Frequency

The minimum switching frequency of the UCC29950 is fixed at 70 kHz to accommodate enough room for voltage boost, and also to make the transformer with a smaller, nominal switching frequency (corresponding to second resonant frequency is chosen to be 100 kHz).

2.2.3 LLC Transformer Turns Ratio

The transformer turns ratio is given by Equation 1:

$$N = \frac{\frac{V_{IN}}{2}}{V_{OUT}} = \frac{200}{29} = 7.14 \approx 7 \tag{1}$$

where

- V_{IN} is the voltage on the bulk capacitor

This is regulated at 400-V DC. No additional diode drop needs to be accounted for because a synchronous rectifier is used. Further, it is aimed that the converter operates at resonance when delivering a 28-V DC output.

2.2.4 LLC Stage Equivalent Load Resistance

This is the effective load resistance reflected through the transformer turns ratio. R_E is determined at the full load point with Equation 2.

$$R_E = \frac{8N^2}{\pi^2} R_L = 8 \times \frac{7^2}{\pi^2} \times \frac{28}{11} = 101\ \Omega \tag{2}$$

2.2.5 LLC Gain Range

These parameters set the gain range required of the LLC stage. Note that $V_{IN(min})$ and $V_{IN(max)}$ are taken as 410- and 380-V DC.

$$M_{G(min)} = N \frac{V_{OUT(min)}}{\frac{V_{IN(max)}}{2}} = 7 \times \frac{20}{200} = 0.7 \tag{3}$$

$$M_{G(max)} = N \frac{V_{OUT(max)}}{\frac{V_{IN(min)}}{2}} = 7 \times \frac{30}{200} = 1.05 \tag{4}$$

Figure 3 shows the LLC stage gain versus normalized switching frequency curves for various quality factors (Q_E). The definition of quality factor is provided in the next subsection.

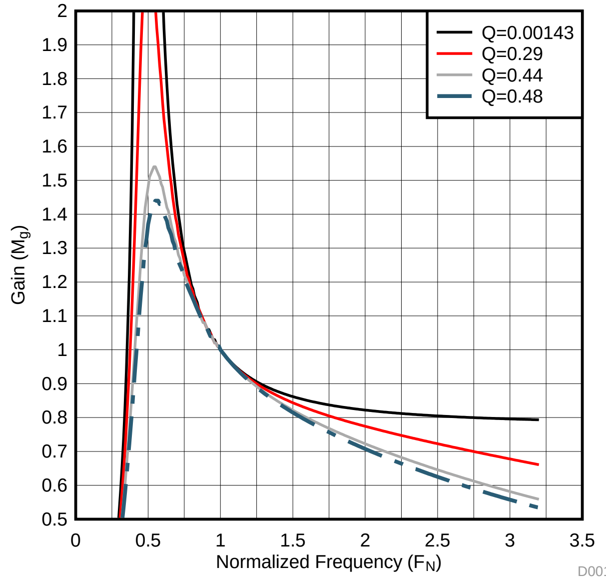


Figure 3. LLC Stage Gain Curve

2.2.6 Select L_N and Q_E

From Figure 4, select suitable L_N and Q_E values to meet the $M_{G(min)}$ and $M_{G(max)}$ values calculated.

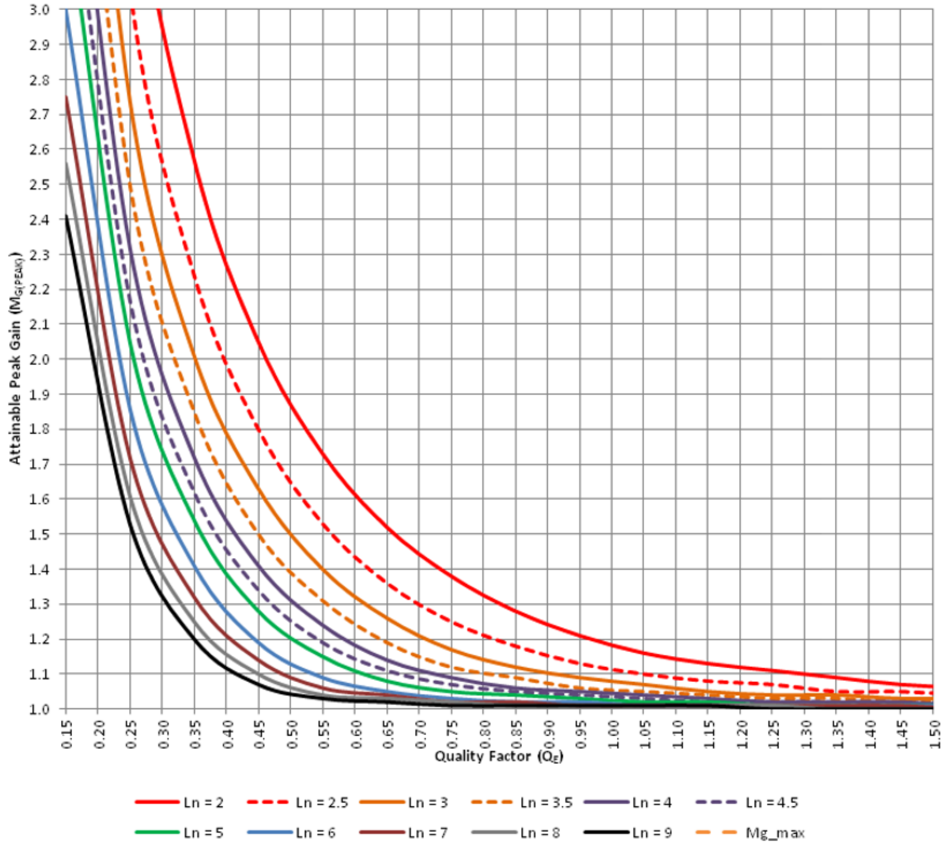


Figure 4. Quality Factor versus Peak Gain Curves for Various Values of L_N

L_N is the primary inductance ratio and is given by:

$$L_N = N\frac{L_M}{L_R} = 6 \tag{5}$$

Q_E is the quality factor of the resonant network.

$$Q_E = \frac{\sqrt{\frac{L_R}{C_R}}}{R_E} = 0.5 \tag{6}$$

Set L_N = 6 and Q_E = 0.5 for this application. The following LLC peak gain curves show a maximum that is greater than the required maximum gain $M_{G(max)}$.

2.2.7 LLC No-Load Gain

The minimum gain required at no load is:

$$M_{G(\infty)} = \frac{L_N}{L_N + 1} = \frac{6}{6+1} = 0.86 \tag{7}$$

Figure 3 shows that the design can achieve a minimum gain of 0.86 at the maximum frequency of the UCC29950 (290 kHz or 2.9 times the normalized f_0 of 100 kHz). If the gain is too high, then the UCC29950 enters a burst mode of operation to keep the output voltage under control.

2.2.8 Parameters of LLC Resonant Circuit

The value of the resonant capacitor is given by Equation 8:

$$C_R = \frac{1}{2\pi \times f_{SW} \times R_E \times Q_E} = \frac{1}{2\pi \times 100\ \text{kHz} \times 101 \times 0.5} = 31.5\ \text{nF} \approx 33\ \text{nF} \quad (8)$$

The resonant inductor is given by Equation 9:

$$L_R = \frac{1}{(2\pi \times f_{SW})^2 \times C_R} = \frac{1}{(2\pi \times 100\ \text{kHz})^2 \times 32\ \text{nF}} = 79.2\ \mu\text{H} \quad (9)$$

Rearranging Equation 5 gives a value for L_M, the transformer magnetizing inductance:

$$L_M = L_N \times L_R = 6 \times 79.2\ \mu\text{H} \approx 480\ \mu\text{H} \quad (10)$$

2.2.9 Verify LLC Resonant Circuit Design

The series resonant frequency is given by:

$$f_0 = \frac{1}{2\pi\sqrt{L_R \times C_R}} = \frac{1}{2\pi\sqrt{79.2\ \mu\text{H} \times 33\ \text{nF}}} = 98.49\,\text{kHz} \quad (11)$$

The inductance ratio is given by:

$$L_N = \frac{L_M}{L_R} = \frac{480\ \mu\text{H}}{79.2\ \mu\text{H}} \approx 6 \quad (12)$$

The quality factor at full load is given by:

$$f_0 = \frac{\sqrt{\frac{L_R}{C_R}}}{R_E} = \frac{\sqrt{\frac{79.2\ \mu\text{H}}{33\ \text{nF}}}}{101} \approx 0.49 \quad (13)$$

This differs from the initial value of 0.5 because a rounded value for C_R is used here and in the calculation of L_R. However, the difference is not significant.

Figure 5 has been normalized to the series resonant frequency, which is 100 kHz in this example. At the minimum gain condition with a minimum output voltage of 20 V and a maximum input voltage ($M_{G(min)}$), the frequency is 2.1 times f_0 or $f_{SW(max)}$ = 210 kHz. At the maximum gain condition with a maximum output voltage of 32 V and a minimum input voltage ($M_{G(max)}$), the frequency is 0.7 times f0 or $f_{SW(min)}$ = 70 kHz.

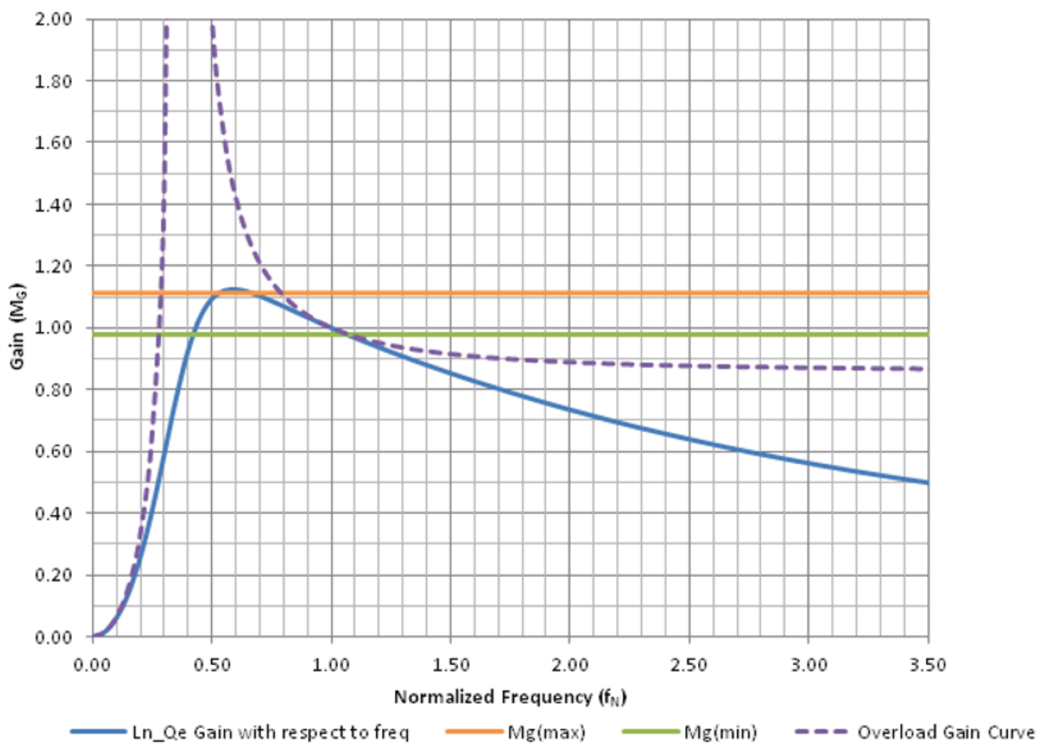


Figure 5. LLC Gain Curve With Selected L_N and Q_E

2.2.10 LLC Primary-Side Currents

The primary-side RMS load current is given by:

$$I_{OE} = \frac{\pi}{2\sqrt{2}} \times \frac{1}{N} \times I_O = \frac{\pi}{2\sqrt{2}} \times \frac{1}{7} \times 11 = 1.74\text{ A} \tag{14}$$

The approximate RMS magnetizing current at the minimum switching frequency is:

$$I_M = \frac{1}{2\sqrt{3}} \times \frac{N \times V_{OUT(max)}}{f_{min} \times L_m} = \frac{1}{2\sqrt{3}} \times \frac{7 \times 32}{70\text{ kHz} \times 480\ \mu\text{H}} = 1.92 \tag{15}$$

The total current in the resonant circuit is then given by:

$$I_R = I_{WP} = I_{CR} = \sqrt{I_M{}^2 + I_{OE}{}^2} = \sqrt{1.74^2 + 1.92^2} = 2.59\text{ A} \tag{16}$$

This current also flows in the transformer primary winding (I_{WP}) and the resonant capacitor (I_{CR}).

2.2.11 LLC Secondary-Side Currents

The total secondary-side RMS current is the current referred from the primary side (I_{OE}) to the secondary side.

$$I_{OE(S)} = N \times I_{OE(S)} = 7 \times 1.74 = 12.2\text{ A} \tag{17}$$

The design uses a center tapped secondary so that this current is shared equally between the two windings. The current in each winding is then:

$$I_{WS} = \frac{I_{OE(S)}\sqrt{2}}{2} = \frac{12.2}{\sqrt{2}} = 8.63\text{ A} \tag{18}$$

This value goes higher as the secondary voltage goes higher (as operation goes below resonance). The half-wave average current in the secondary windings is:

$$I_{SAV} = \frac{I_{OE(S)}\sqrt{2}}{\pi} = \frac{12.2\sqrt{2}}{\pi} = 5.5\ \text{A} \quad (19)$$

2.2.12 LLC Transformer

The resonant inductor can be integrated into the transformer to reduce the size of the magnetics. The transformer can be built or purchased according to these specifications:

- Turns ratio (N): 7
- Primary magnetizing inductance: L_M = 480 μH
- Primary terminal voltage: 270-V AC (= 32 × 7 × 1.2)
- Primary winding rated current: I_{WP} = 2.59 A
- Secondary terminal voltage: 56-V AC
- Secondary winding rated current: I_{WS} = 10 A
- Maximum operating frequency: $f_{SW(max)}$ = 350 kHz
- Minimum operating frequency: $f_{SW(min)}$ = 70 kHz
- Reinforced insulation barrier from primary-to-secondary to IEC60950

The minimum operating frequency during normal operation is that calculated above but during shutdown the LLC can operate at LLC_{FMIN}. The magnetic components in the resonant circuit, the transformer, and resonant inductor must be rated to operate at this lower frequency.

2.2.13 LLC Resonant Capacitor

This capacitor carries the full-primary current at a high frequency. A low dissipation factor part is needed to prevent overheating in the part.

The AC voltage across the resonant capacitor is given by its impedance times the current.

$$V_{CR} = \frac{I_{CR}}{\omega_{min} \times C_R} = \frac{2.59}{2\pi \times 70\ \text{kHz} \times 33\ \text{nF}} = 179\ \text{V} \quad (20)$$

$$V_{CR(RMS)} = \sqrt{\left(\frac{V_{IN(max)}}{2}\right)^2 + V_{CR}^{\ 2}} = \sqrt{200^2 + 179^2} = 268\ \text{V} \quad (21)$$

And the corresponding peak voltage:

$$V_{CR(PEAK)} = \frac{V_{IN(max)}}{2} + \sqrt{2} \times V_{CR} = \frac{400\ \text{V}}{2} + \sqrt{2} \times 268 = 453\ \text{V} \quad (22)$$

The part selected must meet these specifications:

- Rated current: I_{CR} = 2.59 A
- AC voltage: $V_{CR(peak)}$ = 434 V

This capacitor must also be able to take three times this voltage for short time, which corresponds to the peak overcurrent limit.

2.2.14 LLC Primary-Side MOSFETs

V_{IN} appears across the MOSFET, which is not conducting. The voltage rating must then be above:

$$V_{Q1(PEAK)} = V_{Q2(PEAK)} > V_{IN} \approx 500\ \text{V} \quad (23)$$

IPP60R190P6 MOSFET with 600 V and a 20-A rating is chosen to meet the efficiency targets and give enough voltage margin to accommodate surge tests.

2.2.15 LLC Output Rectifier Diodes

The minimum voltage rating for the output diodes is given by:

$$V_{DB} = 2 \times V_{O(max)} = 64\ \text{V} \tag{24}$$

Voltage rating of the output diode is selected as 80 V.

The current rating for the output diodes is given by:

$$I_{SAV} = \frac{\sqrt{2} \times 12.2}{\pi} = 5.5\ \text{A} \tag{25}$$

2.2.16 LLC Stage Output Capacitors

The LLC converter topology does not require an output filter, but a small second stage filter inductor may be useful in reducing peak-to-peak output noise.

Assuming that the output capacitors carry the rectifier's full wave output current then the capacitor ripple current rating is:

$$I_{RECT} = I_{SW} = \frac{\pi}{2\sqrt{2}} \times I_{OUT} = \frac{\pi}{2\sqrt{2}} \times 11 = 12.2 \tag{26}$$

The capacitor's RMS current rating at 70 kHz is:

$$I_{C(OUT)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times I_{OUT}\right)^2 - I_{OUT}^2} = 0.483 \times 11 = 5.313 \tag{27}$$

Solid aluminum capacitors with conductive polymer technology have high ripple-current ratings and are a good choice here. The ripple-current rating for a single capacitor may not be sufficient, so multiple capacitors are often connected in parallel.

The ripple voltage at the output of the LLC stage is a function of the amount of AC current that flows in the capacitors. To estimate this voltage, assume that all the current, including the DC current in the load, flows in the filter capacitors.

$$ESR_{MAX} = \frac{300\ \text{mV}}{12.2\sqrt{2}} = 17.4\ \text{m}\Omega \tag{28}$$

The capacitor specifications are:

- Voltage rating: 50 V
- Ripple current rating: 5.313 A at 70 kHz
- ESR: < 17.4 mΩ

2.2.17 LLC Stage Overcurrent Protection, Current Sense Resistor

The LLC stage input current contains a significant component at the switching frequency in additional to a DC component. Only the DC component is proportional to the load current. This means that the signal must be filtered before it is applied to the LLC_CS pin of the UCC29950. The degree of filtering is a compromise between response time and accuracy.

An RC filter with a pole at about 3 kHz is used to filter the signal. An additional capacitor, across the current sense resistor provides a higher frequency pole at approximately 6 kHz.

The LLC current sensing resistor is selected so that the LLC_CS signal is at 90% of the OCP1 level (400 mV × 0.9 = 360 mV) when the converter is operating at full load and nominal input and output conditions. The resistor value is then given by:

$$R_{CS(LLC)} = \frac{R_{CS(LLC)} \times V_{BLK(min)}}{P_{OUT}} = \frac{0.36\ \text{V} \times 370\ \text{V}}{1.1 \times 300\ \text{W}} = 403\ \text{m}\Omega \approx 0.4\ \Omega \tag{29}$$

Assuming there is no ripple current in the current sensing resistor, the full load power dissipated in this resistor is given by:

$$P_{R\_CS(LLC)} = \frac{V_{CS(LLC)}^{2}}{R_{CS(LLC)}} = \frac{(0.36\ V)^2}{400\ m\Omega} = 324\ mW \tag{30}$$

The resistor must be able to dissipate the power due to an overload, which is just lower than the OCP_1 threshold.

$$P_{R\_CS(LLC)} = \frac{V_{CS(OCP1)}^{2}}{R_{CS(LLC)}} = \frac{(0.4\ V)^2}{400\ m\Omega} = 400\ mW \tag{31}$$

2.3 PFC Stage Design Goal Parameters

Table 3 shows the design goal parameters for the PFC stage.

Table 3. Design Parameters for PFC Power Stage Design

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{IN}	Input voltage	85	—	265	VAC
f_{LINE}	Input frequency	47	—	63	Hz
OUTPUT					
V_{OUT}	Output voltage	—	400	—	VDC
P_{OUT}	Output power	—	—	320	W
—	Line regulation	—	—	3	%
—	Load regulation	—	—	3	%
PF	Targeted power factor	—	0.99	—	—
η	Targeted efficiency	—	96	—	%

2.3.1 Design Procedure for PFC Stage

The boost topology operated in CCM is a popular choice for a PFC stage because it has lower component stresses than other topologies. This becomes more important at higher power levels. The schematic for a basic PFC is shown in Figure 6. The basic schematics for the three boost PFC circuits (Discontinuous Conduction Mode (DCM), Transition Mode (TM) and CCM) are the same. The differences relate to whether or not the inductor current is allowed to go to zero for part of the PWM cycle (DCM) and whether the PFC frequency is held constant or used as a control variable.

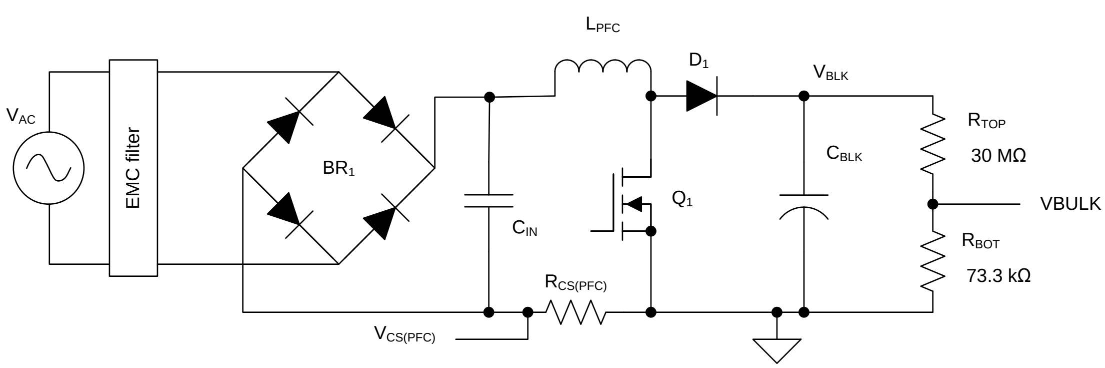


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Figure 6. Basic PFC Schematic

2.3.2 PFC Stage Output Current Calculation

The first step is to determine the maximum load current on the PFC stage, allowing for an overload to 110% of maximum load power.

$$I_{OUT(PFC)} = \frac{110\% \times P_{OUT}}{V_{BLK(min)}} = \frac{1.1 \times 300\,W}{400\,V} = 0.825\,A \tag{32}$$

2.3.3 Line Current Calculation

Next determine the maximum RMS input-line current, allowing for an overload to 110% of maximum load power.

$$I_{LINE(RMS(max))} = \frac{110\% \times P_{OUT}}{\eta V_{AC(min)}} = \frac{1.1 \times 300\,W}{0.9 \times 85\,V} = 4.31\,A \tag{33}$$

The peak line current is:

$$I_{LINE(PEAK(max))} = \sqrt{2} \times I_{LINE(RMS(max))} = \sqrt{2} \times 4.31\,A = 6.1\,A \tag{34}$$

The average line current is given by:

$$I_{LINE(AVG(max))} = \frac{2 \times I_{LINE(PEAK(max))}}{\pi} = \frac{2 \times 6.1\,A}{\pi} = 3.88\,A \tag{35}$$

2.3.4 Bridge Rectifier

A typical bridge rectifier has a forward voltage drop VF_BR of 0.95 V. The power loss in the bridge rectifier can be calculated from:

$$P_{BR} = 2 \times V_{F(BR)} \times I_{LINE(AVG(max))} = 2 \times 0.95\,V \times 3.88\,A = 7.37\,W \tag{36}$$

The bridge rectifier must be rated to carry the full-line current ($I_{LINE(avg\_max)}$). The voltage rating of the bridge must be at least 600 V. The bridge rectifier also carries the full inrush current as the bulk capacitor (C_{BLK}) charges when the line is connected. The amplitude and duration of this current is difficult to determine in advance because it depends on parameters that are hard to predict.

2.3.5 PFC Boost Inductor

The boost inductor is usually chosen so that the peak-to-peak amplitude of the switching frequency ripple current, $I_{HFR(pfc)}$, is between 20% and 40% of the average current at peak of line. This design example uses IHFR_PFC = 30%. Numerically this is, (from Equation 34)

$$I_{HFR} = 0.3 \times I_{LINE(PEAK(max))} = 0.3 \times 6.1\,A = 1.83\,A \tag{37}$$

The minimum boost inductor value is calculated from a worst case duty cycle of 50%.

$$L_{PFC} \geq \frac{V_{BLK}\, D(1-D)}{f_{PFC} \times I_{HFR\_PFC}} = \frac{400 D(1-D)}{98\,kHz \times 1.83\,A} = 557\,\mu H \tag{38}$$

The boost inductor must be able to support a maximum current of:

$$I_{L(PEAK)} = I_{LINE(PEAK(max))} + \frac{I_{HFR\_PFC}}{2} = 6.1\,A + \frac{1.83\,A}{2} = 1.83\,A = 7\,A \tag{39}$$

The boost inductor was selected with the following specifications to allow proper margins:

- L_{PFC} = 750 µH
- Current = 9 A

2.3.6 PFC Input Capacitor

The purpose of the input capacitor is to provide a local, low-impedance source for the high-frequency ripple currents, which flow in the PFC inductor. The allowed voltage ripple on C_{IN} is ΔV_{IN}.

$$\Delta V_{IN} = 5\% \times \sqrt{2} \times V_{AC(min)} = 5\% \times \sqrt{2} \times 85\ V = 6\ V \quad (40)$$

$$C_{IN} = \frac{I_{HFR(PFC)}}{8 \times f_{PFC} \times \Delta V_{IN}} = \frac{1.83\ A}{8 \times 98\ kHz \times 6\ V} = 390\ nF \quad (41)$$

An X2-rated film capacitor of 470 nF is chosen for this application.

2.3.7 PFC Stage MOSFET

The main specifications for the PFC stage MOSFET are:

- B_{VDSS}, drain source breakdown voltage, ≥ 600 V
- $R_{DS(on)}$, on-state drain source resistance, approximately 200 mΩ at 100°C
- t_r, device rise time, 8 ns approximately (Note that this time will vary with change in the gate turn-off resistance)
- t_f, device fall time, 7 ns approximately (Note that this time will vary with change in the gate turn-on resistance)

The losses in the device are calculated in the following calculations. These calculations are approximations because the losses are dependent on parameters, which are not well controlled. For example, the $R_{DS(on)}$ of a MOSFET can vary by a factor of 2 from 25°C to 125°C. Therefore, several iterations may be needed to choose an optimum device for an application different to the one discussed.

The conduction losses are estimated by:

$$P_{Q1(COND)} = \left(\frac{P_{OUT(max)}}{\sqrt{2} \times V_{AC(min)}} \times \sqrt{2 - \frac{16 \times \sqrt{2} \times V_{AC(min)}}{3\pi \times V_{BLK}}} \right)^2 R_{DS(on)} \quad (42)$$

$$= \left(\frac{300}{\sqrt{2} \times 85\ V} \times \sqrt{2 - \frac{16 \times \sqrt{2} \times 85\ V}{3\pi \times 400}} \right)^2 0.3\ \Omega = 2.8\ W$$

The switching losses in the MOSFET are estimated by:

$$P_{Q1(SW)} = \frac{1}{2} F_{PFC} \times \left(V_{BLK} \times I_{LINE(RMS(max))} \times (t_r + t_f) + Coss \times V_{BLK}^{\ 2} \right) \quad (43)$$

$$P_{Q1(SW)} = \frac{1}{2} 98\ kHz \times \left(400\ V \times 4.31\ A \times (8\ ns + 7\ ns) + 76\ pF \times 400^2 \right) = 1.86\ W$$

$$P_{Q1} = P_{Q1(COND)} + P_{Q1(SW)} = 2.8\ W + 1.83\ W = 4.63\ W \quad (44)$$

2.3.8 PFC Boost Diode

Reverse recovery losses can be significant in a CCM boost converter, so a silicon carbide diode is chosen here because it has no reverse recovery charge, Q_{RR}, and therefore zero reverse recovery losses. The disadvantage is that the cost is higher than that of Silicon ultra-fast diodes. The losses are estimated as follows:

$$P_{D1} = V_f \times I_{OUT} = 1.6\ V \times 0.825\ A = 1.32\ W \quad (45)$$

2.3.9 Bulk Capacitor

The value of the bulk capacitor is determined by three factors.

1. To ensure loop stability, the capacitance must be between 0.5 μF/ W and 2.4 μF/ W; see "PFC Inductor and Bulk Capacitor Recommendations" of the UCC29950 datasheet (SLUSC18). For this 300-W application, a bulk capacitance in the range 150 to 720 μF is allowed.
2. It must be large enough to provide the required hold-up time.
3. It must be large enough to keep the ripple at twice line frequency within the required limits.

For battery charger applications, the back-up time is not a target design parameter. Hence a value of 220 μF has been chosen for this particular design.

The peak-to-peak ripple voltage at twice line frequency on C_{BLK} is calculated as follows:

$$V_{BLK(RIPPLE)} = \frac{I_{OUT(PFC)}}{\pi \times 2 \times f_{LINE(min)} \times C_{BLK}} = \frac{0.9\,A}{\pi \times 2 \times 47\,Hz \times 220\,\mu F} = 13.85\,V \quad (46)$$

The ripple current flowing in the bulk capacitor depends on the duty cycle, which varies over the line cycle, and also as a function of the RMS value of the line voltage. This makes a precise calculation difficult however the following equation gives a good approximation.

$$I_{C(BLK\_R)} = I_{OUT(PFC)} \times \sqrt{\frac{D}{1-D}} = 0.825\,A \times \sqrt{\frac{0.5}{1-0.5}} = 0.825\,A \quad (47)$$

2.3.10 PFC Stage Current Sense Resistor

The current sense resistor is selected so that:

$$R_{CS(PFC)} = V_{PFCCS(cav\_max)} \times V_{AC(min)} \times \frac{\eta}{\sqrt{2} \times 125\% \times P_{OUT}} \quad (48)$$

$$R_{CS(PFC)} = 225\,mV \times 85\,V \times \frac{0.9}{\sqrt{2} \times 1.25 \times 300} = 33\,m\Omega$$

3 Getting Started Hardware

3.1 Test Conditions

Input conditions: V_{IN}: 85- to 265-V AC. Set the input current limit to 3.5 A.

Output: Variable simulated battery load, 20 to 32 V, 0 to 11 A.

3.2 Equipment Needed

- Isolated AC source
- Single phase power analyzer
- Digital oscilloscope
- Multimeters
- Electronic load to simulate battery

3.3 Procedure

1. Connect input terminals (connector J4) of the reference board to the AC power source.
2. Connect output terminals (connector J1) to electronic load, maintaining correct polarity. Add an additional power supply of 20 V in parallel to the load through a diode such that the anode of the diode is connected to the power supply positive and the cathode of the diode is connected to the positive terminal of connecter J1. The negative of the power supply has to be directly connected to the negative terminal of the connector J1. This external power supply simulates the battery during start up because the PFC and LLC circuit does not turn on, unless the board senses at least 15 V at its output terminals.
3. Set minimum load of about 100 mA and minimum voltage of 20 V.
4. Gradually increase the input voltage from 0 V to turn on voltage of 85-V AC.
5. Turn on the 20 V power supply connected on the load side to the load to apply voltage to the connector J1.
6. Observe that the output voltage across the load terminals has risen to about 30 V.
7. Turn on the load and observe the smooth switching waveforms.

4 Testing and Results

4.1 Efficiency and Regulation

4.1.1 Performance Data of Charger

Table 4. At 230-V AC

V_{INAC}	PF	THD	P_{INAC}	VDC_{BUS}	V_{OUT}	I_{OUT}	P_{OUT}	EFF (%)
230	0.940	22.0	65.0	399.2	29.14	2.0	58.28	89.7
230	0.972	17.0	95.8	399.4	29.13	3.0	87.86	91.7
230	0.983	14.5	126.1	399.8	29.11	4.0	116.73	92.6
230	0.990	13.3	156.7	400.1	29.10	5.0	145.50	92.9
230	0.990	11.0	187.8	400.1	29.09	6.0	174.77	93.1
230	0.990	9.5	218.9	400.1	29.07	7.0	203.96	93.2
230	0.991	8.2	249.9	400.1	29.06	8.0	232.54	93.1
230	0.991	7.0	281.5	400.2	29.05	9.0	261.51	92.9
230	0.991	6.5	313.7	400.2	29.03	10.0	290.71	92.7
230	0.991	4.9	341.5	400.2	29.02	10.9	315.51	92.4
230	0.991	5.8	330.0	400.2	27.98	10.9	303.86	92.1
230	0.990	6.6	319.4	400.2	27.00	10.9	293.22	91.8
230	0.990	6.7	309.3	400.2	26.02	10.9	282.68	91.4
230	0.990	6.9	299.0	400.2	25.01	10.9	271.81	90.9
230	0.990	7.2	288.3	400.2	23.99	10.9	260.58	90.4
230	0.990	7.0	277.8	400.2	23.01	10.9	249.98	90.0
230	0.990	7.4	266.6	400.2	22.00	10.9	238.96	89.6
230	0.990	7.9	255.5	400.2	20.98	10.9	227.93	89.2
230	0.990	8.1	244.9	400.2	20.00	10.9	217.28	88.7

Table 5. At 115-V AC

V_{INAC}	PF	THD	P_{INAC}	VDC_{BUS}	V_{OUT}	I_{OUT}	P_{OUT}	EFF (%)
115	0.970	15.2	66.9	399.0	29.11	2.0	58.34	87.2
115	0.980	12.3	97.4	398.9	29.10	3.0	87.24	89.6
115	0.986	9.1	128.4	399.0	29.09	4.0	116.01	90.4
115	0.989	7.2	160.3	399.0	29.08	5.0	145.34	90.7
115	0.990	6.9	192.2	399.0	29.07	6.0	174.59	90.8
115	0.991	5.3	223.8	389.9	29.06	7.0	203.13	90.8
115	0.991	5.1	256.3	398.7	29.05	8.0	232.11	90.6
115	0.992	4.9	289.3	398.9	29.04	9.0	261.07	90.2
115	0.992	4.4	323.7	398.8	29.02	10.0	290.55	89.8
115	0.992	4.0	352.4	398.8	29.01	10.8	314.64	89.3
115	0.992	4.2	341.2	389.9	27.98	10.9	303.64	89.0
115	0.992	4.4	330.4	389.9	27.02	10.9	293.38	88.8
115	0.991	4.6	319.3	399.0	26.02	10.9	282.58	88.5
115	0.991	4.8	307.9	399.0	25.00	10.9	271.60	88.2
115	0.991	4.9	296.2	399.0	23.99	10.8	260.00	87.8
115	0.991	4.9	285.0	399.0	23.01	10.8	249.38	87.5
115	0.991	5.0	273.4	399.0	22.00	10.8	238.44	87.2
115	0.991	5.2	261.8	399.0	20.99	10.8	227.49	86.9
115	0.991	5.3	250.8	399.0	20.00	10.8	216.76	86.4

4.1.2 Efficiency of Overall System

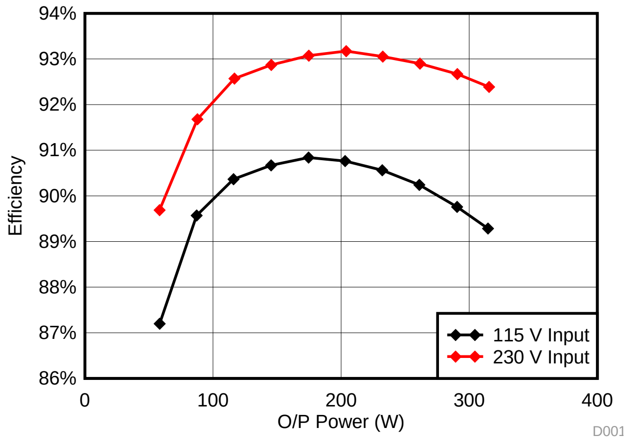

Figure 7. Efficiency versus Output Power in CV Operation

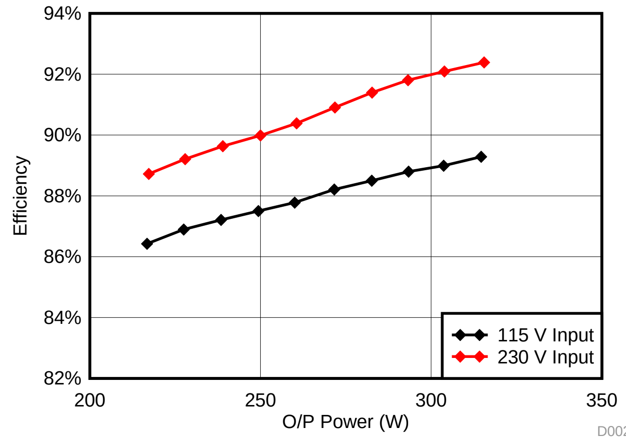

Figure 8. Efficiency versus Output Power in CC Operation

4.1.3 Load Regulation

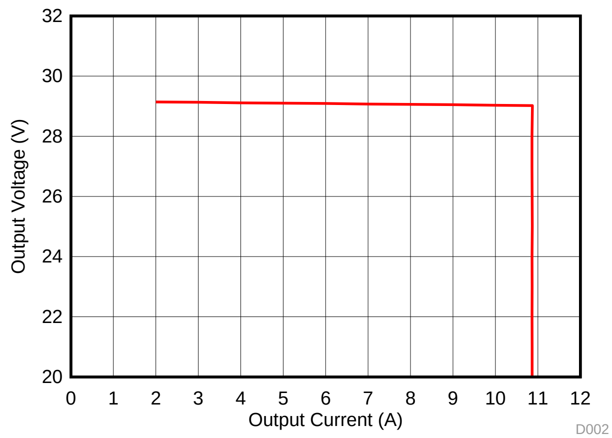

Figure 9. CC-CV Operation

4.1.4 Efficiency of PFC Power Stage

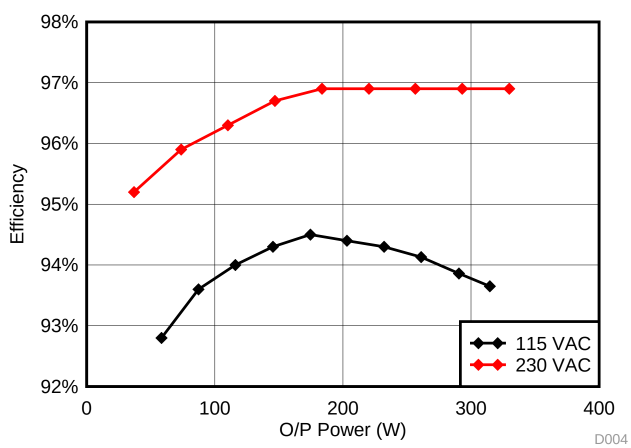

Figure 10. PFC Stage Efficiency

4.1.5 Efficiency of LLC Power Stage in CV Mode

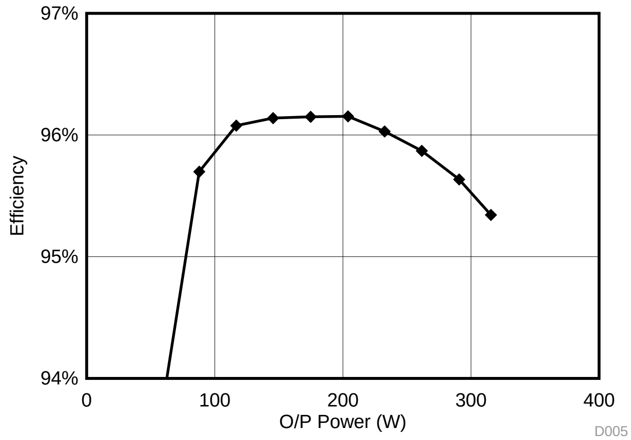

Figure 11. Efficiency of LLC Power Stage in CV Mode

4.1.6 Efficiency of LLC Power Stage in CCM

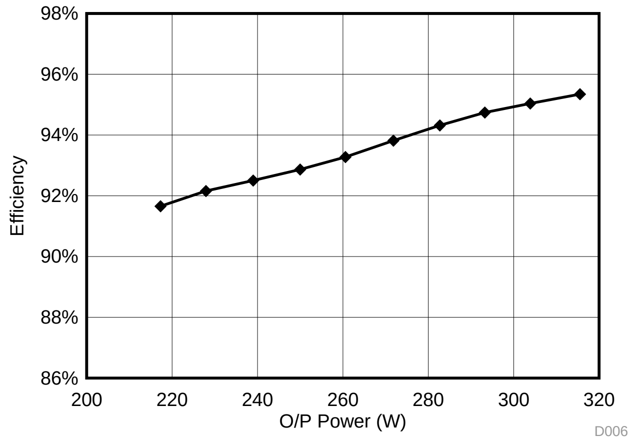

Figure 12. Efficiency of LLC Power Stage in CCM

4.2 Waveforms

4.2.1 PFC Switching Waveforms

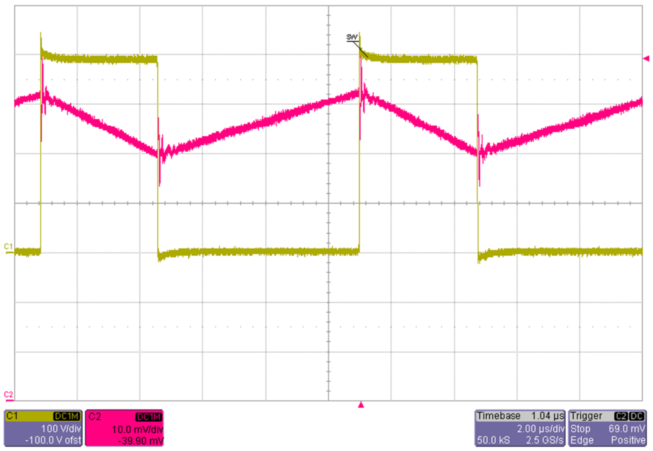

Figure 13. V_{IN} = 115-V AC, Full Load

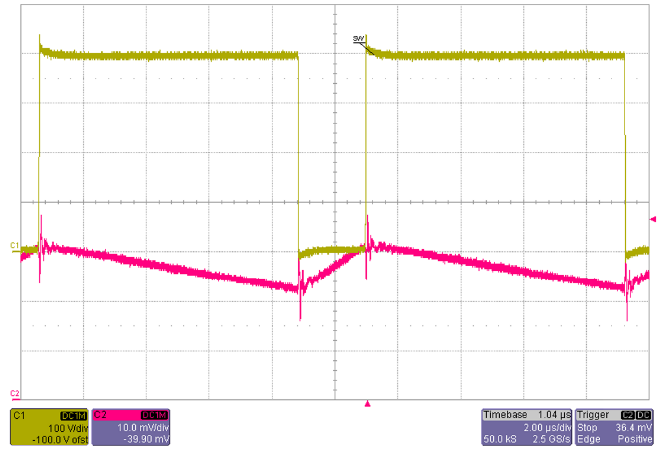

Figure 14. V_{IN} = 230-V AC, Full Load

NOTE: Yellow trace: Drain voltage, 100 V/div; Red trace: Inductor current, 1 A/div (10 mV/A)

4.2.2 LLC Waveforms

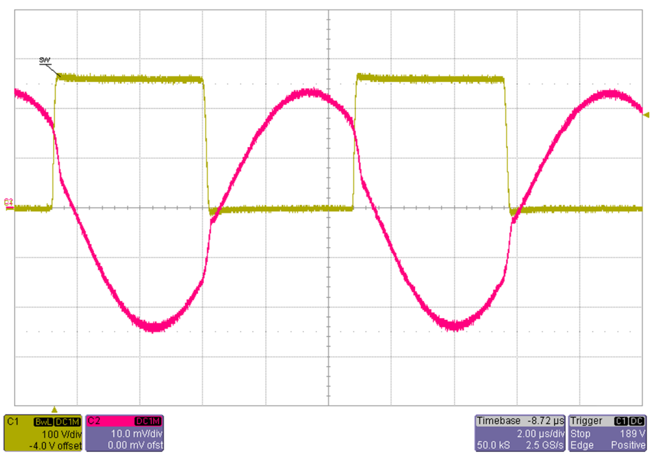

Figure 15. Full Load, CV/CC Transition Point

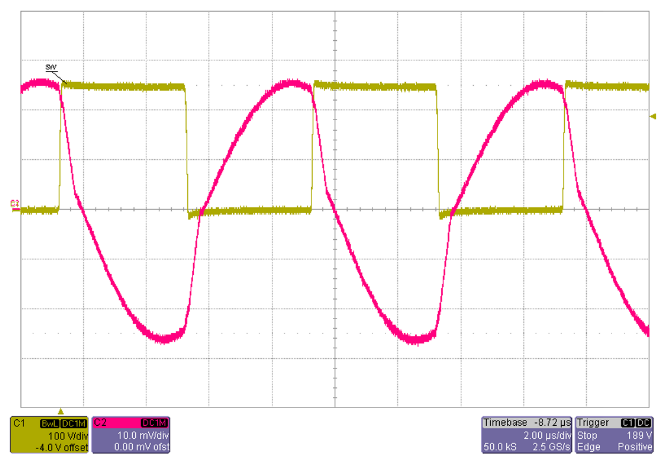

Figure 16. CC Operation, V_O = 24 V

NOTE: Yellow trace: Switch node voltage, 100 V/div; Red trace: Resonant tank current, 1 A/div (10 mV/A)

4.2.3 Output Synchronous Rectifier Stress

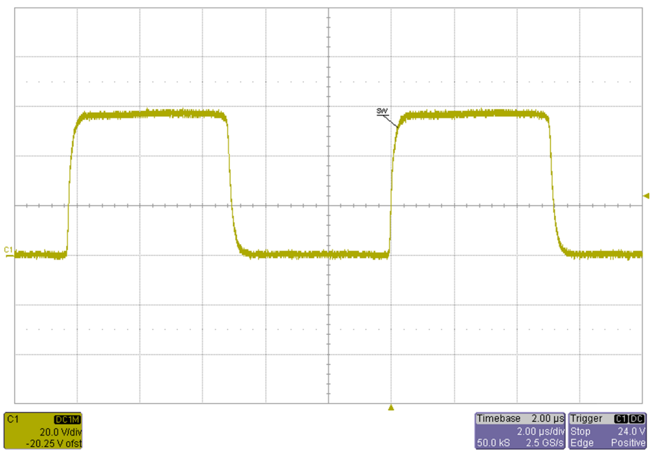

Figure 17. Full Load, CV/CC Transition Point

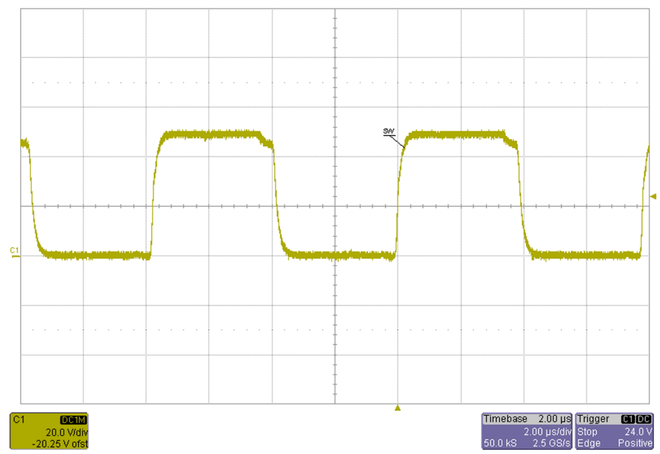

Figure 18. Deep CC Operation, V_O = 20 V

NOTE: Yellow trace: Output synchronous rectifier reverse voltage, 20 V/div

4.2.4 Output Ripple and Noise

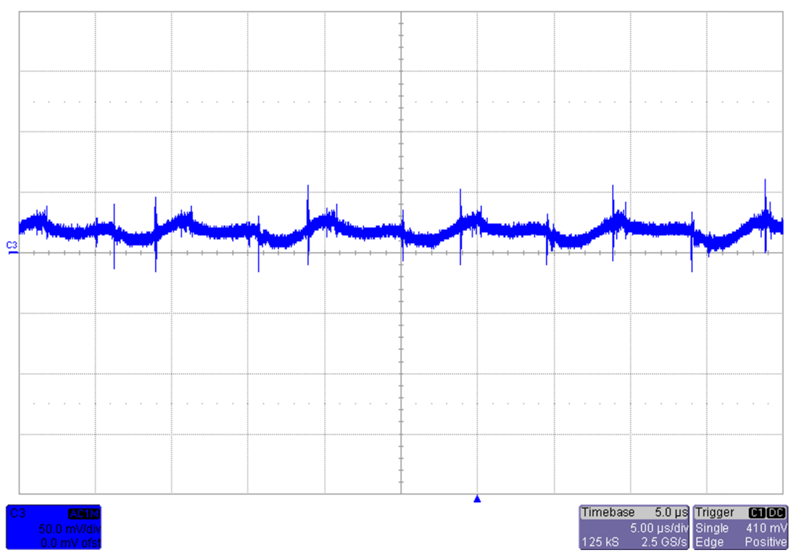

Figure 19. Ripple at Full Load Current (V_O = 29 V)

NOTE: Blue trace: Output voltage ripple and noise, 50 mV/div

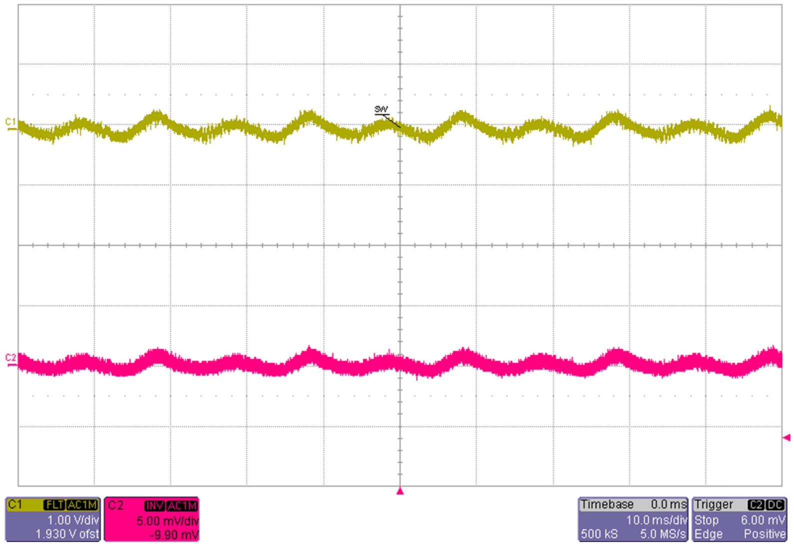

Figure 20. CC Operation, V_O = 29 V

NOTE: Yellow trace: Output voltage ripple and noise, 1 V/div; Red trace: Output current ripple, 0.5 A/div (10 mV/A)

4.2.5 Start-up

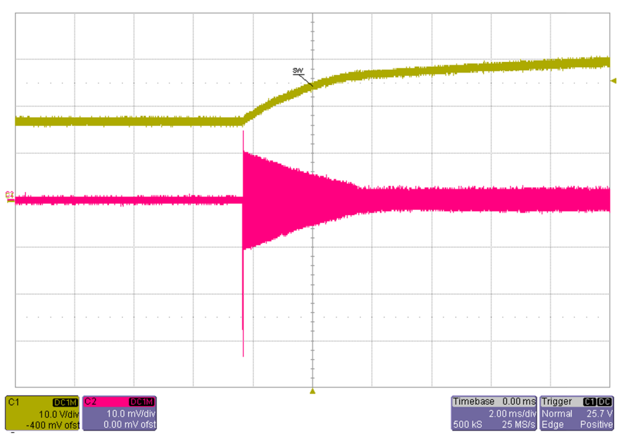

Figure 21. Deep CC Operation, V_O = 20 V

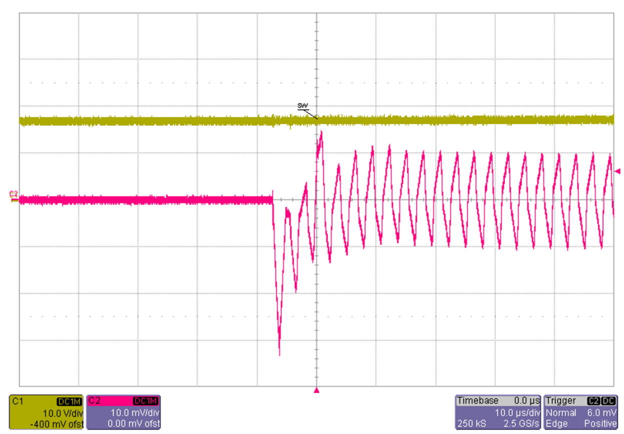

Figure 22. Deep CC Operation, V_O = 20 V (Zoomed in)

NOTE: Yellow trace: Output voltage, 10 V/div; Yellow trace: Input current, 1 A/div (10 mV/A)

NOTE: Yellow trace: Output voltage, 20 V/div; Red trace: Input current, 1 A/div (10 mV/A)

4.2.6 Inrush

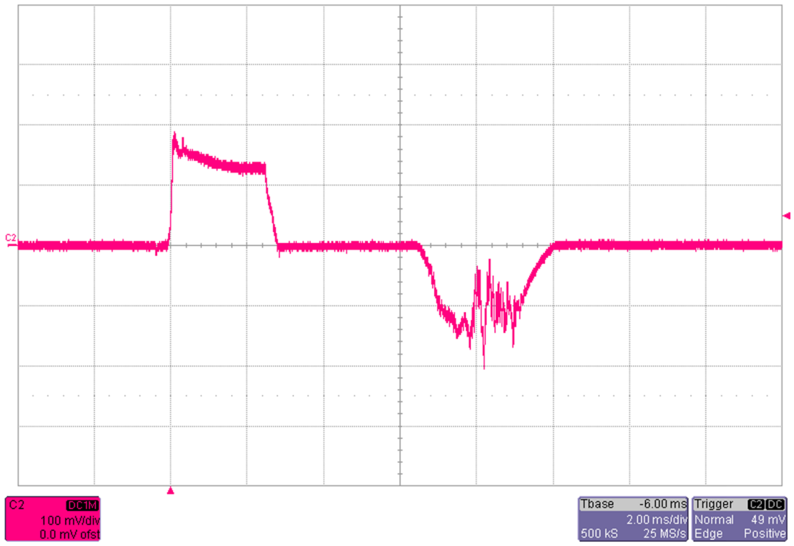

Figure 23. V_{IN} = 230-V AC, Full Load

NOTE: Red trace: Input current, 10 A/div (10 mV/A)

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00704.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00704.

5.3 PCB Layout Recommendations

A careful PCB layout is critical for proper operation of power electronics devices. As with all switching power supplies, attention to detail in the layout can save much time in troubleshooting later on.

5.3.1 Power Stage Specific Guidelines

Key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents, on both the primary and secondary sides of the converter. This helps reduce EMI and improve converter overall performance.
- Keep traces with high dv/dt potential and high di/dt capability away from or shielded from sensitive signal traces.
- Keep power ground and control ground separately for each power supply stage. If they are electrically connected, tie them together at one point near DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, the layout should be symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher currents and become hotter.
- Tie the heat-sinks of all the power switching components to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device. They are intended for protection, and hence need to be routed with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current per IPC2152 as well as acceptable DC and AC impedances. Also, the traces should withstand the fault currents (such as short circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various circuits according to the requirements of applicable standards, such as the UL60950.
- Adapt thermal management to fit the end-equipment requirements.

5.3.2 Controller Specific Guidelines

- The GND pin is the power ground connection and must be used as the return connection for the driver pins PFC_GD, GD1, and GD2.
- The GD1 and GD2 gate drive pins can be used to directly drive the primary winding of a gate-drive transformer or a high-voltage gate driver device. The tracks connected to these pins carry high dv/dt signals.
- The VCC pin must be decoupled to GND and AGND by two 10-µF 1206 ceramic capacitors placed close to the pins. In addition, it is recommended to place an additional 0.1-µF ceramic capacitor 0603 in parallel between the VCC and AGND pin.
- The SUFG is a high-impedance pin and can only be connected to the gate of the external depletion mode MOSFET when the external high-voltage start-up feature is required. If the application does not require the external high-voltage start-up circuit and X-cap discharge function, then the SUFG pin must be left open.
- The SUFS connects to the source of an external depletion mode MOSFET; if this feature in not required, SUFS must be connected to the VCC rail.
- As with all PWM controllers, the effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. Place all decoupling and filter capacitors as close as possible to the device pins with short traces. The AGND pin is used as the return connection for the low-power signaling and sensitive signal traces, AC1, AC2, VBULK, FB, MD_SEL/PS_ON, and AC DET. It is also used as a local decoupling return for PFC_CS and LLC_CS. It is connected to the GND pin at a star point close to the device.
- The VBULK is a high-impedance connection and must be shielded by a ground plane from any high-voltage switching nets. The copper area connecting the VBULK pin to the lower resistor/filter capacitor and the last resistor in the high-side divider chain must be kept to a minimum to reduce parasitic capacitance to any nearby switching nets. The bottom resistor in the divider network and filter capacitor must be placed close to the VBULK pin.
- The AC1 and AC2 are connected to the AC input lines by resistive divider chains. These divider chains are normally formed using several discrete resistors in series. The AC1 and AC2 are high-impedance pins and take care to route the resistor divider components away from high-voltage switching nets. Ideally, the connections must be shielded by ground planes. Give sufficient PCB spacing between the high-voltage connections and any low-voltage nets. A filter capacitor, 470 pF, must be placed in close proximity to the pins on the controller to decouple any high-frequency noise picked up on the AC1 and AC2 sense-chain connections.

5.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-00704.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00704.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00704.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00704.

6 Related Documentation

1. Texas Instruments, *Designing an LLC Resonant Half-Bridge Power Converter*, Power Supply Design Seminar (SLUP263)
2. Texas Instruments, *LLC Design for UCC29950*, Application Note (SLUA733)
3. S. Y. R. Hui and H. Chung, "Resonant and Soft-Switching Converters," In: M. H. Rashid, Ed., Power Electronics Handbook, Academic Press, Cambridge, 2000, pp. 271–304.
4. Texas Instruments, *Feedback Loop Design of an LLC Resonant Power Converter*, Application Report (SLUA582)
5. Texas Instruments, *UCC29950 CCM PFC and LLC Combo Controller*, UCC29950 Datasheet (SLUSC18)

6.1 Trademarks

7 About the Authors

KRISHNA DORA is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the Power Delivery, Industrial Segment. Krishna brings to this role his extensive experience in high-power converters (Solar and UPS). Krishna earned a B.E degree from Andhra University, India in 2001, and M.Tech degree from IIT Bombay, Mumbai in 2004, both in electrical engineering. He has two US patents in his name.

LATIF AMEER BABU is a systems architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Latif brings to this role his extensive experience in power electronics, high-frequency DC-DC converters, and analog circuit designs. Latif earned his master of technology in power electronics and power systems from Indian Institute of Technology, Mumbai; IN. Latif is a member of the Institute of Electrical and Electronics Engineers (IEEE) and has one US patent.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to A Revision	Page
• Changed from preview draft	1

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265