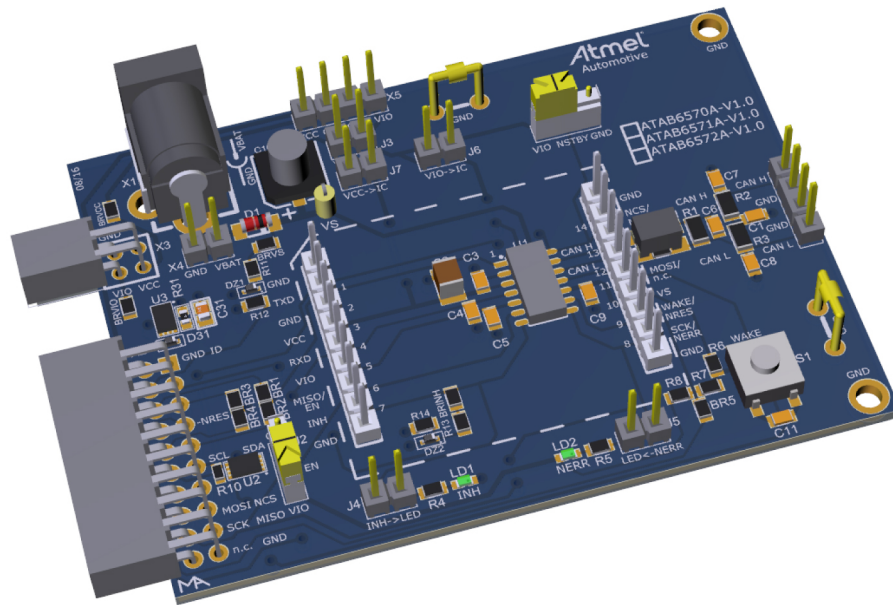# ATAB657XA Development Board User's Guide

Introduction

The development board ATAB657XA is a hardware platform to evaluate the new ATA657X CAN device family and it enables users to rapidly prototype and test new CAN designs with the ATA657X ICs.

The ATA657X device family includes three high-speed controller area network (CAN) transceivers, which interface a CAN protocol controller and the physical two-wire CAN bus designed for high-speed CAN applications (up to 5 Mbit/s) in the automotive environment. Two of them also support partial networking. All offer improved electromagnetic compatibility (EMC) and electrostatic discharge (ESD) performance and very low-power consumption in Standby and Sleep modes:

- Besides local wake-up via WAKE and remote wake-up pattern in accordance with ISO 11898-5, the ATA6570 is fully compliant to the ISO 11898-6 supporting CAN partial networking. The ATA6570 additionally supports a CAN-FD device and can be easily configured via the SPI as Non-FD (meaning classical CAN 2.0), CAN FD silent, CAN FD passive or as CAN FD active device, in order to fulfill the corresponding application requirements. The VIO pin allows the automatic adjustment of the I/O levels to the I/O level of the connected microcontroller.

- The **ATA6571** has ideal passive behavior to the CAN bus when the supply voltage is off. Microcontrollers with supply voltages from 3V to 5V can be directly interfaced via the VIO pin. Its advanced low-power management with local and remote wake-up support makes it possible to achieve very low current consumption in Standby and Sleep mode, even when the internal VIO and VCC supplies are switched off. Diagnostic and protection functions, including bus line short-circuit detection and battery connection detection, are also part of the ATA6571's features.

- The **ATA6572** is a CAN Partial Networking transceiver and is very similar to the ATA6570. The only difference is that instead of the WAKE pin, it has a dedicated reset pin indicating a watchdog failure or an undervoltage event.

Various operating modes together with the dedicated fail-safe features make the ATA657X an excellent choice for all types of high-speed CAN networks, especially in nodes requiring low-power mode with local wake-up capability or via the CAN bus. With the INH output they have the capability to power down the complete CAN node.

The ATA657X devices are available in a SOIC14 package as well as in a VDFN14 package, for space-saving application. The development board ATAB657XA supports only SOIC14 packages. However, an adaptor board can be plugged in using the adaptor board-header, if a device in a VDFN package is used (the adaptor board is within the not scope of supply and services of this demo kit/board).

Figure 1. SOIC14 Pinning
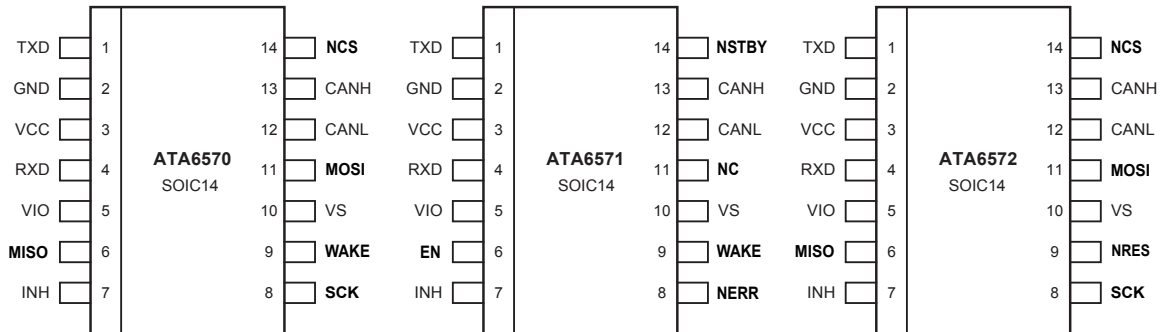
Development Board Features

The development board for the ATA657X ICs supports the following features:

- All components necessary to put the ATA6570, ATA6571 or ATA6572 into operation are included
- Placeholders for some optional components for extended functions
- All pins are easily accessible
- Switching into Normal, Standby or Sleep mode via two jumpers (ATA6571)
- Push button included for creating a local wake-up after entering Sleep mode
- LEDs for operation indication
- Ground coulter clip for easy probe connection while measuring with oscilloscope
- Connectors for direct plug-in with the C21-XPRO Xplained board (only ATA6570 and ATA6572 with SPI)

WHAT DOES THE ATAB657XA DEVELOPMENT BOARD KIT CONTAIN?

This ATAB657XA Development Board kit includes:
- ATAB657XA Development Board (ADM00870)
- Important Information Sheet

Table of Contents

1.   Hardware Description

The development board for the ATA657X is shipped with all components necessary to start developing a CAN node immediately. However, commands, data and status information are transferred to and from the ATA6570 and ATA6572 via SPI. This is how the ATA6570 and the ATA6572 can be configured and operated.

Microchip offers an Xplained Pro board (ATSAMC21-XPRO Xplained board), which can be used to interface with the ATA657X GUI to operate and control the ATA6570 and ATA6572. This Xplained Pro board must be ordered separately, as the ATAB657XA board comes as a stand-alone board. The ATA657X GUI can be downloaded directly from Microchip's web site: http://www.microchip.com/.

Figure 1-1. ATAB657XB Evaluation Board Overview
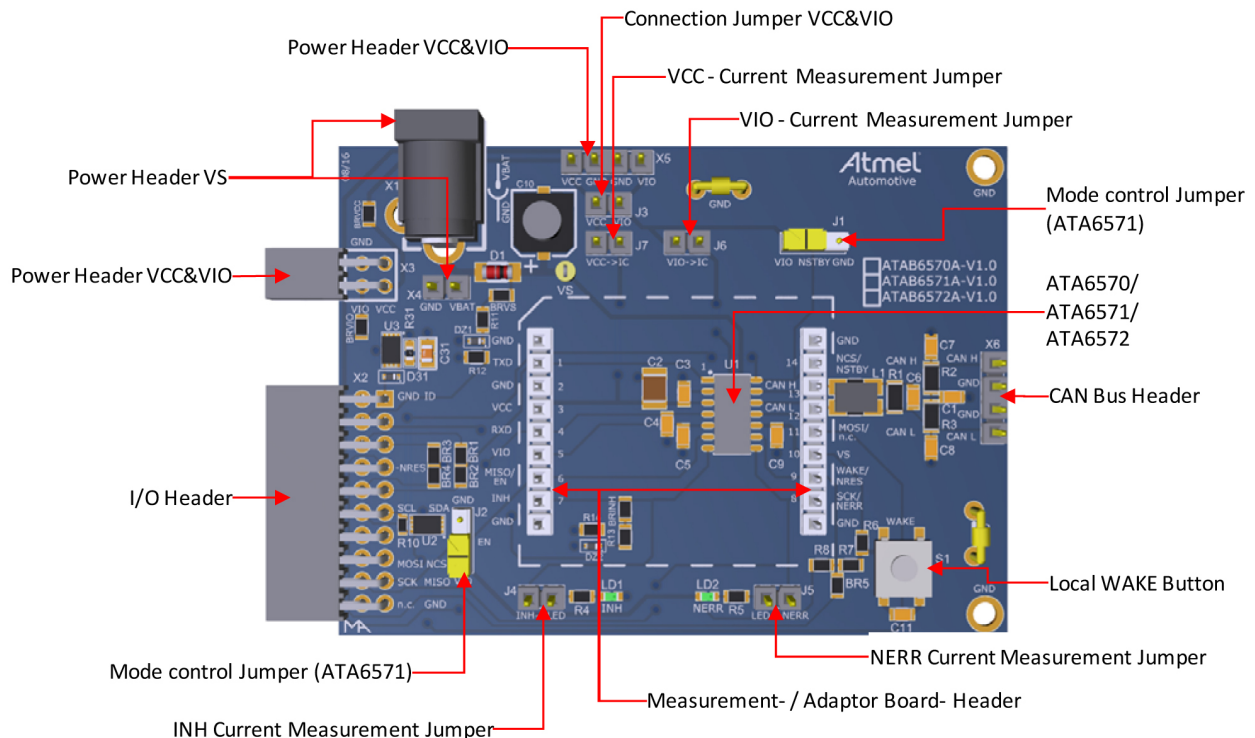
After correctly connecting an external 12V DC power supply (Power Header VS) to the power connector of the ATAB657X A board and connecting the Xplained Pro interface board to the PC via the USB cable, the kit is ready to use. To start working with the kit, execute the `ATA6570/72.exe.`

The ATA6570/72 IC starts in Standby mode, INH is active (if jumper J4 is set the LED LD1 is ON) and the window watchdog is switched off at the ATA6570 and switched on at the ATA6572. A quick check to determine if everything is working properly can be done by executing the following:

CAN Communication Check:

- Click the **Normal Mode** button in the **Operating mode** section
- Click the **Normal Mode** button in the **CAN transceiver** section
- Set "TXD Pulsed"
- Choose 250 kHz as "Frequency" and press the **Set** button. A 250 kHz signal should be visible on the CANH and CANL pins, when you put oscilloscope probes on those pins.

Sleep/Wake-up Check:

- Select **Falling edge** or **Rising edge** in the **Wake-up settings** section
- Click the **Sleep Mode** button in the **Operating mode** section. Please keep in mind that at least one wake-up source should be selected prior putting the ATA657X device into Sleep mode (to avoid dead lock). Otherwise the go to sleep command will be ignored and the device will switch to Standby mode.
- The INH will be switched off and if the jumper J4 is set the LED "LD1" will be switched off
- Press the local wake-up button (ATAB657X board) -> the LED LD1 will be switched on (the ATA657X device switches from Sleep to Standby mode and the INH becomes active)

Watchdog Check:
- Press the **STBY Mode** button in the **Operating mode** section
- Select "Window mode"
- The LED LD1 should be flashing – Watchdog resets at INH, because the watchdog is not triggered
- Set 100 ms for the "Trigger period" in the **Watchdog** section
- Set "Trigger On"
- The LED LD1 should be permanently on – Watchdog is working properly and no resets are generated at the INH pin

1.1   Power Supply

The ATAB657XA board can be powered by an external power source (4.5V to 28V) through the X1 connector or the 2-pin power header X4.

Additionally, a 5V external power source should be connected to the X5 connector (VCC) and the power source (2.8V to 5.5V) used to supply the used microcontroller should be connected to the X5 connector (VIO), when working in stand-alone mode. When the ATAB657XA board is connected to a C21-XPRO Xplained Pro board, VIO and VCC will be delivered from the Xplained Pro board through the X3 power header. However if it is necessary to have an external VIO and/or VCC power supply while an Xplained Pro board is connected to the ATAB657XA board, the trace at BR5 and BR6 should be cut. This cut-connection can be at any time restored by soldering a 0Ω resistance on the BR5 and/or BR6 footprint.

1.1.1   Measuring the ATA657X Current Consumption

As part of an evaluation of the ATA657X device it can be of interest to measure its current consumption. Because the device has different power supplies (VBAT, VCC and VIO) it is possible to measure the current consumption via separate jumpers. By replacing the jumper J6 by an ampere-meter it is possible to determine the current consumption at VIO and by replacing the jumper J7 it is possible to measure the current consumption at VCC.

1.2   Headers, Connectors and Jumpers

The following table describes the implementation of the relevant connectors, headers and jumpers on the ATAB657XA evaluation board.

Table 1-1. Headers, Connectors and Jumpers

Type	Name	Description
Switch Jumper	J1	NSTBY-pin mode control jumper. The NSTBY pin together with the EN pin controls the operating mode of the device. Available only on the ATAB6571A board.
Switch Jumper	J2	EN-pin mode control jumper. The EN pin together with the NSTBY pin controls the operating mode of the device. Available only on the ATAB6571A board.
Jumper	J3	VIO to VCC jumper. If the VIO voltage is same as VCC (5V) this jumper can be set and only one supply can be applied at header X5. If VIO is different than VCC this jumper should be removed.
Jumper	J4	When replacing the jumper J4 by an amperemeter it is possible to determine the current consumption at INH, or connect an external circuitry. When measuring the allover current consumption of the device this jumper should be removed in order to disconnect the LD1 LED from the INH pin.
Jumper	J5	When replacing the jumper J5 by an amperemeter it is possible to determine the current consumption at NERR. Or connect an external circuitry. Or when measuring the all-over current consumption of the device this jumper should be removed in order to disconnect the LD2 LED from the NERR pin. Available only on the ATAB6571A board
Jumper	J6	When replacing the jumper J6 by an amperemeter it is possible to determine the current consumption at VIO.
Jumper	J7	When replacing the jumper J7 by an amperemeter it is possible to determine the current consumption at VCC.
Connector	X1	Main power supply connector – VBAT
Header	X2	Interface header to C21-XPRO Xplained board
Header	X3	External supply power header – GND, VIO and VCC supplied from C21-XPRO Xplained board.
Header	X4	Optional main power supply connector – VBAT
Header	X5	VCC and VIO power supply header
Header	X6	CAN bus connection header

1.3   Mechanical Buttons

There is one mechanical button on the ATAB657XA board. It is only mounted at the ATAB6570A and ATAB6571A boards and is used to generate a local wake-up. At the ATAB6572A variant this button is not assembled.

1.4   LEDs

There are two LEDs available on the ATAB657XA board (LD1 and LD2) indicating activity on INH pin and NERR pin respectively. Via the jumpers J4 and J5, the LEDs can be deactivated if necessary (for example for current measurements, or if an external circuitry should be connected to the INH pin or to NERR pin).

2.   Crypto Authentication Device

On the ATAB657XA board two crypto authentication devices are mounted. The ATSHA204 contains information that identifies the extension with its name and some extra data. When an ATAB657XA board is connected through an interface Xplained Pro board to a PC, the information is read and sent to the GUI. The table below shows the data fields stored in the ID chip with example content.

Table 2-1. ID Chip Content

Data Field	Name	Example Content
Manufacturer	ASCII string	Atmel'\0'
Product Name	ASCII string	ATAB657xA'\0'
Product Revision	ASCII string	01'\0'
Product Serial Number	ASCII string	1774020200000010'\0'
Minimum Voltage [mV]	uint16_t	3300
Maximum Voltage [mV]	uint16_t	5500
Maximum Current [mA]	uint16_t	50

The second crypto authentication device is the Microchip ATECC508A. It integrates ECDH (Elliptic Curve Diffie-Hellman) security protocol — an ultra-secure method to provide key agreement for encryption/decryption, along with ECDSA (Elliptic Curve Digital Signature Algorithm) sign-verify authentication.

Similar to all Microchip CryptoAuthentication products, ATECC508A employs ultra-secure hardware-based cryptographic key storage and cryptographic countermeasures that are more secure than software-based key storage.

The device is compatible with any microprocessor (MPU) or microcontroller (MCU) including Microchip and Microchip AVR MCUs or MPUs. As with all CryptoAuthentication devices, the ATECCC508A delivers extremely low power consumption, requires only a single GPIO over a wide voltage range and has a tiny form factor making it ideal for a variety of applications that require longer battery life and flexible form factors.

The ATECC508A can be used together with the ATA657X can transceiver in order to provide secured CAN communication. For more information about the ATECC508A crypto authentication device and how it can be configured please visit our web site: http://www.microchip.com/wwwproducts/en/ATECC508A.

3.   Mode Control

The ATA657X devices offer various operation modes.

The desired operating mode of the ATA6570 and the ATA6572 devices can be set via the SPI interface. With the dedicated GUI and the connected Xplained Pro interface board (C21-XPRO) configuring the ATA6570 and the ATA6572 devices can be easily done (for more information please see section Graphical User Interface (GUI)).

The ATA6571 can be set into its different operating modes via the switch jumpers J1 and J2, which are connected with the NSTBY pin respectively the EN pin. The following table shows the switch jumper setting and the corresponding selected mode.

Table 3-1. Mode Control Jumper Settings

Mode	J1 (NSTBY) Position	J2 (EN) Position
Sleep Mode	In the middle	In the middle
Standby Mode	Left (VIO)	In the middle
Standby Mode	Right (GND)	In the middle
Standby Mode	Right (GND)	Up (GND)
Sleep Mode	Right (GND)	In the middle
Silent Mode	Left (VIO)	Up (GND)
Normal	Left (VIO)	Down (VIO)

Figure 3-1. ATAB6571A Evaluation Board Mode Change Jumpers
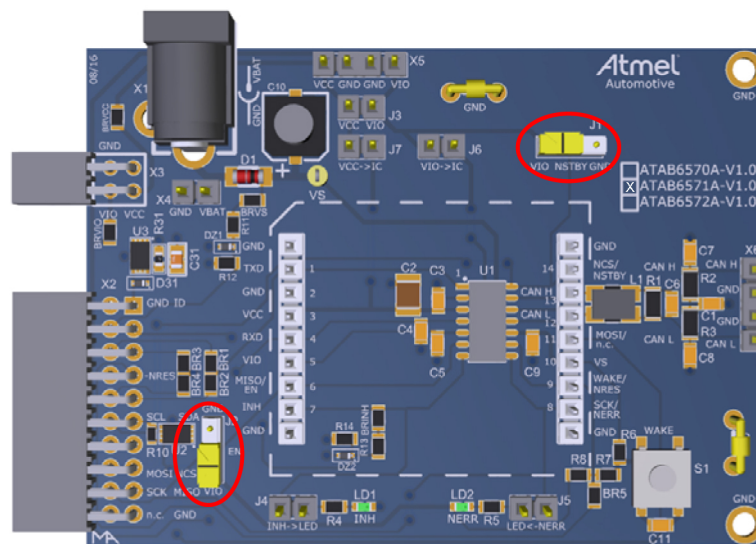
Normal Mode

A high level on the NSTBY pin and a high level on the EN pin selects Normal mode. In this mode, the transceiver is able to transmit and receive data via the CANH and CANL bus lines. The output driver stage is active and drives data from the TXD input to the CAN bus. The differential receiver converts the

analog data on the bus lines into digital data that is output to pin RXD. The bus biasing is set to VCC/2 and the undervoltage monitoring of VCC is active. Also the INH output is switched on.

The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible electromagnetic emission (EME).

To switch the device in normal operating mode, set the NSTBY pin to high (jumper J1 set to the left side) and the EN pin to high (jumper J2 set to lower position).

The STBY and the EN pins each provide a pull-down current to GND, thus ensuring defined levels if the pins are open.

Silent Mode

A high level on the NSTBY pin and a low level on the EN pin selects Silent mode. This receive-only mode can be used to test the connection of the bus medium. In Silent mode, the ATA6571 can still receive data from the bus, but the transmitter is disabled and therefore no data can be sent to the CAN bus. The bus pins are released to recessive state (VCC/2) and the INH output remains active. All other IC functions, including the receiver, continue to operate as they do in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

Standby Mode

A low level on the NSTBY pin selects Standby mode. In this mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and the Normal-mode receiver are switched off to reduce current consumption and only a low power differential receiver monitors the bus line for a valid wake-up signal. If a dominant state longer than t_{wake} is received, the RXD switches to low to signal a wake-up request.

In Standby mode, the bus lines are biased to ground to reduce current consumption to a minimum. The low-power differential receiver monitors the bus lines for a valid wake-up signal. When the RXD pin switches to low to signal a wake-up request, a transition to Normal mode is not triggered until the STBY pin is forced back to low by the microcontroller.

In the event the NSIL input pin is set to low in Standby mode, the internal pull-up resistor causes an additional quiescent current from VIO to GND. Microchip therefore recommends setting the NSIL to high in Standby mode.

Sleep Mode

In Sleep Mode the current into the VS pin is reduced to a minimum. The behavior of the transceiver is the same as in Standby mode, but the INH output is switched off.

4. Graphical User Interface (GUI)

Figure 4-1. ATA6570/72 Graphical User Interface
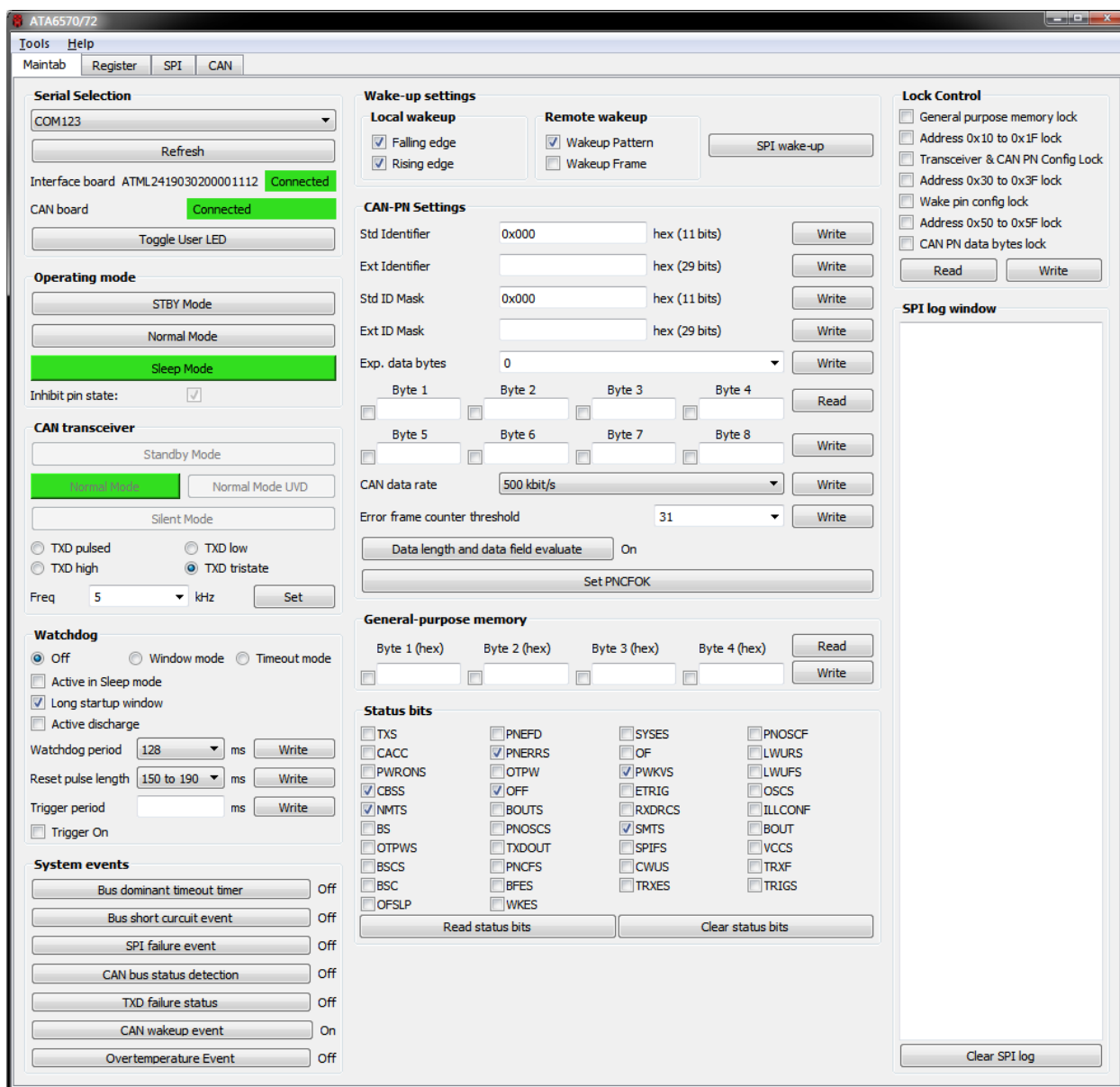
Note: The root directory of the GUI contains installers for the Visual C# runtime from Microsoft and for the Microchip USB drivers. Both are necessary to run the GUI and must be run before the GUI is launched. `vc_redist.x86.exe` should be installed for x86/x64 based systems. For the USB driver the correct installer should be chosen depending on the host computer.

4.1 Features

- Configuration of functions
  - Operating mode
  - CAN Transceiver mode

- – Watchdog
- – System events
- – Wake-up settings
- – CAN-PN settings
- – General-purpose memory
- – Status bits
- – Lock Control
- Direct read/write to all registers
- Configuration for Xplained Pro
  - – Watchdog trigger
  - – CAN TXD pin static/pulsed/data
- SPI commands

The ATA657X GUI is a PC software application that graphically displays configuration of an ATA657X device received through the PC's USB connection. The received data is shown in different tabs.

4.2 Maintab

This tab gives access to most of the functionality from a feature perspective. The device can be configured without accessing the registers directly. Register accesses (read and write) will happen in the background and will be printed to the SPI log window.

This tab is not refreshed periodically. Instead, relevant parts are refreshed when performing an action. For example, when configuring the operating mode, the mode is read back and updated accordingly. There are two ways to refresh the complete tab:

- Switch from a different tab
- Select a different SAMC21 Xplained Pro board in the **Serial Selection** section and press **Refresh**

Both methods will refresh the entire **Maintab**.

4.2.1 Serial Selection

The GUI supports connecting to multiple SAMC21 Xplained Pro boards, hence it is necessary to select which one to send the command to. In the drop-down menu, all boards with a suitable firmware are shown. Commands are sent to the currently selected one. The board can be identified by the Serial number that is also shown in this window. This serial number is printed on a sticker on the bottom of the PCB. To help identifying the board the LED0 close to the SW0 can be toggled by the GUI.

4.2.2 Operating Mode

The operating mode of the device can be chosen in this section. Available are Standby, Normal and Sleep modes, as described in the data sheet. Additionally, the state of the INH pin is continuously monitored and shown in a check box. The switch to Normal and Standby mode can always be executed by issuing the corresponding write to the DCMR register. To enter Sleep mode, certain conditions must be fulfilled, which are described in the data sheet. The GUI checks for these conditions and if they are not fulfilled logs an error in the SPI log window. The mode will remain as before. A write attempt to DCMR will not happen.

4.2.3 CAN Transceiver

In this section the transceiver part can be configured. For the CAN Transceiver the following modes are accessible

- Standby mode
- Normal mode
- Normal mode with undervoltage detection active
- Silent mode

Note: To use the transceiver the device operating mode has to be Normal mode. This mode can be changed as described in Operating Mode

In this section it is also possible to control an output of the SAMC21 connected to the TXD input. Available options are

- TXD pulsed - this will pulse the TXD with a 50% duty cycle
- TXD static low
- TXD static high
- TXD tristate - in this case the internal pull-up on the ATA657X will pull the pin high

When the pulse option is selected, the nearest possible value for the frequency will be selected and the Freq. cell will be updated accordingly.

4.2.4   Watchdog

In this section, the watchdog can be configured. Available modes are:

- "Off"
- "Window mode"
- "Time-Out mode"

Additionally, all the configuration bits for the watchdog can be controlled.

The following bits can be set/cleared:

- "Active in Sleep mode" - sets/clears the WDSLP bit in WDCR1 register
- "Long startup window" - sets/clears the WDLW bit in the WDCR1 register
- "Active Discharge" - sets/clears the ADCH bit in the WDCR1 register

"Watchdog period" and "Reset pulse length" control the settings in WDCR1 and WDCR2.

Note: In order to avoid unwanted configuration of the window watchdog (WWD), the ATA6570 only allows users to configure the WWD (write access to WDCR1 register and WDCR2) when the device is in Standby mode. For more information, please see the data sheet.

An appropriate trigger setup should be made that configures the SAMC21 Xplained Pro to generate an SPI trigger command with the configured frequency. Activating the trigger will first update the frequency on the SAMC21 Xplained Pro and then activate the continuous triggering.

4.2.5   System Events

This section allows the user to enable/disable the capturing of all events distributed across the different registers. The current status is indicated next to the button that toggles the status. The following bits can be configured:

- BOUTE - **Bus dominant time-out timer**
- BSCE - **Bus short circuit event**
- SPIFE - **SPI failure event**
- BSE - **CAN bus status detection**
- TRXFE - **TXD failure status**

- • CWUE - **CAN wake-up event**
- • OTPWE - **Overtemperature event**

The displayed status is not a live-view and only updates when the corresponding button is pressed or the complete tab is updated as described in Section Maintab.

4.2.6 Wake-up Settings

In this section, all wake-up sources supported by the ATA657X device can be activated. For the Local wake-up on pin Wake, falling, rising or both edges can be configured as a valid wake-up source. For the Remote wake-up, either wake-up pattern, wake-up frame or none have to be configured. If "Wake-Up Frame" is selected, the frame must be configured as described in section CAN PN Settings The **SPI wake-up** button will wake up the device by setting the device into Standby mode. The four check boxes are updated when a full refresh on the **Maintab** tab is performed.

4.2.7 CAN PN Settings

This section allows the user to configure the CAN-PN functionality available in the ATA657X. The wake-up frame can be configured with either a STD identifier or an extended one, and, if necessary, a data byte mask can be activated, as well.

Note: It should be noted that the data bytes are a mask of bits expected to be 1, i.e., a data byte of 0xAA on the bus will generate a wake-up for devices configured for 0x01, 0x0A and 0xAA and others where all bits selected in the mask are fulfilled.

Note: It should be noted that the configuration for the CAN PN only becomes valid and active after the PNCFOK flag has been set. This can be done by pressing the "Set PNCFOK" button in this section.

4.2.8 General Purpose Memory

This section gives access to the 4 bytes of general purpose memory available on the ATA657X (available at addresses 0x6-0x9). The bytes read/written are selected with the check boxes. The displayed values are not a live-view but only update when the corresponding button is pressed or the complete tab is updated as described in section Maintab.

4.2.9 Status bits

This section gives an overview of all status bits of the device. The display is not updated continuously but must be refreshed manually by clicking the **Read Status bits** button.

Bits can not be manipulated individually but it is possible to clear all status-bits that are writable at once. The following bits are cleared when clicking the **Clear status bits** button:

- • "BOUTS" - Bus dominant timeout status
- • "BS" - Bus silence
- • "BSCS" - Bus short circuit
- • "CACC" - Corrupted write access to watchdog configuration registers
- • "CWUS" - CAN wake-up status
- • "ETRIG" - Early watchdog trigger
- • "ILLCONF" - Watchdog configuration was written while the device is not in Standby mode
- • "LWUFS" - Local wake-up falling edge detected
- • "LWURS" - Local wake-up rising edge detected
- • "OF" - Watchdog overflow
- • "OFSLP" - Watchdog overflow in Sleep mode

- • "OTPW" - Over-temperature pre-warning
- • "PNEFD" - Partial networking frame detection status
- • "PWRONS" - Power-on Rteset
- • "SPIFS" - SPI failure status
- • "TRXF" - Transceiver failure

A list of all status-bits and their descriptions can be found in the data sheet https://www.microchip.com/wwwproducts/en/ATA6570.

4.2.10 Lock Control

In this section, it is possible to control the bits locking specific parts of the device memories. All seven lock bits can be configured. The configuration is only written/read when pressing the write/read button. Ticking the check boxes will not update the value on the ATA657X. The displayed status is not a live-view but only updates when the corresponding button is pressed or the complete tab is updated as described in section Maintab.

4.2.11 SPI Log Window

In this section, all SPI communication with the ATA657X will be logged and possible errors are displayed. The log can be cleared by pressing the **Clear SPI** log button below it. The log entry will be made as soon as an action in the GUI is performed. If the command was accepted by the ATA657X, it is not actually checked. As more data is written in the log file, the GUI navigation speed might be affected. In such cases, try clearing the log.

4.3 Registers

This tab allows the user to manipulate the registers directly. Each column shows the name of the register, the address, the last read value and gives the option to read from the register or write to it.

Figure 4-2. Registers

It is also possible to read all registers at once. When writing registers, it is possible to automatically verify the value afterward. This is selectable with the check box "Verify after write". Until a value is verified, it will be shown in a red font.

Note: The displayed values are not a live-view but only updates when the corresponding button is pressed or the complete tab is updated by a tab-switch.

4.4 SPI

This tab allows to send SPI commands to the ATA657X device directly. This can be useful for writing multiple registers at the same time or for debugging purposes. To read an address, a valid hex value must be entered in the Address (hex) field.

Figure 4-3. SPI
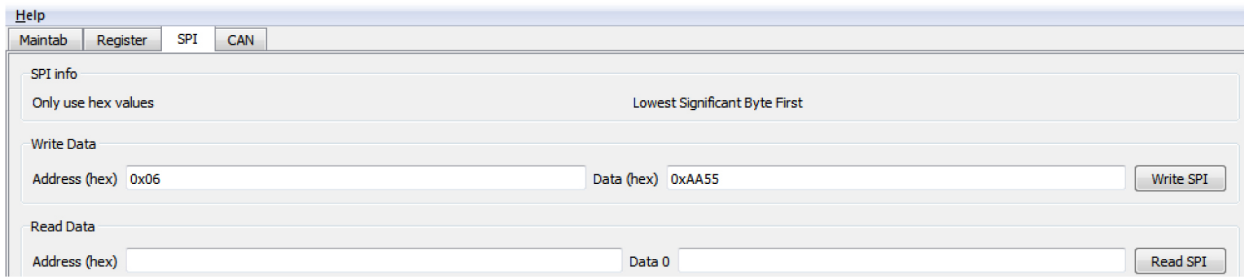
Note: The data is sent out starting from the lowest significant byte. The order in which the bytes are sent is from right to left. Writing address 0x06 and data 0xAA55 will write 0x55 to 0x06 and 0xAA to 0x07.

4.5 CAN

This tab allows some very limited sending of CAN messages for testing. Only "singleshot" messages are supported.

Figure 4-4. CAN
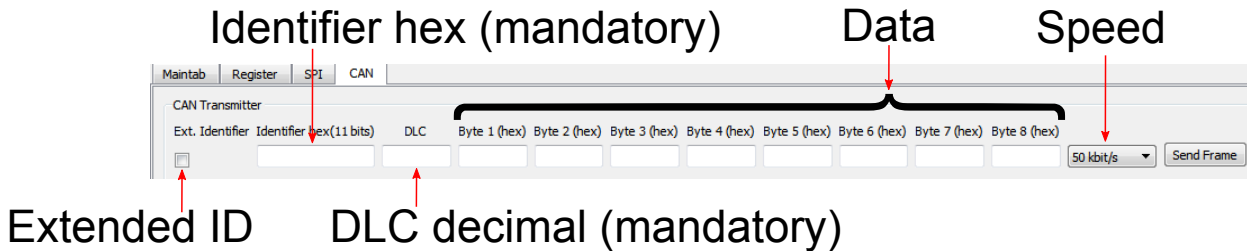
To initiate a transmission the identifier, the DLC and at least the number of bytes specified in the DLC must be given. After clicking send frame, the frame will be sent one time if the configuration is valid. It is not possible to receive CAN data.

5. Test Setups and Measurements

5.1 Various Measurements

The required components on the basic application board can be found below. A two- or better four-channel oscilloscope is sufficient to measure the timing characteristics of the ATA657X. The transmit data signal TXD can be generated by any signal generator that is capable of delivering a rectangular or pulse signal with 3.3V to 5V amplitude, referenced to ground or directly from the GUI. The temporal relation of TXD, RXD and the CANH, CANL signals, for example, can be examined.

Figure 5-1. Test Circuit
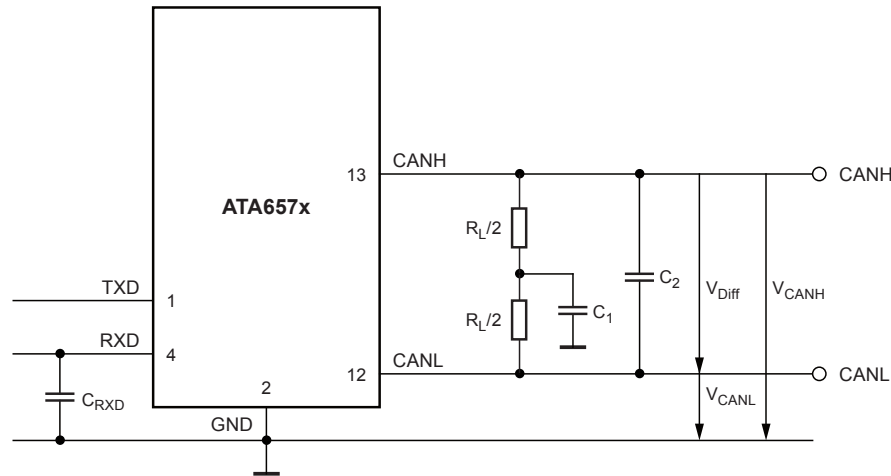
The footprint for an optional common mode choke (L_1) is implemented on the ATAB657XA board. This common mode choke (L_1) is per default replaced by two 0Ω resistors.

Instead of a one-resistor termination, it is highly recommended to use split termination, which is per default assembled. EMC measurements have shown that split termination is able to significantly improve the signal symmetry between CANH and CANL, thus reducing emissions. Basically, the termination is split into two resistors of equal value (per default mounted: $R_2 = R_3 = 62Ω$) and a capacitor (C_1) to GND at the center tap, which represents one of the two usual bus end terminations. The special characteristic of this approach is that the common-mode signal, available at the center tap of the two resistors, is terminated to ground via the capacitor C_1. The recommended value for this capacitor C_1 is in the range of 4.7 nF to 47 nF (4.7 nF mounted per default). As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors R_1 and R_2 should be as low as possible (< 1% is desirable).

Timing Measurements

Additionally placeholders are implemented on the board for timing measurements (R_1, C_6 and C_4).

Figure 5-2. Components to be Removed (Red) or Replaced (Green) for the Timing Measurement Setup
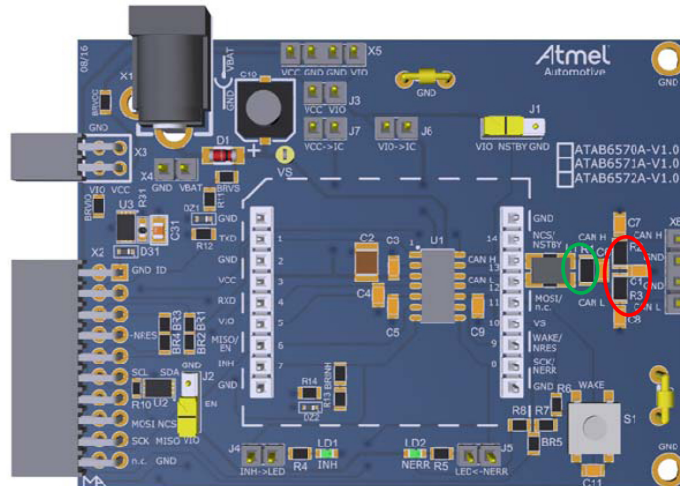
If a function generator is connected to the TXD header, it can be adjusted to output a rectangular signal up to a frequency corresponding to the maximum data rate of the final application. Please ensure that its output signal levels are in the appropriate range, particularly that no negative voltage occurs. Of course, the function generator can be replaced by a dedicated data generator in order to form a better approach to the desired application or use the Xplained Pro board. The high-impedance inputs of the oscilloscope can be connected directly; however, it is advantageous to use probes, so that the signals are not noticeably affected by the capacitance of the coaxial cable.

Figure 5-3. Communication Signals of the ATA657X
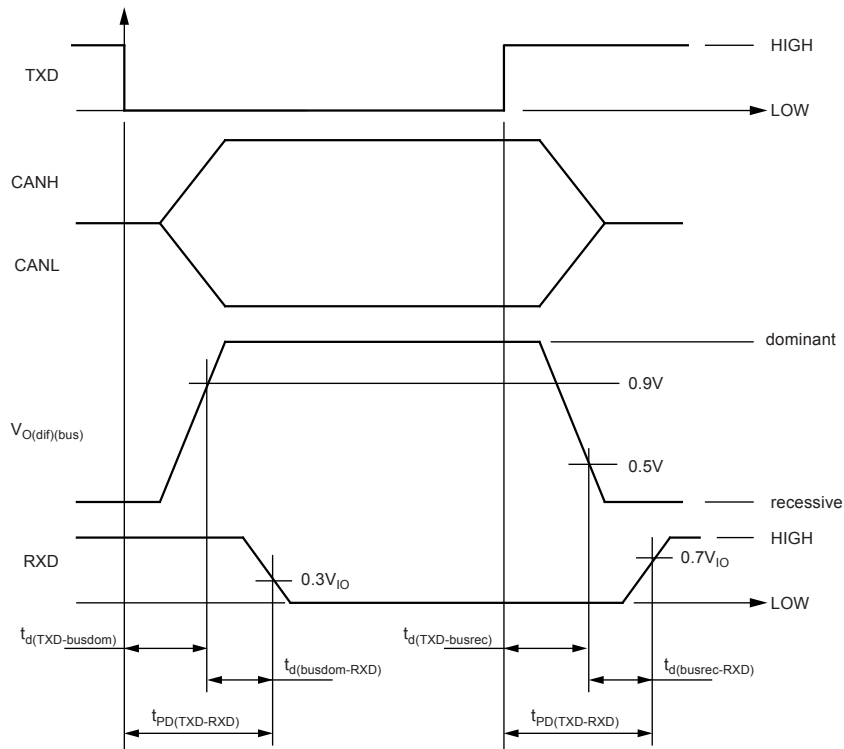
5.2 Measurement Hints

5.2.1 Passive Behavior

In up-to-date in-vehicle networks, partial networking is widely implemented. In these applications, some transceivers can become unpowered (e.g., Clamp-15 nodes), while other transceivers are continuously supplied (e.g., Clamp-30 nodes). In such networks the ATA657X is favored for those applications, which are partly unpowered, because of its excellent passive behavior to the bus when the VCC supply is switched off. In addition, the ATA657X is protected against reverse currents via the pins TXD, RXD and STB. There will be no backward current via those pins if the accompanying microcontroller is still supplied.

5.2.2 Optional Circuitry at CANH and CANL

The EMC performance of the ATA657X has been optimized for use of the CAN termination without a common mode choke. The excellent output stage symmetry allows usage without chokes. If, however, the system performance is still not sufficient, there is the option to use additional measures like common mode chokes (a footprint for a common mode choke is available on the ATAB657XA board), capacitors and ESD clamping diodes. Please note that if any critical measurements on EMI (electromagnetic interference) performance, like electromagnetic immunity or electromagnetic emission, shall be taken, it's recommended to use a dedicated board with highly symmetrical layout for the bus lines and ground-vias at each connection to the ground plane. For investigations on complete links, like bit error measurements, a test board with at least two transceivers is required.

5.2.2.1 Common Mode Choke

A common mode choke provides high impedance for common mode signals and low impedance for differential signals. Due to this, common mode signals produced by RF noise and/or by nonperfect

transceiver driver symmetry get effectively reduced while passing the choke. In fact, a common mode choke helps reduce emission and improve immunity against common mode disturbances. Older transceiver devices usually needed a common mode choke to fulfill the stringent emission and immunity requirements of the automotive industry when using unshielded twisted-pair cable. The ATA657X has the potential to build in-vehicle bus systems without chokes. Whether a choke is needed or not ultimately depends on the specific system implementation such as the wiring harness and the symmetry of the two bus lines (matching tolerances of resistors and capacitors). In addition to the RF noise reduction, the stray inductance (noncoupled portion of inductance) may establish a resonant circuit together with pin capacitance. This can result in unwanted oscillations between the bus pins and the choke, both for differential and common mode signals, and in extra emission around the resonant frequency. To avoid such oscillations, it is highly recommended to use only chokes with a stray inductance lower than 500 nH. Bifilar wound chokes typically show an even lower stray inductance. The choke shall be placed nearest to the transceiver bus pins.

The use of common-mode chokes in CAN systems may cause extremely high transient voltages at the bus pins of the transceiver. These transients are generated by the change in current through the inductance of the common-mode chokes if the CAN bus is shorted to DC voltages. The actual transients that may be generated are highly dependent on the common-mode choke type and value and also depend on the CAN system architecture, termination, components, and location and the severity of the short circuit.

For systems where common-mode chokes are required, care should be used in the choice of the common-mode choke and the system circuit to avoid the introduction of severe transients during DC short-circuit conditions on the bus.

The best methods to avoid transients generated from common-mode chokes during CAN bus line shorts to DC voltages are:

- Remove common-mode chokes from systems, where applicable.
- Move transient suppression circuits between the common-mode choke and the CAN bus pins on the transceiver.
- Choose a common-mode choke type and value and a CAN termination scheme to minimize transients.

5.2.2.2 Capacitors

Matching capacitors (in pairs) at CANH and CANL to GND are frequently used to enhance immunity against electromagnetic interferences. Along with the impedance of corresponding noise sources (RF), capacitors at CANH and CANL to GND form an RC low-pass filter. Regarding immunity, the capacitor value should be as large as possible to achieve a low corner frequency. The overall capacitive load and impedance of the output stage establish an RC low-pass filter for the data signals. The associated corner frequency must be well above the data transmission frequency. This results in a limit for the capacitor value depending on the number of nodes and the data transmission frequency. Notice that capacitors increase the signal loop delay due to reducing rise and fall times. Due to that, bit timing requirements, especially at 1 Mbit/s, call for a value of lower than 100 pF (see also SAE J2284 and ISO11898). At a bit rate of 125 Kbit/s, the capacitor value should not exceed 470 pF. Typically, the capacitors are placed between the common mode choke (if applied at all) and the ESD clamping diodes.

5.2.2.3 ESD Protection

The ATA657X is designed to withstand ESD pulses of up to 8 kV according to the human body model at the bus pins CANH and CANL and thus typically does not need further external protection methods. Nevertheless, if much higher protection is required, external clamping devices can be applied to the CANH and CANL lines.

Care must be taken when selecting the right protection devices. The transient protectors must be fast enough to clamp the transient voltages. In addition, their capacitance must be considered. If the capacitance is too high, it can work together with the choke's inductance and cause ringing on the bus signals. Although this ringing does not corrupt the CAN signals, it may show up as electromagnetic emission at higher frequencies.

6.   Schematics and Layout

This appendix contains the following schematics and layouts for the ATAB657XA:

- ATAB657XA Board Schematic
- Board – Top Silk
- Board – Top Copper and Silk
- Board – Top Copper
- Board – Bottom Copper

6.1   ATAB657XA Board Schematic
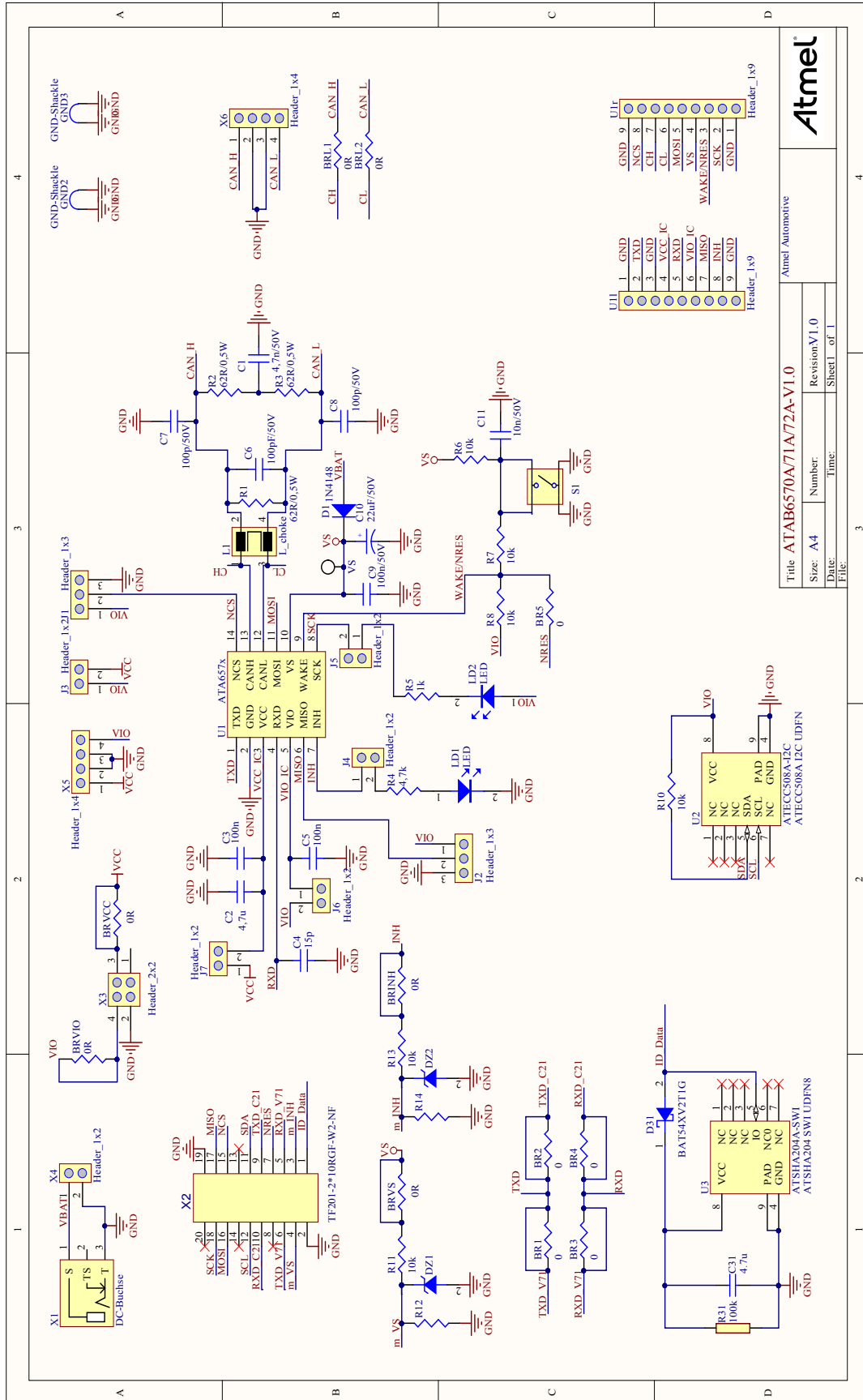
6.2   Board - Top Silk

6.3   Board - Top Copper and Silk
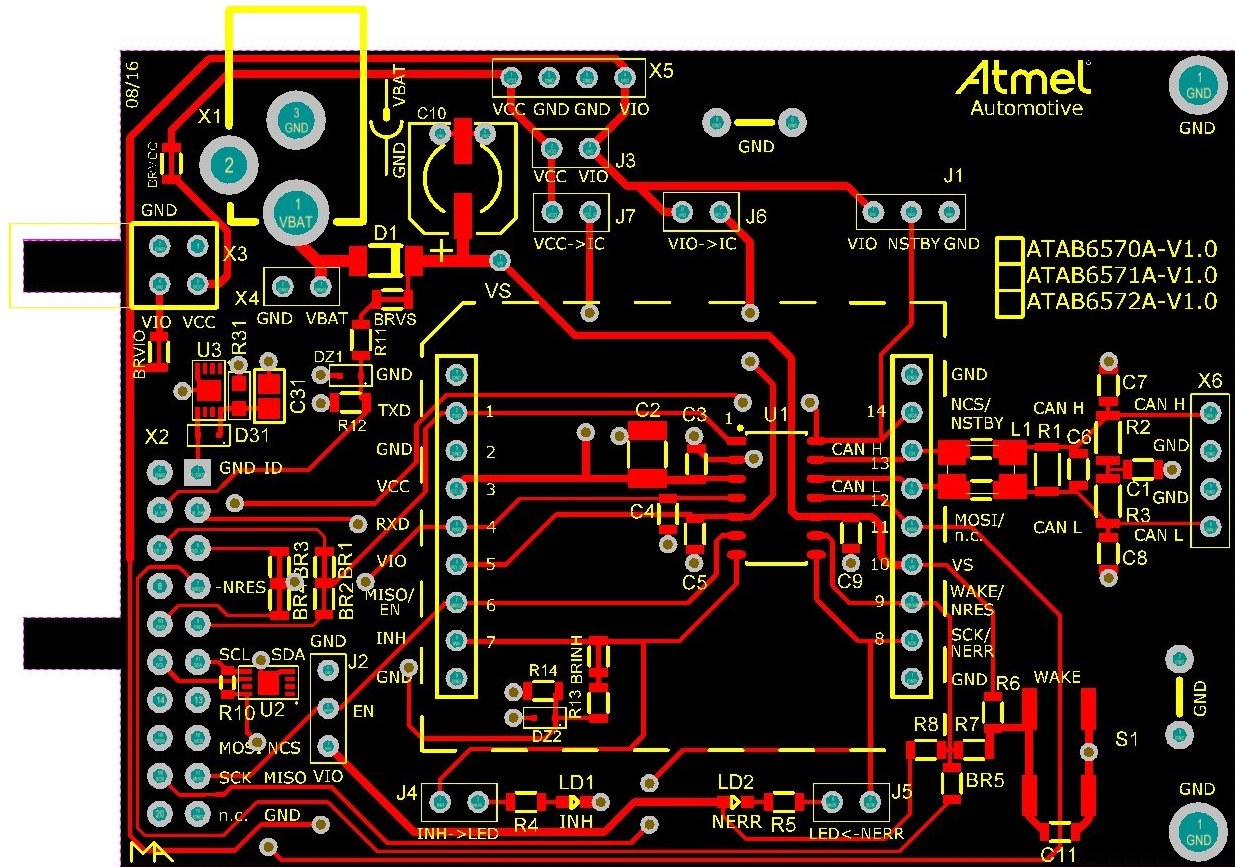
6.4   Board - Top Copper
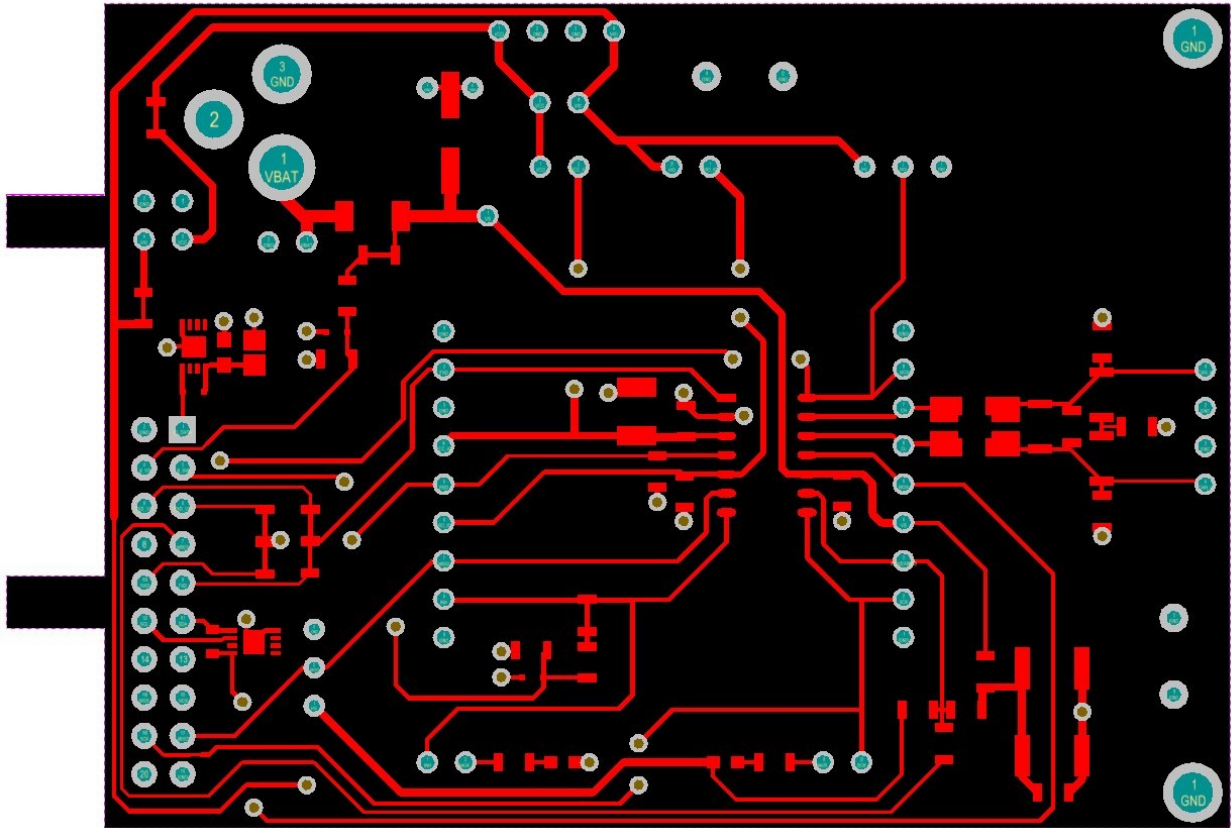
6.5   Board - Bottom Copper
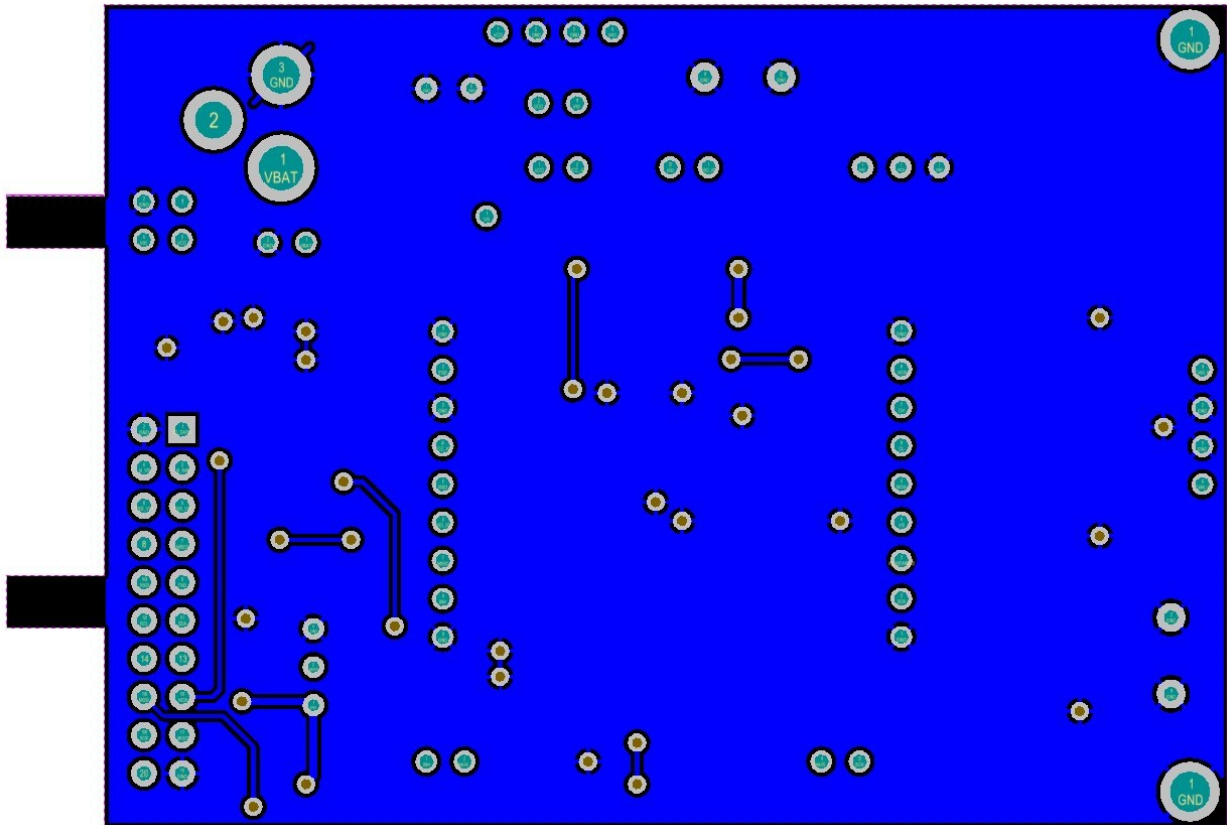
7. ATAB657XA Board BOM

The ATA657X-EK Board is designed to handle all three devices, in SOIC14 package only. It is just a matter of soldering option. In the following table the different solder options are shown.

Table 7-1. ATAB6570 Board BOM

Part	Description	Part Size	Part value
BRL1	Resistor	0805	0Ω
BRL2	Resistor	0805	0Ω
C1	Capacitor	0805	4.7 nF/50V
C2	Capacitor	1210 (MLCC)	10 µF/10V
C3, C5	Capacitor	0805	100 nF
C9	Capacitor	0805	100 nF/50V
C10	Capacitor	1210 (ELKO)	22 µF/50V
C11	Capacitor	0805	10 nF/50V
C31	Ceramic capacitor, SMD 0805, Y5V, 10V, 4.7 µF −20/+80%	AP1-00003	CAP-NONPOL
D1	High Conductance Fast Diode	SOD-80	1N4148
D31	Schottky diode, I_f = 200 mA, V_f = 0.35V, V_{rrm} = 30V, SOD-523	AP4-00036	Farnell# 1615809
DZ1	Zener Diode, SMD SOD-523, 3.3V, 0.2W	AP4-00036	Farnell# 1431218
DZ2	Zener Diode, SMD SOD-523, 3.3V, 0.2W	AP4-00036	Farnell# 1431218
GND2, GND3		GND-Shackle	GND-Shackle
J1, J2		J-Switch 1x3 2.54 mm	Header_1x3
J3, J4, J6, J7		Header 1x2 2.54 mm	Header_1x2
J5		Header 1x2 2.54 mm	Header_1x2
L1	e.g., Epcos CAN Bus Choke B82799	L_Choke	L_choke
LD1	LED	0603_LED_gn	LED
LD2	LED	0603_LED_rt	LED
PCB	ATA6570 Evaluation Board - Printed Circuit Board		**104-10721**
R1	Resistor	1206	62Ω/0.5W
R2, R3	Resistor	1206	62Ω/0.5W

Part	Description	Part Size	Part value
R4	Resistor	0805	4.7 kΩ
R5	Resistor	0805	1 kΩ
R6, R7	Resistor	0805	10 kΩ
R8	Resistor	0805	10 kΩ
R10	Resistor	0603	10 kΩ
R11	Resistor	0805	10 kΩ
R12	Resistor	0805	TBD
R13	Resistor	0805	10 kΩ
R14	Resistor	0805	TBD
R31	Thick film resistor, SMD 0603, 1/10W, 1%	AP2-00001	100 kΩ
S1	Tactile Switch, e.g. KSC241J	ksc241J	Switch
U1	CAN TRX	SO-14	ATA6570
U2	ATECC508A with an I2C Interface and a 8 Pin UDFN Package with Paddle	AP6-00409	ATECC508A-I2C
U3	ATSHA204 with 1-wire interface and UDFN8 package	AP6-00409	ATSHA204A-SWI
X1	DC-Jack	DC- Connector	DC-Connector
X2	2x10, female pin header receptable, right-angled, 2.54 mm pitch, THM, Pin In Paste	AP8-00621	HEADER-2X10
X3		Socket 2x2 2.54 mmRA	Header_2x2
X5, X6		Header 1x4 2.54 mm	Header_1x4

Table 7-2. ATAB6571 Board BOM

Part	Description	Part Size	Part value
BRL1	Resistor	0805	0Ω
BRL2	Resistor	0805	0Ω
C1	Capacitor	0805	4.7 nF/50V
C2	Capacitor	1210 (MLCC)	10 µF/10V
C3, C5	Capacitor	0805	100 nF
C9	Capacitor	0805	100 nF/50V
C10	Capacitor	1210 (ELKO)	22 µF/50V

Part	Description	Part Size	Part value
C11	Capacitor	0805	10 nF/50V
C31	Ceramic capacitor, SMD 0805, Y5V, 10V, 4.7 µF −20/+80%	AP1-00003	CAP-NONPOL
D1	High Conductance Fast Diode	SOD-80	1N4148
D31	Schottky diode, I_f = 200 mA, V_f = 0.35V, V_{rrm} = 30V, SOD-523	AP4-00036	Farnell# 1615809
DZ1	Zener Diode, SMD SOD-523, 3.3V, 0.2W	AP4-00036	Farnell# 1431218
DZ2	Zener Diode, SMD SOD-523, 3.3V, 0.2W	AP4-00036	Farnell# 1431218
GND2, GND3		GND-Shackle	GND-Shackle
J1, J2		J-Switch 1x3 2.54 mm	Header_1x3
J3, J4, J6, J7		Header 1x2 2.54 mm	Header_1x2
J5		Header 1x2 2.54 mm	Header_1x2
LD1	LED	0603_LED_gn	LED
LD2	LED	0603_LED_rt	LED
R2, R3	Resistor	1206	62Ω/0.5W
R4	Resistor	0805	4.7 kΩ
R6, R7	Resistor	0805	10 kΩ
R10	Resistor	0603	10 kΩ
R11	Resistor	0805	10 kΩ
R12	Resistor	0805	TBD
R13	Resistor	0805	10kΩ
R14	Resistor	0805	TBD
R31	Thick film resistor, SMD 0603, 1/10W, 1%	AP2-00001	100 kΩ
S1	Tactile Switch, e.g. KSC241J	ksc241J	Switch
U1	CAN TRX	SO-14	ATA6571
U2	ATECC508A with an I2C Interface and a 8 Pin UDFN Package with Paddle	AP6-00409	ATECC508A-I2C
U3	ATSHA204 with 1-wire interface and UDFN8 package	AP6-00409	ATSHA204A-SWI

Part	Description	Part Size	Part value
X1	DC-Jack	DC- Connector	DC-Connector
X5, X6		Header 1x4 2.54 mm	Header_1x4

Table 7-3. ATAB6572 Board BOM

Part	Description	Part Size	Part value
BR5	Resistor	0805	0Ω
BRL1	Resistor	0805	0Ω
BRL2	Resistor	0805	0Ω
C1	Capacitor	0805	4.7 nF/50V
C2	Capacitor	1210 (MLCC)	10 µF/10V
C3, C5	Capacitor	0805	100 nF
C9	Capacitor	0805	100 nF/50V
C10	Capacitor	1210 (ELKO)	22 µF/50V
C31	Ceramic capacitor, SMD 0805, Y5V, 10V, 4.7 µF −20/+80%	AP1-00003	CAP-NONPOL
D1	High Conductance Fast Diode	SOD-80	1N4148
D31	Schottky diode, I_f = 200 mA, V_f = 0.35V, V_{rrm} = 30V, SOD-523	AP4-00036	Farnell# 1615809
DZ1	Zener Diode, SMD SOD-523, 3.3V, 0.2W	AP4-00036	Farnell# 1431218
DZ2	Zener Diode, SMD SOD-523, 3.3V, 0.2W	AP4-00036	Farnell# 1431218
GND2, GND3		GND-Shackle	GND-Shackle
J3, J4, J6, J7		Header 1x2 2.54mm	Header_1x2
LD1	LED	0603_LED_gn	LED
R2, R3	Resistor	1206	62Ω/0.5W
R4	Resistor	0805	4.7kΩ
R5	Resistor	0805	1kΩ
R8	Resistor	0805	10kΩ
R10	Resistor	0603	10kΩ
R11	Resistor	0805	10kΩ
R12	Resistor	0805	TBD
R13	Resistor	0805	10kΩ
R14	Resistor	0805	TBD

Part	Description	Part Size	Part value
R31	Thick film resistor, SMD 0603, 1/10W, 1%	AP2-00001	100kΩ
U1	CAN TRX	SO-14	ATA6572
U2	ATECC508A with an I2C Interface and a 8 Pin UDFN Package with Paddle	AP6-00409	ATECC508A-I2C
U3	ATSHA204 with 1-wire interface and UDFN8 package	AP6-00409	ATSHA204A-SWI
X1	DC-Jack	DC- Connector	DC-Connector
X2	2x10, female pin header receptable, right-angled, 2.54mm pitch, THM, Pin In Paste	AP8-00621	HEADER-2X10
X3		Socket 2x2 2.54mmRA	Header_2x2
X5, X6		Header 1x4 2.54mm	Header_1x4

8. Register Description

8.1 Device Mode Control Register (Address 0x01)

Name: DMCR
Offset: 0x01
Reset: 0x4
Property:

Bit	7	6	5	4	3	2	1	0
			Reserved[4:0]					
Access	R	R	R	R	R			
Reset	0	0	0	0	0			

Bits 7:3 – Reserved[4:0]   Reserved for future use

8.2 Device Mode Status Register (Address 0x03)

Name: DMSR
Offset: 0x03
Reset: 0x20
Property: Read-only

The register provides device operation mode transition related information to the external microcontroller.

Bit	7	6	5	4	3	2	1	0
	SMTS	OTPWS	NMTS	Reserved[4:0]				
Access	R	R	R	R	R	R	R	R
Reset	0	0	1	0	0	0	0	0

Bit 7 – SMTS Sleep mode transition status
The device sets the bit to '0' if the recent transition to Sleep mode is triggered by an SPI command and sets the bit to '1' if the recent transition to Sleep mode is forced by an VCC/VIO undervoltage.

Bit 6 – OTPWS Over-temperature prewarning status
The device sets the bit to '1' if IC temperature is over over-temperature prewarning threshold and to '0' vice versa.

Bit 5 – NMTS Normal mode transition status
The device sets the bit to '0' when IC has entered Normal mode after power-up and set the bit to '1' when the IC has powered up but has not yet switched to Normal mode.

Bits 4:0 – Reserved[4:0] Reserved for future use

8.3   CAN Transceiver Control Register (Address 0x20)

Name: TRXCR
Offset: 0x20
Reset: 0x41
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved	CFDPE	PNCFOK	CPNE	Reserved[1:0]		COPM[1:0]	
Access	R	R/W	R/W	R/W	R	R	R/W	R/W
Reset	0	1	0	0	0	0	0	1

Bit 7 – Reserved   Reserved for future use

Bit 6 – CFDPE
The external microcontroller should set the bit to '1' to enable the CAN FD passive feature when selective wake-up is activated, should set the bit to '0' vice versa. The bit is set to 1 by default after power on reset. The bit shall be set to 1 for continuous sending "dom-rec" bits with a bitrate higher than 1Mbit/s.

Bit 5 – PNCFOK
The external microcontroller should set the bit to '1' after successfully configuring the partial networking registers, and to '0' vice versa. In addition, the device will reset the bit to 0 automatically after any write access to the partial networking configuration related registers.

Bit 4 – CPNE
The external microcontroller should set the bit to '1' to enable selective wake-up and to '0' vice versa.

Bits 3:2 – Reserved[1:0]   Reserved for future use

Bits 1:0 – COPM[1:0]
The TRXCR register is a control register. Therefore, the state of the transceiver will not be mirrored to this register. COPM bit only defines the expected state of the transceiver when the device is switched to Normal mode. The finite state machine will not change the COPM bits.

COPM[1:0]	CAN TRX Operation Mode
2'b00	TRX Standby mode
2'b01	TRX Normal mode (when DOPM = Normal), VCC undervoltage detection active for the transceiver finite state machine. The transceiver switches to the TRX biased Standby mode immediately after detecting the VCC undervoltage.
2'b10	TRX Normal mode (when DOPM = Normal), VCC undervoltage detection inactive for the transceiver finite state machine. The transceiver switches from TRX Normal/Reduced Normal mode to TRX biased Standby mode when the device is forced to Sleep mode by a VCC undervoltage event.
2'b11	TRX Silent mode

8.4 CAN Transceiver Status Register (Address 0x22)

Name: TRXSR
Offset: 0x22
Reset: 0x48
Property: Read-only

Bit	7	6	5	4	3	2	1	0
	TXS	PNERRS	PNCFS	PNOSCS	CBSS	Reserved	VCCS	TXDOUT
Access	R	R	R	R	R	R	R	R
Reset	0	1	0	0	1	0	0	0

Bit 7 – TXS
Transmitter status, the device sets the bit to '1' if the transmitter is ready to transmit data and to '0' if CAN transmitter is disabled.

Bit 6 – PNERRS
Partial networking error detection status, the device sets the bit to '0' if no CAN partial networking error detected (PNEFD = 0 && PNCFOK = 1 && no oscillator hardware failure detected (default)), to '1' vice versa (PNEFD = 1 || PNCFOK = 0).

Bit 5 – PNCFS
Partial networking configuration status, the device sets the bit to '0' if partial networking configuration error is detected (PNCFOK = 0), to '1' vice versa.

Bit 4 – PNOSCS
Partial networking oscillator ok, the device sets the bit to '1' if CAN partial networking oscillator is running at target frequency, to '0' vice versa.

Bit 3 – CBSS
Bus status, the device sets the bit to '1' if CAN bus is inactive (for longer than $t_{Silence}$), to '0' vice versa.

Bit 2 – Reserved   Reserved for future use

Bit 1 – VCCS
V_{VCC} status, the device sets the bit to '1' if V_{VCC} is below the undervoltage detection threshold, to '0' vice versa.

Bit 0 – TXDOUT
TXD time out status, the device sets the bit to '1' if CAN transmitter is disabled due to a TXD dominant timeout event, to '0' if no TXD dominant timeout event was detected.

8.5 Bus Failure Indication Register (Address 0x33)

Name: BFIR
Offset: 0x33
Reset: 0x00
Property: Read-only

Bit	7	6	5	4	3	2	1	0
				Reserved[5:0]			BOUT	BSC
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[5:0]   Reserved for future use

Bit 1 – BOUT
Bus dominant timeout event indicator, the BOUT bit shows the current status of the bus dominant timeout detection. If the bit reads '1' the bus is currently in dominant timeout state; otherwise the bit reads '0'.

Bit 0 – BSC
Bus short-circuit event capture indicator, the BSC bit shows the current status of the bus short-circuit event detection. If the bit reads '1' the bus is currently in short-circuit state; otherwise the bit reads '0'.

8.6   Transceiver Event Status Register 2 (Address 0x35)

Name: TRXESR2
Offset: 0x35
Reset: 0x00
Property: Read-only

Bit	7	6	5	4	3	2	1	0
				Reserved[6:0]				RXDRCS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:1 – Reserved[6:0]   Reserved for future use

Bit 0 – RXDRCS
RXD recessive clamping status, the device sets the bit to '1' if the event is enabled in the TRXECR2 register and a RXD recessive clamping event is detected. The bit is reset to '0' by the device either when the device enters Sleep, or Standby or Unpowered mode or the RXD pin shows dominant again.

8.7 Data Rate Configuration Register (Address 0x26)

Name: DRCR
Offset: 0x26
Reset: 0x05
Property:

Bit	7	6	5	4	3	2	1	0
			Reserved[4:0]				DR[2:0]	
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	1

Bits 7:3 – Reserved[4:0] Reserved for future use

Bits 2:0 – DR[2:0] Select CAN data rate

DR[2:0]	CAN Data Rate (Kbit/s)
3'b000	50
3'b001	100
3'b010	125
3'b011	250
3'b100	Reserved (intended for future use; currently selects 500Kbit/s)
3'b101	500
3'b110	Reserved (intended for future use; currently selects 500Kbit/s)
3'b111	1000

8.8   CAN ID Register 0 (Address 0x27)

Name: CIDR0
Offset: 0x27
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				ID0[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ID0[7:0]
ID0 bits ID07 to ID00 of the extended frame format

8.9   CAN ID Register 1 (Address 0x28)

Name: CIDR1
Offset: 0x28
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
				ID1[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ID1[7:0]
ID1 bits ID15 to ID08 of the extended frame format

8.10 CAN ID Register 2 (Address 0x29)

Name: CIDR2
Offset: 0x29
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				ID2[5:0]			ID2[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – ID2[5:0]
ID2 bits ID23 to ID18 of the extended frame format; bits ID05 to ID00 of the standard frame format

Bits 1:0 – ID2[1:0]
ID2 bits ID17 to ID16 of the extended frame format

8.11 CAN ID Register 3 (Address 0x2A)

Name: CIDR3
Offset: 0x2A
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
		Reserved[2:0]				ID3[4:0]		
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – Reserved[2:0] Reserved for future use

Bits 4:0 – ID3[4:0]
ID3 bits ID28 to ID24 of the extended frame format, bits ID10 to ID06 of the standard frame format

8.12   CAN ID Mask Register 0 (Address 0x2B)

Name: CIDMR0
Offset: 0x2B
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				IDM0[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – IDM0[7:0]
IDM0 Mask bits ID07 to ID00 of the extended frame format. 1 means 'don't care'.

8.13   CAN ID Mask Register 1 (Address 0x2C)

Name: CIDMR1
Offset: 0x2C
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				IDM1[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – IDM1[7:0]
IDM1 Mask bits ID15 to ID08 of the extended frame format. 1 means 'don't care'.

8.14 CAN ID Mask Register 2 (Address 0x2D)

Name: CIDMR2
Offset: 0x2D
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	IDM2[5:0]						IDM2[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – IDM2[5:0]
IDM2 Mask bits ID23 to ID18 of the extended frame format; bits ID05 to ID00 of the standard frame format

Bits 1:0 – IDM2[1:0]
IDM2 Mask bits ID17 to ID16 of the extended frame format. 1 means 'don't care'.

8.15 CAN ID Mask Register 3 (Address 0x2E)

Name: CIDMR3
Offset: 0x2E
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved[2:0]			IDM3[4:0]				
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – Reserved[2:0] Reserved for future use

Bits 4:0 – IDM3[4:0]
IDM2 Mask bits ID17 to ID16 of the extended frame format. 1 means 'don't care'.

8.16 CAN Frame Configuration Register (Address 0x2F)

Name: CFCR
Offset: 0x2F
Reset: 0x40
Property:

Bit	7	6	5	4	3	2	1	0
	IDE	PNDM	Reserved[1:0]		DLC[3:0]			
Access	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

Bit 7 – IDE
Identifier format, the external microcontroller should set the bit to '1' if identifier is in extended frame
format (29-bit), set to '0' if identifier is in standard frame format (11-bit)

Bit 6 – PNDM
Partial networking data mask, the external microcontroller should set the bit '1' if data length code and
data field are evaluated at wake-up, set to '0' if data length code and data field are 'don't care' for wake-
up

Bits 5:4 – Reserved[1:0] Reserved for future use

Bits 3:0 – DLC[3:0]
Data length configuration, select number of data bytes expected in a CAN frame

DLC[3:0]	Number of Data Bytes
4'b0000	0
4'b0001	1
4'b0010	2
4'b0011	3
4'b0100	4
4'b0101	5
4'b0110	6
4'b0111	7
4'b0000	8
4'b1001 to 4'b1111	Tolerated, 8 bytes expected; DM0 (data mask 0) ignored

8.17 Error Frame Counter Threshold Register (Address 0x3A)

Name: EFCR
Offset: 0x3A
Reset: 0x1F
Property:

Bit	7	6	5	4	3	2	1	0
		Reserved[2:0]				EERCNT[4:0]		
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	1

Bits 7:5 – Reserved[2:0] Reserved for future use

Bits 4:0 – EERCNT[4:0]
Set the error frame counter overflow threshold. If the counter overflows (counter > ERRCNT), a frame detect error is captured (PNEFD = 1) and the device wakes up.

8.18 Failure Error Counter Register (Address 0x3B)

Name: FECR
Offset: 0x3B
Reset: 0x00
Property: Read-only

Bit	7	6	5	4	3	2	1	0
		Reserved[2:0]				FEC[4:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – Reserved[2:0] Reserved for future use

Bits 4:0 – FEC[4:0]
If the device receives a CAN frame containing errors (e.g., a 'stuffing' error) that are received in advance of the ACK field, an internal error counter is incremented. If a CAN frame is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (FEC > ERRCNT, see section FECR – Failure Error Counter Register (address 0x3B)), a frame detect error is captured (PNEFD = 1, see section TRXESR – Transceiver Event Status Register (address 0x63)) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

8.19   Glitch Filter Threshold Register (Address 0x67)

Name: GLFT
Offset: 0x67
Reset: 0x02

Bit	7	6	5	4	3	2	1	0
			Reserved[4:0]				GLF[2:0]	
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	0

Bits 7:3 – Reserved[4:0] Reserved for future use

Bits 2:0 – GLF[2:0]
Set the glitch filter threshold from 5% to 55% of the arbitration bit rate.

GLF[2:0]	#samples(≤500Kbit/s)	#samples(1Mbit/s)
3'b000	1 [<2.42%/<5.17%]	1 [<4.83%/<10.35%]
3'b001	2 [<4.83%/<7.76%]	2 [<9.66%/<15.52%]
3'b010	3 [<7.25%/<10.35%]	3 [<14.49%/<20.7%]
3'b011	4 [<9.66%/<12.94%]	4 [<19.32%/<20.87%]
3'b100	5 [<12.08%/<15.52%]	5 [<24.15%/<31.05%]
3'b101	6 [<14.49%/<18.11%]	6 [<28.99%/<36.22%]
3'b110	7 [<16.91%/<20.7%]	7 [<33.82%/<41.40%]
3'b111	24 [<57.97%/<64.69%]	13 [<62.8%/<72.45%]

8.20   CAN Data Mask Registers 0...7 (Address 0x68…0x6F)

Name: CDMR0..7
Offset: 0x68…0x6F
Reset: 0xFF

Bit	7	6	5	4	3	2	1	0
				DM0...7[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 7:0 – DM0...7[7:0] data mask 0…7 configuration

Table 8-1. Data Mask and the CAN Data Filed

CAN frame	...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC	...
Data mask	DLC > 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame	...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC	...
Data mask	DLC = 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame	...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC	...
Data mask	DLC = 7			DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame		...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	CRC	...
Data mask	DLC = 6				DM2	DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame			...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	CRC	...
Data mask	DLC = 5					DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame				...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	CRC	...
Data mask	DLC = 4						DM4	DM5	DM6	DM7	CRC	...
CAN frame					...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	CRC	...
Data mask	DLC = 3							DM5	DM6	DM7	CRC	...
CAN frame						...	DLC	Byte 0	Byte 1	Byte 2	CRC	...
Data mask	DLC = 2								DM6	DM7	CRC	...
CAN frame							...	DLC	Byte 0	Byte 1	CRC	...
Data mask	DLC = 1									DM7	CRC	...
CAN frame								...	DLC	Byte 0	CRC	...

DM x							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Byte x							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

8.21   Bus Failure Event Capture Enable Register (Address 0x32)

Name: BFECR
Offset: 0x32
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
			Reserved[5:0]					BOUTE	BSCE
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[5:0] Reserved for future use

Bit 1 – BOUTE
bus dominant timeout event capture enable, the BOUTE bit must be set to '1' to enable the bus dominant timeout detection. Setting the bit to `0` disables the bus dominant timeout detection.

Bit 0 – BSCE
bus short-circuit event capture enable, the BSCE bit must be set to '1' to enable the bus short-circuit event detection. Setting the bit to `0` disables the bus short-circuit event detection.

8.22   Pin WAKE Status Register (Address 0x4B)

Name: PWKS
Offset: 0x4B
Reset: 0x00
Property: Read-only

Bit	7	6	5	4	3	2	1	0
			Reserved[5:0]				PWKVS	Reserved
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[5:0] Reserved for future use

Bit 1 – PWKVS
Pin WAKE voltage status, the device sets the bit to '1' if WAKE is high, to '0' if WAKE is low. PWKVS is always "0" in power-down mode if local wake-up is disabled.

Bit 0 – Reserved Reserved for future use

8.23   Global Event Status Register (Address 0x60)

Name: GESR
Offset: 0x60
Reset: 0x01
Property: Read-only

Bit	7	6	5	4	3	2	1	0
	OSCS	Reserved	BFES	Reserved	WKES	TRXES	Reserved	SYSES
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

Bit 7 – OSCS
System oscillator status, the device sets the bit to '1' if a hardware failure of the system oscillator is detected and sets the bit to '0' when the system oscillator is disabled for power saving purpose or the hardware failure disappeared after the oscillator is enabled (for instance, in device Normal mode).

Bit 6 – Reserved Reserved for future use

Bit 5 – BFES
Bus failure event status, the device sets the bit to '1' if there is bus failure event pending (any bit in the BFESR register is '1'). The bit reads '0' if all status bits in the BFESR register are cleared.

Bit 4 – Reserved Reserved for future use

Bit 3 – WKES
WAKE event status, the device sets the bit to '1' if there is a wake pin event pending (any bit in the WKESR register is '1'). The bit reads '0' if all status bits in the WKESR register are cleared.

Bit 2 – TRXES
Transceiver event status, the device sets the bit to '1' if there is a transceiver event pending (any bit in the TRXESR register is '1'). The bit reads '0' if all status bits in the TRXESR register are cleared.

Bit 1 – Reserved Reserved for future use

Bit 0 – SYSES
SYSES System event status, the device sets the bit to '1' if there is a system event pending (any bit in the SESR register is '1'). The bit reads '0' if all status bits in the SESR register are cleared.

8.24 System Event Status Register (Address 0x61)

Name: SESR
Offset: 0x61
Reset: 0x10
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved[2:0]			PWRONS	Reserved	OTPW	SPIFS	Reserved
Access	R	R	R	R/W	R	R/W	R/W	R
Reset	0	0	0	1	0	0	0	0

Bits 7:5 – Reserved[2:0] Reserved for future use

Bit 4 – PWRONS
Power on status, the device sets the bit to '1' if the device has left Power off mode after power-on. The bit can be reset to '0' by writing a '1' to the bit. PWRONS is also cleared when the device is forced to Sleep mode due to an undervoltage event. The information stored in PWRONS could be lost in this case. Bit NMTS in the Device Mode Status Register (DMSR), which is set to 0 when the device switches to Normal mode after power-on, compensates for this.

Bit 3 – Reserved Reserved for future use

Bit 2 – OTPW
Overtemperature prewarning status, the device sets the bit to '1' if the event is enabled in the SECR register and the chip temperature has exceeded the overtemperature prewarning threshold. The bit can be reset to '0' by writing a '1' to the bit. OTPW is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bit 1 – SPIFS
SPI failure status, the device sets the bit to '1' if the event is enabled in the SECR register and an SPI failure is detected. The bit can be reset to '0' by writing a '1' to the bit. SPIFS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bit 0 – Reserved Reserved for future use

8.25 Transceiver Event Status Register (Address 0x63)

Name: TRXESR
Offset: 0x63
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[1:0]		PNEFD	BS	Reserved[1:0]		TRXF	CWUS
Access	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:6 – Reserved[1:0] Reserved for future use

Bit 5 – PNEFD
Partial networking frame detection status, the device sets the bit to '1' if a partial networking frame detection error is detected (error counter overflow). The bit can be reset to '0' by writing a '1' to the bit. PNEFD is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bit 4 – BS
Bus status, the device sets the bit to '1' if the event is enabled in the TRXECR register and no activity on CAN bus is detected for tSilence. The bit can be reset to '0' by writing a '1' to the bit. BS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bits 3:2 – Reserved[1:0] Reserved for future use

Bit 1 – TRXF
Transceiver failure status, the device sets the bit to '1' if the event is enabled in the TRXECR register and a CAN failure event was detected. The bit can be reset to '0' by writing a '1' to the bit. TRXF is also cleared when the device is forced to Sleep mode due to an undervoltage event. TRXF is triggered if:
- TXD is clamped dominant and system is in TRX Normal mode
- a VCC undervoltage is detected, COPM = 01 and system is in TRX Normal or TRX Reduced Normal mode
- a RXD recessive clamping error is detected and system is in TRX Normal or TRX Silent mode.

The RXD recessive clamping error detection must additionally be enabled in the TRXECR2 register.

Bit 0 – CWUS
CAN wake-up status, the device sets the bit to '1' if the event is enabled in the TRXECR register and a CAN wake-up event was detected. The bit can be reset to '0' by writing a '1' to the bit. CWUS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

8.26   WAKE Event Status Register (Address 0x64)

Name: WKESR
Offset: 0x64
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				Reserved[5:0]			LWURS	LWUFS
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[5:0]   Reserved for future use

Bit 1 – LWURS
Local Wake-up Rising Edge Status, the device sets the bit to '1' if the event detection is enabled in the WKECR register and a rising edge on the WAKE pin is detected. The bit can be reset to '0' by writing a '1' to the bit. LWURS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bit 0 – LWUFS
Local Wake-up Falling Edge Status, the device sets the bit to '1' if the event detection is enabled in the WKECR register and a falling edge on WAKE pin is detected. The bit can be reset to '0' by writing a '1' to the bit. LWUFS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

8.27 Bus Failure Event Indication Status Register (Address 0x65)

Name: BFESR
Offset: 0x65
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
				Reserved[5:0]			BOUTS	BSCS
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[5:0]   Reserved for future use

Bit 1 – BOUTS
Bus dominant timeout event status bit, the device sets the bit to '1' if a bus dominant timeout event is detected. The bit is set to '0' by writing '1' to the bit via SPI.

Bit 0 – BSCS
Device bus short-circuit event status bit, the device sets the bit to '1' if a bus short-circuit event is detected. The bit is set to '0' by writing '1' to the bit via SPI.

8.28 System Event Capture Enable Register (Address 0x04)

Name: SECR
Offset: 0x04
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
			Reserved[4:0]			OTPWE	SPIFE	Reserved
Access	R	R	R	R	R	R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

Bits 7:3 – Reserved[4:0] Reserved for future use

Bit 2 – OTPWE
overtemperature prewarning event capture, the OTPWE bit must be set to '1' to enable the
overtemperature prewarning detection. Setting the bit to '0' disables the overtemperature prewarning
detection.

Bit 1 – SPIFE
SPI failure event capture, the SPIFE bit must be set to '1' to enable the SPI failure detection. Setting the
bit to '0' disables the SPI failure detection.

Bit 0 – Reserved Reserved for future use

8.29 Transceiver Event Capture Enable Register (Address 0x23)

Name: TRXECR
Offset: 0x23
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[2:0]			BSE	Reserved[1:0]		TRXFE	CWUE
Access	R	R	R	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – Reserved[2:0] Reserved for future use

Bit 4 – BSE
BSE Bus status capture enable, the BSE bit must be set to '1' to enable the CAN bus silence detection. Setting the bit to '0' disables the CAN bus silence detection.

Bits 3:2 – Reserved[1:0] Reserved for future use

Bit 1 – TRXFE
Transceiver failure status capture enable, the TRXFE bit must be set to '1' to enable the CAN failure detection. Setting the bit to '0' disables the CAN failure detection.

Bit 0 – CWUE
CAN bus wake-up detection enable, the CWUE bit must be set to '1' to enable the CAN wake-up detection. Setting the bit to '0' disables the CAN wake-up detection. At an undervoltage event the bit is set to '1' automatically.

8.30 Transceiver Event Capture Enable Register 2 (Address 0x34)

Name: TRXECR2
Offset: 0x34
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				Reserved[6:0]				RXDRCE
Access	R	R	R	R	R	R	R	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:1 – Reserved[6:0] Reserved for future use

Bit 0 – RXDRCE
RXD recessive clamping capture enable, the RXDRCE bit must be set to '1' to enable the RXD recessive clamping detection. Setting the bit to '0' disables the RXD recessive clamping detection.

8.31 WAKE Event Capture Enable Register (Address 0x4C)

Name: WKECR
Offset: 0x4C
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[5:0]						LWURE	LWUFE
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[5:0]   Reserved for future use

Bit 1 – LWURE
The bit must be set to "1" to enable the WAKE pin rising edge detection interrupt. Setting the bit to "0" disables the interrupt. The LWURE bit is set automatically before a Sleep mode is activated due to an undervoltage event.

Bit 0 – LWUFE
The bit must be set to "1" to enable the WAKE pin falling edge detection interrupt. Setting the bit to "0" disables the interrupt. The LWUFE bit is set automatically before a Sleep mode is activated due to an undervoltage event.

8.32 Device ID Register (Address 0x7E)

Name: DIDR
Offset: 0x7E
Reset: 0x74
Property: Read-only

The register provides the ID of the ATA6570.

Bit	7	6	5	4	3	2	1	0
				DID[7:0]				
Access	R	R	R	R	R	R	R	R
Reset	0	1	1	1	0	1	0	0

Bits 7:0 – DID[7:0]
The device ID is 0x74 for ATA6570.

8.33 Register Write Protection Register (Address 0x0A)

Name: RWPR
Offset: 0x0A
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved	WP6	WP5	WP4	WP3	WP2	WP1	WP0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – Reserved Reserved for future use

Bit 6 – WP6
address area 0x67 to 0x6F – partial networking data byte registers, the external microcontroller should set the bit to '1' to enable register write protection, to '0' vice versa

Bit 5 – WP5
address area 0x50 to 0x5F – the external microcontroller should set the bit to '1' to enable register write protection, to '0' vice versa

Bit 4 – WP4
address area 0x40 to 0x4F– WAKE pin configuration, the external microcontroller should set the bit to '1' to enable register write protection, to '0' vice versa

Bit 3 – WP3
address area 0x30 to 0x3F– the external microcontroller should set the bit to '1' to enable register write protection, to '0' vice versa

Bit 2 – WP2
address area 0x20 to 0x2F– transceiver control and partial networking, the external microcontroller should set the bit to '1' to enable register write protection, to '0' vice versa

Bit 1 – WP1
address area 0x10 to 0x1F – the external microcontroller should set the bit to '1' to enable register write protection, to '0' vice versa

Bit 0 – WP0
address area 0x06 to 0x09 – the external microcontroller should set the bit to '1' to enable register write protection, to '0' vice versa

8.34   Watchdog Configuration Register 1 (Address 0x36)

Name: WDCR1
Offset: 0x36
Reset: 0x22
Property:

Bit	7	6	5	4	3	2	1	0
		WDC[2:0]		WDPRE[1:0]		WDSLP	WDLW	ADCH
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	1	0

Bits 7:5 – WDC[2:0] Watchdog mode control

WDC	Device Operation Mode
001	Off mode (default in the Atmel ATA65670)
010	Timeout mode
100	Window mode

Bits 4:3 – WDPRE[1:0] Watchdog Period control (extend watchdog period T ms by the factor defined below)

WDPRE	Device Operation Mode
00	Watchdog prescale factor 1 (default)
01	Watchdog prescale factor 1.5
10	Watchdog prescale factor 2.5
11	Watchdog prescale factor 3.5

Bit 2 – WDSLP
Set to 1 to let the window watchdog running in Sleep mode, otherwise set to 0.

Bit 1 – WDLW
Set to 1 if a reset to window watchdog timer and a long open window exist after INH switch to high. Otherwise set to 0.

Bit 0 – ADCH
Enable (1) and disable (0) active discharger of external voltage regulator via VIO pin. By default set to 0.

Eight watchdog periods (8ms to 4096ms) are supported in the Atmel ATA6570. The watchdog period is programmable via the watchdog period bits (WWDP) in the watchdog control register 2 (WDCR2). The selected period is valid for both Window and Timeout modes. The default watchdog period is 128ms. A watchdog trigger event (an SPI write access to WDTRIG register with the pattern 01010101) resets the watchdog timer. The watchdog period and the reset pulse width can also be configured via the WRPL bits in the watchdog control register 2. A window watchdog active discharger is integrated in the Atmel ATA6570 to ensure a predictable reset of the external microcontroller. If the WWD active discharger is

activated (ADCH = 1), the discharger will draw a minimum of 2mA discharging current from VIO pin when a microcontroller reset is triggered by the window watchdog.

In order to let the WWD continue working when the device is in Sleep mode, the WDSLP bit of the WWD control register must be set to 1. When the device goes to Sleep mode with WDSLP = 1, the counter gets reset and restarts counting immediately. Otherwise, the WWD counter is reset when the device switches to Sleep mode and waits the next INH low-to-high event to restart itself (entering long window mode if the mode is enabled).

8.35   Watchdog Control Register 2 (Address 0x37)

Name: WDCR2
Offset: 0x37
Reset: 0x47
Property:

Bit	7	6	5	4	3	2	1	0
			WWDP[3:0]				WRPL[3:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	1	1	1

Bits 7:4 – WWDP[3:0] Window watchdog period configuration (ms, prescale factor = 1, ±10%)

WWDP	Watchdog period
1000	8
0001	16
0010	32
1011	64
0100	128 (default)
1101	256
1110	1024
0111	4096

Bits 3:0 – WRPL[3:0] Window watchdog reset pulse length (ms)

WRPL	Reset pulse length
1000	1 to 1.5
0001	3.6 to 5
0010	10 to 12.5
1011	20 to 25
0100	40 to 50
1101	60 to 75
1110	100 to 125
0111	150 to 190 (default)

The watchdog is a valuable safety mechanism, so it is critical that it is configured correctly. Two features are provided to prevent watchdog parameters being changed by mistake:

- Redundant states of configuration bits WDC, WWDP and WRPL

- Reconfiguration protection: only configurable in Standby mode.

Redundant states associated with control bits WDC, WWDP and WRPL ensure that a single bit error cannot cause the watchdog to be configured incorrectly (at least two bits must be changed to reconfigure WDC, WWDP or WRPL). If an attempt is made to write an invalid code to WDCR1 register or WDCR2 register, the SPI operation is abandoned and the CACC bit in watchdog status register is set. The inhibit output is switched off.

8.36 Watchdog Status Register (Address 0x38)

Name: WDSR
Offset: 0x38
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	OFF	CACC	ILLCONF	TRIGS	OF	OFSLP	ETRIG	Reserved
Access	R	R/W	R/W	R	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

Bit 7 – OFF
Window watchdog is off

Bit 6 – CACC
Corrupted write access to the window watchdog configuration registers

Bit 5 – ILLCONF
An attempt is made to reconfigure the watchdog control register while the device is not in Standby mode

Bit 4 – TRIGS
The device set the bit to 1 if window watchdog is in first half of window and set the bit to 0 of window watchdog is in second half of window. If the WWD is not in window mode, the bit is always be set to 0.

Bit 3 – OF
Watchdog overflow (Timeout mode or Window mode in Standby or Normal mode)

Bit 2 – OFSLP
Watchdog overflow in Sleep mode (Timeout mode)

Bit 1 – ETRIG
Watchdog triggered too early (Window mode)

Bit 0 – Reserved
Reserved for future use

Writing 1 to the corresponding bit of the watchdog status register will reset the bit. A microcontroller reset is triggered immediately in response to an illegal watchdog configuration (configuration of WWD in Normal or Sleep mode), a watchdog failure in Window mode (watchdog overflow or triggered too early), and when the watchdog overflows in Timeout mode. If a reset is triggered by the window watchdog, the window watchdog reset event register will be set. The device will enter the reset mode and enter Standby mode after reset is finished.

If there is a corrupted write access to the window watchdog configuration registers, or/and an illegal configuration of watchdog control register when the watchdog is in Off mode, the corresponding status register bit will be set. If the register bits are not reset to zero before enable the window watchdog, a reset will be triggered to the microcontroller immediately after enabling the window watchdog.

8.37 Watchdog Trigger Register (Address 0x39)

Name: WDTRIG
Offset: 0x39
Reset: 0x00
Property: Write-only

Bit	7	6	5	4	3	2	1	0
				WDTRIG[7:0]				
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – WDTRIG[7:0]
A watchdog trigger event (an SPI write access to WDTRIG register with the pattern 01010101) resets the watchdog timer.

8.38 General purpose memory 0 (Address 0x06)

Name: GPM0
Offset: 0x06
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				GPM0[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPM0[7:0]
General purpose memory bits

8.39   General purpose memory 1 (Address 0x07)

Name: GPM1
Offset: 0x07
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				GPM1[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPM1[7:0]
General purpose memory bits

8.40   General purpose memory 2 (Address 0x08)

Name: GPM2
Offset: 0x08
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				GPM2[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPM2[7:0]
General purpose memory bits

8.41   General purpose memory 3 (Address 0x09)

Name: GPM3
Offset: 0x09
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
				GPM3[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPM3[7:0]
General purpose memory bits

9.   Revision History

Revision A (February 2018)
Original Release of the Document.

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PART NO. [X][1] - X /XX XXX

Device | Tape and Reel Option | Temperature Range | Package | Pattern

Device:	PIC16F18313, PIC16LF18313, PIC16F18323, PIC16LF18323	
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel[1]
Temperature Range:	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package:[2]	JQ	= UQFN
	P	= PDIP
	ST	= TSSOP
	SL	= SOIC-14
	SN	= SOIC-8
	RF	= UDFN
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

- PIC16LF18313- I/P Industrial temperature, PDIP package
- PIC16F18313- E/SS Extended temperature, SSOP package

Note:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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