Precision Analog Microcontroller with Chemical Sensor Interface

Preliminary Technical Data

ADuCM355

FEATURES

- Analog input/output
  - 16-bit, 400 kSPS ADC
  - Voltage, current, and impedance measurement capability
    - Internal/external current and voltage channels
    - Ultralow leakage switch matrix and input mux
    - Input buffers, programmable gain amplifier
- Voltage DACs
  - 2 dual output VDACs
    - Output range 0.2 V to 2.4 V (±2.2 V voltage potential to sensor)
    - 2 bias potentiostat and TIA amplifiers
      - Ultralow power, 1 µA per DAC
  - One high speed 12-bit VDAC
    - Output range to sensor ±607 mV
    - High speed TIA for impedance measurements
    - Programmable gain amplifier on output
- Amplifiers, accelerators, and references
  - 2 low power, low noise amplifiers
    - Suitable for potentiostat bias in electrochemical sensing
  - 2 low power, low noise TIAs
    - Suitable for measuring sensor current output
      - 200 pA to 3 mA range
    - Programmable load and gain resistors
  - Analog hardware accelerators
    - DDS waveform generator
    - DFT and digital filters
  - 2.5 V and 1.82 V on-chip, precision voltage references
- Internal temperature sensor, ±2°C accurate
- Impedance measurement range of <1 Ω to 10 MΩ, 1 Hz to 200 kHz
- Voltammetry scan rate up to 2000 steps per second
- Microcontroller
  - 26 MHz ARM Cortex-M3 processor
  - Serial wire port supports code download and debug
  - 128 kB flash/64 kB of SRAM
- Security/safety
  - Hardware crypto accelerator with AES-128 and AES-256
  - Hardware CRC with programmable polynomial generator
  - Read/write protection of user flash
- On-chip peripherals
  - UART, I^2C, and SPI serial input/output
  - Up to 10 GPIO pins
    - External interrupt option
  - General-purpose, wake-up, and watchdog timers
- Power
  - 2.8 V to 3.6 V supply and active measurement range
  - Power-supply monitor
  - Active current consumption 30 µA/MHz for digital part
  - Hibernate with bias to external sensor, 8.5 µA
  - Shutdown mode with no SRAM retention, 2 µA
- Packages and temperature range
  - 6 mm × 5 mm, 72-lead LGA package
  - Fully specified for −40°C to +85°C ambient operation

APPLICATIONS

- Gas detection
- Food quality
- Environmental sensing (air, water, soil)
- Blood glucose meters
- Life sciences and biosensing analysis
- Bioimpedance measurements
- General Amperometry, voltammetry, and impedance spectroscopy functions

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

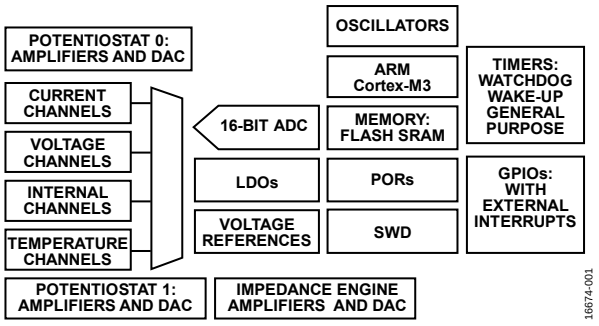

Figure 1.

Rev. PrB
Document Feedback

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GENERAL DESCRIPTION

The ADuCM355 is an on-chip system designed to control and measure electrochemical and biosensors. The ADuCM355 is an ultralow power mixed-signal microcontroller based on the ARM®Cortex™-M3 processor. It is designed with current, voltage, and impedance measurement capability.

The ADuCM355 features a 16-bit, 400 kSPS multichannel successive approximation register (SAR) analog-to-digital converter (ADC) with input buffers, built in antialias filter (AAF) and programmable gain amplifier (PGA). The current inputs include three transimpedance amplifiers (TIA) with programmable gain and load resistors for measuring different sensor types. The analog front end (AFE) also contains two more low power amplifiers designed specifically for potentiostat capability to maintain a constant bias voltage to an external electrochemical sensor. The noninverting inputs of these two amplifiers are controlled by on-chip dual output digital-to-analog converters (DAC). The analog outputs include another high speed DAC and output amplifier designed to generate an ac signal.

The ADC is capable of operating at conversion rates up to 400 kSPS with an input range of ±0.9 V. An input mux before the ADC allows the user to select an input channel for measurement. These input channels include three external current inputs, multiple external voltage inputs, and internal channels. The internal channels allow diagnostic measurements of the internal supply voltages, die temperature, and reference voltages.

Two of the three voltage DACs are dual output, 12-bit string DACs. One output per DAC controls the noninverting input of a potentiostat amplifier, and the other controls the noninverting input of the TIA.

The third DAC (sometimes referred to as the high speed DAC) is designed for the high power TIA for impedance measurements. Its output frequency range is up to 200 kHz.

A precision 1.82 V and 2.5 V on-chip reference source is available. The internal ADC and VDAC circuits use this on-chip reference source to ensure low drift performance for all of these peripherals.

The ADuCM355 integrates a 26 MHz ARM Cortex-M3 processor. It is a 32-bit reduced instruction set computer (RISC) machine, offering up to 32.5 DMIPS peak performance. The ARM Cortex-M3 processor also has a flexible multichannel direct memory access controller (DMA) supporting serial peripheral interface (two independent SPI ports), universal asynchronous receiver/transmitter (UART), and I^2C communication peripherals. The ADuCM355 has 128 kB of nonvolatile flash/EE memory and 64 kB of SRAM integrated on-chip.

The digital processor subsystem is clocked from a 26 MHz on-chip oscillator. This is the source of the main digital die system clock. Optionally, a 26 MHz PLL can be used as the digital system clock. This clock can be internally subdivided so that the processor operates at a lower frequency and saves power. A low power internal 32 kHz oscillator is available and can clock the timers. The ADuCM355 includes three general-purpose timers, a wake-up timer (which can be used as a general-purpose timer), and a system watchdog timer.

The analog subsystem has a separate 16 MHz oscillator used to clock the ADC, DACs, and other digital logic on the analog die. The analog die also contains a separate 32 kHz, low power oscillator to clock a watchdog timer on the low voltage die. Both the 32 kHz oscillator and this watchdog are independent from the digital die oscillators and system watchdog timer.

A range of communication peripherals can be configured as required in a specific application. These peripherals include UART, I^2C, 2xSPI, and GPIO ports. The GPIO, combined with the general-purpose timers, can be combined to generate a pulse width modulation (PWM) type output.

On-chip factory firmware supports in-circuit erasing of user flash triggered via the UART, while nonintrusive emulation and program download are supported via the serial wire debug port (SW-DP) interface.

The ADuCM355 operates from 2.8 V to 3.6 V supply and is specified over a temperature range of −40°C to +85°C. The chip is packaged in a 72-lead 6 mm × 5 mm land grid array (LGA) package.

FUNCTIONAL BLOCK DIAGRAM

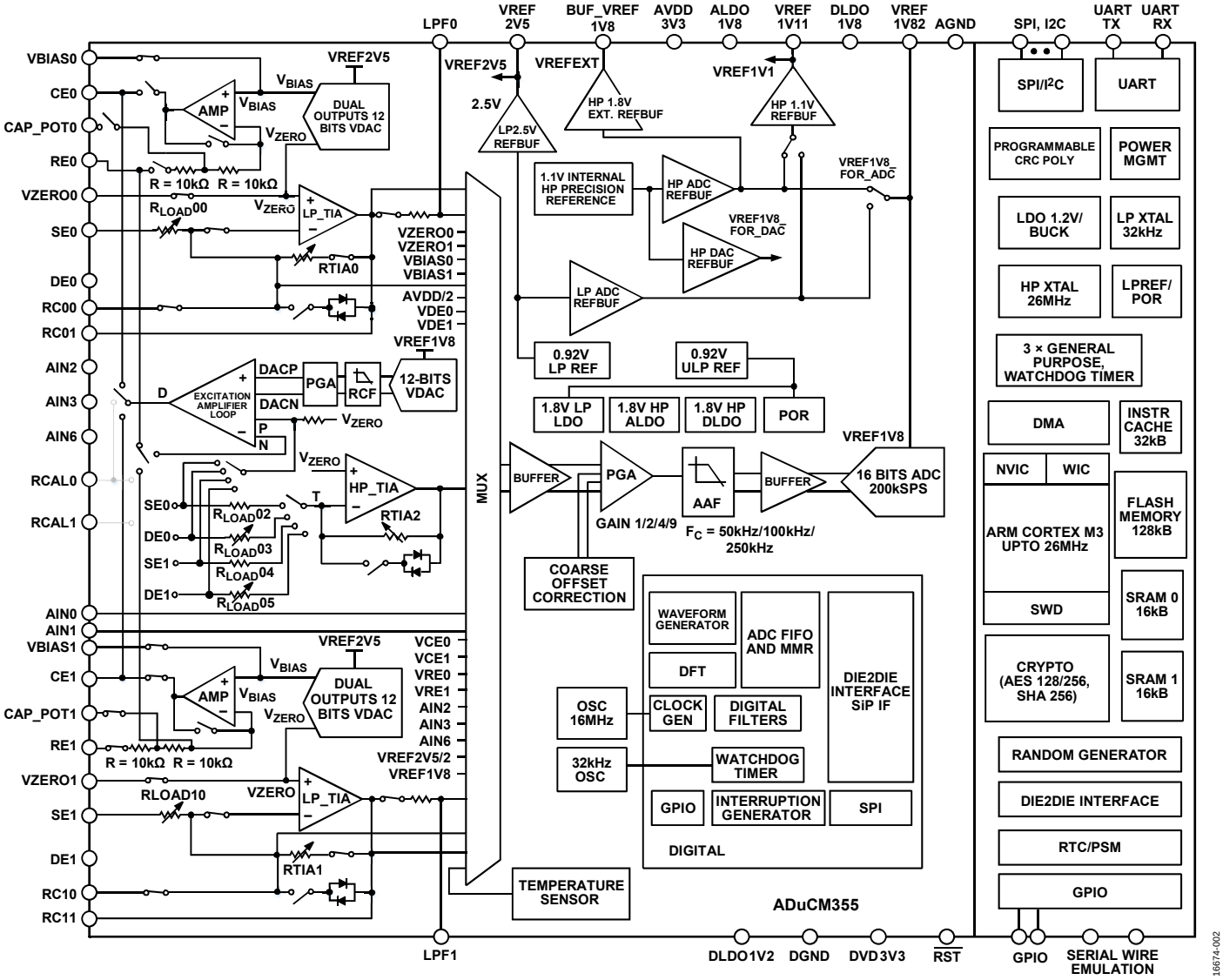

Figure 2.

SPECIFICATIONS

MICROCONTROLLER ELECTRICAL SPECIFICATIONS

AVDD = DVDD = 2.8 V to 3.6 V, maximum difference between supplies = 0.3 V, ADC reference and excitation DAC and amplifier = 1.82 V internal reference, low power VBIAS and VZERO DAC reference = 2.5 V internal reference, f_{CORE} = 26 MHz, T_A = −40°C to +85°C, buck convertor on digital die disabled, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADC SPECIFICATIONS						Pseudo differential mode measured relative to ADCVBIAS_CAP, unless otherwise stated; specs based on high speed mode, unless otherwise stated; ADC voltage channel calibrated in production with PGA gain = 1.5; AFE die ACLK = 32 MHz or 16 MHz, unless otherwise stated
Data Rate[1]	f_{SAMPLE}			400	kSPS	High speed mode, decimation factor of 4
	f_{SAMPLE}			200	kSPS	Normal mode, decimation factor of 4
Resolution[1]		16			Bits	Number of data bits
Integral Nonlinearity[1]	INL	−4	±2.0	+3.5	LSB	PGA Gain = 1.5, 1.82 V internal reference 1 LSB = 1.82 V/2^{15}
		−5.6	±2.0	+4.7	LSB	PGA Gain = 9, 1.82 V internal reference
			±2.0		LSB	1.82 V external reference; 1 LSB = 1.82 V/2^{15}
Differential Nonlinearity, (No Missing Codes)[1]	DNL	−0.99	±0.9	+2.5	LSB	1.82 V internal reference; 1 LSB = 1.82 V/2^{15}
DC Code Distribution[2]			±6		LSB	PGA gain = 1.5, low power (LP) mode, ADC input 0.9 V; ADC output data rate = 200 kSPS, 1 LSB = 1.82 V/2^{15}
			±6		LSB	Input channel is LPTIA0 = 1 µA, RTIA = 512 KΩ, RLOAD = 10 Ω, ADC output data rate = 200 kSPS
			±6		LSB	Input channel is high speed TIA (HPTIA) = 1 µA, RTIA = 10 KΩ, RLOAD = 100 Ω, ADC output data rate = 200 kSPS
ADC ENDPOINT ERRORS						For AIN0 to AIN7 inputs; 200 kSPS ADC update rate; SINC3 filter enabled
Offset Error		−600	±200	+600	µV	PGA gain = 1.5, LP mode, all channels except AIN3
		−620	±200	+880	µV	PGA gain = 1.5, LP mode, AIN3 only
High Power (HP) Mode[3]		−1.1	±0.5	+1.4	mV	PGA gain = 1.5, HP mode
Drift[1]			±3		µV/°C	Using 1.82 V internal reference
Offset Matching			±1		LSB	Matching compared to AIN3
Full Scale Error		−750	±400	+940	µV	Excluding internal channels; both negative and positive full scale; error at both end points. PGA gain = 1.5, LP mode
HP Mode[4]		−1.6	±0.8	+1.82	mV	PGA gain = 1.5, HP mode
			0.1[1]	0.75[1]	% of Full Scale	AVDD/2, DVDD/2, ADCVBIAS_CAP, VREF_2.5V, VREF_1.8V, AVDD_REG
Gain Drift[1]		−3	±1	+3	µV/°C	Full scale error drift minus offset error drift
Gain Error Matching			±1.5		LSB	Mismatch from channel to channel
PGA Mismatch Error[1]						ADC offset and gain calibration with gain = 1.5
PGA Gain of 1 to Gain of 1.5		−0.2	+0.1	+0.3	%	
PGA Gain of 1.5 to Gain of 2		−0.2	+0.1	+0.3	%	
PGA Gain of 2 to Gain of 4		−0.3	+0.2	+0.8	%	
PGA Gain of 4 to Gain of 9		−0.55	+0.2	+0.55	%	
PGA Gain Mismatch Drift			1.5		µV/°C	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADC DYNAMIC PERFORMANCE						f_{IN} = 20 KHz sine wave, f_{SAMPLE} = 200 kSPS; using AINx voltage input channels; PGA gain = 1.5x
Signal-to-Noise Ratio	SNR					Includes distortion and noise components
			80		dB	PGA Gain = 1, 1.5 and 2
			76		dB	PGA Gain = 4
			70		dB	PGA Gain = 9
Total Harmonic Distortion[1]	THD		−84		dB	
Peak Harmonic or Spurious Noise[1]			−86		dB	
Channel-To-Channel Crosstalk[1]			−86		dB	Measured on adjacent channels
Noise (RMS)[1, 5]						0.1 Hz to 10 Hz. ADC update rate = 200 kSPS
			78		µV	PGA Gain = 1,
			55		µV	PGA Gain = 1.5
			42		µV	PGA Gain = 2
			26		µV	PGA Gain = 4
			19		µV	PGA Gain = 9
			800		nV/rt-Hz	Chop off
			400		nV/rt-Hz	Chop on
ADC INPUT						Input to ADC mux
Input Voltage Ranges[1]		0.2		2.1	V	Voltage applied to any input pin
						Pseudo differential voltage between ADCVBIAS_CAP and analog input from mux
		−0.9		+0.9	V	Gain = 1
		−0.9		+0.9	V	Gain = 1.5
		−0.6		+0.6	V	Gain = 2
		−0.3		+0.3	V	Gain = 4
		−0.133		+0.133	V	Gain = 9
Common Mode Range[1]		0.2	1.1	2.1	V	
Leakage Current		−1.5	± 0.5	+1.5	nA	AIN0 to AIN7_LPF1, SE0, SE1, and DE0 pins
Input Current[1]		−8	±2	+8	nA	AIN0 to AIN7_LPF1, SE0, SE1, and DE0 pins
Input Capacitance			40		pF	During ADC acquisition
AAF, 3 dB Frequency Range						3 programmable settings
Mode 0			50		kHz	
Mode 1			100		kHz	
Mode 2			250		kHz	
ADC Channel Switch Settling Time						Time delay required after switching ADC input channel, excludes SINC3 settling time
AAF, 3 dB Cut Off Frequency 250 kHz[1]		20			µs	
AAF, 3 dB Cut Off Frequency 100 kHz[1]		40			µs	
AAF, 3 dB Cut Off Frequency 50 kHz[1]		50			µs	
SINC3 Bypassed		20			µs	800 kSPS ADC output rate

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DFT-BASED IMPEDANCE MEASUREMENTS						For Z of 100 Ω (0.02% tolerant resistor), excitation frequency = 0.5 to 200 kHz, sine amplitude = 9 mV rms, RTIA = 5 kΩ; T_A = 25°C; R_{CAL} = 200 Ω;1% accurate tempco 5 ppm/°C; single DFT measurement; DFT using 8192 ADC samples; Hanning on; DACCON [8:1] = 0x1B for LP mode and impedance measurements ≤80 kHz; DACCON [8:1] = 0x7 for HP mode and impedance measurements > 80 kHz
Frequency Range[1]		0.5		200	kHz	
Accuracy						Device to device repeatability for 1000 devices
Magnitude			2		%	Standard deviation as a percent of Z
			8		%	1 Hz
			3.5		%	10 Hz
Phase			6		Degrees	Standard deviation of Z
Precision						
Magnitude			1		%	Standard deviation as a percent of Z
Phase			3		Degrees	Standard deviation of Z
LOW POWER TIA AND POTENTIOSTAT AMPLIFIERS						
Input Bias Current			80	300	pA	TIA, SE pin
Input Bias Current			20	150	pA	Potentiostat amplifiers, RE pin
Offset Voltage			50	150	µV	
Offset Voltage Drift vs. Temperature			1		µV/°C	
Noise						Unity gain mode; RMS voltage in 0.1 Hz to 10 Hz range
			1.6		µV (RMS)	Normal mode (LPTIACONx [2] = 0)
			2		µV (RMS)	Half Power mode (LPTIACONx [2] = 1)
Potentiostat Source/Sink Current[1]		−750		+750	µA	Normal mode (LPTIACONx [4:3] = 00); from CEx pins
Potentiostat Source/Sink Current[1]		−3		+3	mA	High current mode (ULPTIACONx [4:3] = $01/11_b$); from CEx pins
DC Power Supply Rejection Ratio			70		dB	At REx pin; RTIA = 256 KΩ, RLOAD = 10 Ω
Input Common Mode Range[1]		300		AVDD-600	mV	
Output Voltage Range[1]						
		300		AVDD-400	mV	Normal mode (ULPTIACONx [4:3] = 00_b), sink/source 750 µA
		300		AVDD-400	mV	High current mode (ULPTIACONx [4:3] = 01/11), sink/source 3 mA
Overcurrent Limit Protection			17		mA	Amplifiers will try to limit source/sink current to this value via internal clamp
Allowed Duration of Overcurrent Limit[1]				5	sec	User must limit duration of overcurrent condition to less than this or risk damaging amplifier
Allowed Frequency of Overcurrent Conditions				1	Per hour	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PROGRAMMABLE RESISTORS						
LPTIA RLOAD on SE0, SE1 Inputs[1]						
Drift over Temperature			±200		ppm/°C	10 Ω, 30 Ω, 100 Ω, 1500 Ω, 3000 Ω, 3500 Ω
			±400		ppm/°C	50 Ω
0 Ω RLOAD Accuracy		0.01	0.08	0.15	Ω	
10 Ω RLOAD Accuracy		9.8	11.7	13.5	Ω	
30 Ω RLOAD Accuracy		28	33.8	39	Ω	
50 Ω RLOAD Accuracy		48	55	63	Ω	
100 Ω RLOAD Accuracy		88	110	130	Ω	
LPTIA RTIA Gain on SE0, SE1 Inputs[1]						
Accuracy		−5		+15	% (TBC)	User programmable, includes 1 KΩ, 2 KΩ, 3 KΩ, 4 KΩ, 6 KΩ, 8 KΩ, 10 KΩ, 16 KΩ, 20 KΩ, 22 KΩ, 30 KΩ, 40 KΩ, 64 KΩ, 100 KΩ, 128 KΩ, 160 KΩ, 192 KΩ, 256 KΩ, 512 KΩ
		115	120	130	Ω	200 Ω setting with Rload = 100 Ω
Drift over Temperature			±100		ppm/°C	
LPTIA RTIA Mismatch Error[1]						Error when moving up or down one RTIA value
		−0.6	+0.2	+0.6	%	512 KΩ to 2 KΩ range excluding 40 KΩ
		−3.5	+0.5	+3.5	%	40 KΩ (up to 48 KΩ, down to 32 KΩ)
			±20		%	200 Ω
HPTIA RLOAD on SE0, SE1 Inputs[1]						
Accuracy		102	110	116	Ω	Fixed 100 Ω target setting
Drift			±160		ppm/°C	
HPTIA RTIA Gain on SE0, SE1[1] Inputs						RTIA02 and RTIA04
Accuracy			±20		%	User programmable, includes 0.2 KΩ, 1 KΩ, 5 KΩ, 10 KΩ, 20 KΩ, 40 KΩ, 80 KΩ, 160 KΩ
Drift			±200		ppm/°C	
HPTIA RLOAD on DE0, DE1 Inputs[1]						RLOAD03 and RLOAD05
Accuracy		0.001		0.15	Ω	0 Ω setting
		5		10.7	Ω	10 Ω setting
		26.5	32.6	37.6	Ω	30 Ω setting
			±15	+25	%	30 Ω, 50 Ω,and 100 Ω settings
Drift over Temperature			±0.2		%/°C	10 Ω setting
			±200		ppm/°C	Excludes RLOAD = 0 Ω and 10 Ω
HPTIA RTIA Gain on DE0, DE1 Inputs[1]						User programmable, includes 0.1 KΩ, 0.2 KΩ, 1 KΩ, 5 KΩ, 10 KΩ, 20 KΩ, 40 KΩ, 80 KΩ, 160 KΩ
Accuracy		120	135	150	Ω	100 Ω setting
		230	250	280	Ω	200 Ω setting
			±20		%	1 KΩ, 5 KΩ, 10 KΩ, 20 KΩ, 40 KΩ, 80 KΩ, 160 KΩ
Drift over Temperature			±350		ppm/°C	100 Ω, 200 Ω settings
			±200		ppm/°C	1 KΩ, 5 KΩ, 10 KΩ, 20 KΩ, 40 KΩ, 80 KΩ, 160 KΩ
HPTIA RTIA Mismatch Error SE0/SE1/DE0/DE1[1]						Error introduced when moving up or down one RTIA value
		−3.5	+1	+3.5	%	160 KΩ to 5 KΩ range
		−2.5	±2	+5	%	1 KΩ, 200 Ω, and 100 Ω

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
HIGH POWER TIA AMPLIFIER						
Bias Current			1		nA	
Maximum Current Sink/Source[1]		−3		+3	mA	Ensure RTIA selection generates output voltage of less than ±900 mV with PGA gain = 1
Input Common Mode Range[1]		300		AVDD − 700	mV	
Output Voltage Range[1]		200		AVDD − 400	mV	
Overcurrent Limit Protection[1]			17		mA	Amplifier will try to limit source/sink current to this value via internal clamp; tested with RLOAD = 0 Ω, RTIA = 100 Ω
Allowed Duration of Overcurrent Limit[1]				5	sec	
Allowed Frequency of Overcurrent Conditions[1]				1	Per hour	
LOW POWER ON-CHIP VOLTAGE REFERENCE			2.5		V	0.47 µF from VREF_2.5 V to AGND; reference is measured with all low power VDACs and output amplifiers enabled
Accuracy				±5	mV	TA = 25°C
Noise[1]			60		µV (pk-pk)	Pk-pk voltage in 0.1 Hz to 10 Hz range
Reference Temperature Coefficient[1,6]		−25	±10	+25	ppm/°C	
DC Power Supply Rejection Ratio	PSRR		70		dB	Dc variation due to AVDD supply changes
AC Power Supply Rejection Ratio[7]	PSRR		48		dB	Ac 1 kHz, 50 mV pk-pk ripple applied to AVDD supply
HIGH POWER ON-CHIP VOLTAGE REFERENCE			1.82		V	4.7 µF from VREF_1.82V to AGND; reference is measured with ADC enabled
Accuracy				±5	mV	TA = 25°C
Reference Temperature Coefficient[1,2]		−20	±5	+20	ppm/°C	
DC Power Supply Rejection Ratio	PSRR		85		dB	DC variation due to AVDD supply changes
AC Power Supply Rejection Ratio[8]	PSRR		52		dB	AC 1 kHz, 50 mV pk-pk ripple applied to AVDD supply
ADC Common Mode Reference Source			1.11		V	470 nF from ADCVBIAS_CAP to AGND; reference is measured with ADC enabled
Accuracy				±5	mV	TA = 25°C
Reference Temperature Coefficient[1]		−20		+20	ppm/°C	
DC Power Supply Rejection Ratio	PSRR		80		dB	DC variation due to AVDD supply changes
AC Power Supply Rejection Ratio	PSRR		50		dB	AC 1 kHz, 50 mV pk-pk ripple applied to AVDD supply
BUFFERED REFERENCE VOLTAGE OUTPUT			1.82		V	
Accuracy				±5	mV	TA = 25°C; capacitive load to GND 100 pF
Reference Temperature Coefficient[1,6]		−20		+20	ppm/°C	
Output Impedance			0.5	1	Ω	
Load Current[1]				200	µA	
LOW POWER DAC SPECIFICATIONS (VBIASx/VZEROx)						VBIAS specifications derived from measurements taken with potentiostat amplifier in unity gain mode and measured at CE0/CE1 pins; VZERO specifications derived from measurements at VZERO0/VZERO1 pins; dual output low power DACs
Resolution[1]		12			Bits	12-bit mode, number of data bits
		6			Bits	6-bit mode, number of data bits
Relative Accuracy[1,9], 12-Bit Mode	INL	−6.5	±1	+3	LSB	1 LSB = 2.2 V/(2^{12} − 1)
Relative Accuracy[1,10], 6-Bit Mode	INL	−2.5	±0.1	+2	LSB	1 LSB = 2.2 V/2^6

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Differential Nonlinearity[9]	DNL	−0.99		+2.5	LSB	12-bit mode, guaranteed monotonic, 1 LSB = 2.2 V/(2^{12} − 1)
	DNL	−0.5		+0.5	LSB	6-bit mode, guaranteed monotonic, 1 LSB = 2.2 V/2^6
Offset Error[1]			±1	±7	mV	VBIASx/VZER0x in 12-bit mode, 2.5 V internal reference, DAC Output Code 0x000; target 0x000 code is 200 mV
		−1	±0.2	1	mV	Differential offset voltage of VBIAS referred to VZERO; LPDACDATx = 0x00000
Drift			±5		µV/°C	VBIASx or VZER0x referred to AGND, using internal low power reference
Differential Offset VBIAS to VZERO ≈ 0 V[1]				4	µV/°C	Differential offset voltage of VBIAS referred to VZERO, −40°C to +60°C range; LPDACDATx = 0x1A680
Differential offset VBIAS to VZERO ≈ ±600 mV[1]				10	µV/°C	Differential offset voltage of VBIAS referred to VZERO, −40°C to +60°C range; LPDACDATx = 0x1AAE0
Gain Error[1]			±0.2	±0.5	%	12-bit mode, DAC code = 0xFFF with target voltage of 2.4 V; no correction for internal 2.5 V reference drift
Drift			10		ppm/°C	Using internal low power reference
Mismatch			±0.1		%	% of full scale on VBIAS0 to VBIAS1 in 12-bit mode
Analog Outputs						
Output Voltage Range[1]						LSB size is 2.2/(2^{12} − 1); note input common mode voltage of LP potentiostat and LPTIA is AVDD − 600 mV
12-Bit Outputs		0.2		2.4	V	AVDD ≥2.8 V
		0.2		2.3	V	AVDD <2.8 V; LPDACDATx[11:0] = 0xF40
						LSB size is 2.2/2^6; note input common mode voltage of LP potentiostat and LPTIA is AVDD − 600 mV
6-Bit Outputs		0.2		2.366	V	AVDD ≥2.8 V
		0.2		2.3	V	AVDD <2.8 V; LPDACDATx[17:12] = 0x3D
AVDD to VBIAS/VZERO Headroom Voltage[1]		400			mV	A minimum headroom between AVDD and VBIAS/VZERO output voltage, increases to 600 mV if connected to LPTIA or LP potentiostat amplifiers
Output Impedance[1]			1.65		MΩ	
DAC AC Characteristics						
Output Settling Time			1.5		sec	Settled to ±2 LSB_{12} for ¼ of full scale to ¾ of full scale; with 1 kΩ load on amplifier output, 0.1 µF capacitors connected to VBIASx/VZEROx pins, LPTIASWx[13:12] = 11
Output Settling Time			500		µS	Settled to ±2 LSB_{12} for ¼ of full scale to ¾ of full scale; with 1 kΩ load on amplifier output, capacitors on VBIASx/VZEROx disconnected, LPTIASWx[13:12] = 00
Glitch Energy			±5		nV-sec	1 LSB change when the maximum number of bits changes simultaneously in the LPDACDATx register. Switch to external capacitors on VBIASx/VZEROx opened. No capacitors on CEx/RCx_1 pins.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
EXCITATION DAC/PGA/ RECONSTRUCTION FILTER SPECIFICATIONS						Use HSDACDAT range 0x200 to 0xE00, specified for gain = 2 (HSDACCON[12], HSDACCON[0] = 0) and gain =0.05, (HSDACCON[12], HSDACCON[0] = 1)
DAC						
Common Mode Voltage Range[1]		0.2		AVDD-0.6	V	Set by excitation amplifiers N node
Resolution[1]		12			Bits	
Differential Nonlinearity[9]						
	DNL			+1/−0.99	LSB	Guaranteed monotonic, gain = 2
	DNL		±7	±14	LSB	gain = 0.05
Relative Accuracy[1,9]						
	INL		±2	±3	LSB	Gain = 2
	INL		±8	±18	LSB	Gain = 0.05
Full Scale Error[11]						
Positive		595	607	620	mV	Gain = 2, DAC code = 0xE00
		14	15.1	16	mV	Gain = 0.05, DAC code = 0xE00
Negative		−620	+607	−595	mV	Gain = 2, DAC code = 0x200
		−16	−15.1	−14	mV	Gain = 0.05, DAC code = 0x200
Gain Error Drift						
Gain = 2			11.5		µV/°C	
Gain = 0.05			0.33		µV/°C	
Offset Error (Midscale)						Measured at an output of the excitation loop across RCAL, DAC code = 0x800
			±1	±5	mV	Gain = 2
			±0.2	±0.9	mV	Gain = 0.05
Offset Error Drift						
Gain = 2			TBD		µV/°C	
Gain = 0.05			5		µV/°C	
DC Power Supply Rejection Ratio	PSRR		70		dB	DC variation due to AVDD supply changes
PGA Programmable Gain		0.05		2		
Reconstruction Filter						
3 dB Corner Frequency Accuracy			±5		%	Programmable 50 kHz, 100 kHz, and 250 KHz
Allowed External Load Capacitance[1]						SEx/DEx/AINx/RCALx pins
<80 KHz (Low Power Mode)				30	pF	
>80 KHz (High Power Mode)				30	pF	
Overcurrent Limit Protection[1]			5		mA	Amplifier tries to limit source/sink current to this value via internal clamp
Allowed Duration of Overcurrent Limit[1]				5	sec	
Allowed Frequency of Overcurrent Conditions[1]				1	Per hour	
SWITCH MATRIX SPECIFICATIONS						Switches on AFE before ADC mux
RON[1]						Characterized with a voltage sweep from 0 V to V_{CM}; production tested at 1.8 V
Current Carrying Switches			40	80	Ω	T switches, except T5 and T7
			30	52	Ω	T switches, T5 and T7 only
			35	70	Ω	D Switches
Non-Current Carrying Switches			1	5	KΩ	P and N switches
DC OFF Leakage			370		pA	Analog input pin used for test driven to 0.2 V
DC ON Leakage[1]			530	2000	pA	Analog input pin used for test driven to 0.2 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR						TEMPSENS = 0x2
Resolution			0.3		°C	
Accuracy			±2		°C	Measurement taken immediately after exiting hibernate mode, user single point calibration required
Life Time Drift			TBD		°C	500 hour drift test at 85°C
POWER-ON RESET	POR					Refers to voltage on DVDD pin
POR Trip Level[12]		1.59	1.62	1.67	V	Power-on level
		1.799	1.8	1.801	V	Power-down level
POR Hysteresis[1]			10		mV	
Power Up Timings[1]						
Delay Between POR Power-On and Power-Down Trip Levels		110			ms	After DVDD passes POR power-on trip level, DVDD must remain at or above power down level for this period
Total Power Time for All Supplies				20	ms	All supplies must be above maximum POR trip, power-on trip level in this period
EXTERNAL RESET						
External Reset Minimum Pulse Width[1]		1			µs	Minimum pulse width required on external reset pin to trigger a reset sequence
WATCHDOG TIMERS	WDT					Timer on analog and digital die
Timeout Period[1]			32		sec	Default at power-up, analog die watchdog
FLASH/EE MEMORY						
Endurance		10,000			Cycles	
Data Retention		10			Years	T_J = 85°C
DIGITAL INPUTS						
Input Leakage Current[1]						
Logic 1 GPIO			1	±5	nA	$V_{IH} = V_{DD}$, pull-up resistor disabled
Logic 0 GPIO			1	±10	nA	V_{IL} = 0 V, pull-up resistor disabled
Input Capacitance			10		pF	
Pin Capacitance						
XTALI			10		pF	
XTALO			10		pF	
LOGIC INPUTS						
GPIO Input Voltage						
Low	V_{INL}			0.25 × IOVDD	V	
High	V_{INH}	0.57 × IOVDD			V	
Pull-Up Current[1]		30		130	µA	V_{IN} = 0 V; DVDD = 3.6 V
LOGIC OUTPUTS						All digital outputs excluding XTALO
GPIO Output Voltage[13]						
High	V_{OH}	IOVDD – 0.4			V	I_{SOURCE} = 2 mA
Low	V_{OL}			0.3	V	I_{SINK} = 2 mA
GPIO Short-Circuit Current			11.5		mA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OSCILLATORS						
Internal System Oscillator			26		MHz	Digital die
Accuracy			±1	±3.2	%	26 MHz output mode
System PLL			26		MHz	Main system clock
Internal System Oscillator			16 or 32		MHz	Analog die
Accuracy for 16 MHz Mode			±0.5	±2	%	
Accuracy for 32 MHz Mode			±0.5	±2	%	
Switching Time[1]		4			µs	Time delay required after switching system clock source from 16 MHz or 32 MHz oscillator before accessing AFE die
External Crystal Oscillator			16	32	MHz	Can be selected in place of internal oscillator
Leakage			500	540	nA	XTALI/XTAO pins
Logic Inputs, XTALI Only						
Input Low Voltage (V_{INL})			1.1		V	
Input High Voltage (V_{INH})			1.7		V	
32 kHz Internal Oscillators			32.768		kHz	Used for watchdog timers and wake-up timers
Accuracy			±3	±6	%	Digital die LF oscillator
			±5	±15	%	Analog die LF oscillator
START-UP TIME						Processor clock = 16 MHz
At Power-On			85	120	ms	POR to first user code execution
After Other Reset			50		ms	Reset to first user code execution, includes watchdog, external, and software resets
Digital Die Wake-Up			10	30	µs	
Analog Die Wake-Up[1]			50	85	µs	Wake-up time to allow communication with AFE die
ADC Wake-Up[1]			90	110	µs	Time delay required on exiting hibernate or shutdown mode before starting ADC conversions if 1.8 V ADC reference capacitor voltage is maintained
EXTERNAL INTERRUPTS						
Pulse Width						
Level Triggered[1]		7			ns	
Edge Triggered[1]		1			ns	
POWER REQUIREMENTS[14]						
Power Supply Voltage Range						
AVDD to AGND, DVDD to DGND, DVDD_AD to DGND_AD		2.8	3.3	3.6	V	
Active Mode			4.75	5.2	mA	Default current after a reset, AFE and digital die in active mode
Flexi Mode			3.8	4.2	mA	Cortex-M3 disabled, DMA and other peripherals active
Hibernate Mode			3		µA	32 kHz oscillator active, 64 kB SRAM retained state supported on digital die
Shutdown Mode[1]			2		µA	Lowest power mode, only wake-up controller active
Additional Power Supply Currents						
ADC Circuits			0.75	0.8	mA	fADC = 200 kSPS
			1.1	1.2	mA	fADC = 400 kSPS
High Power TIA			0.3	0.42	mA	LP & HP mode
Low Power Reference			1.65		µA	
Low Power DACs for VZERO and VBIAS			2.3		µA	Per powered up DAC, excluding load current

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Standby Mode						Potentiostat amplifier and low power DACs enabled with both 32 kHz oscillators; 64 KB of SRAM state retained; all other peripherals in hibernate mode (−40°C to +60°C)
			8.5	17.5	µA	Single sensor/potentiostat channel, −40°C to +60°C
				40	µA	Single sensor/potentiostat channel, −40°C to +85°C
			7	14	µA	PA and LPTIA0 in half power mode, −40°C to +60°C
				25	µA	PA and LPTIA0 in half power mode, −40°C to +85°C
			16		µA	Both potentiostat channels on
DC Measurement Mode			4.5	5.5	mA	System clock 4 MHz; ADC, LP mode (−40°C to +60°C)
				6.6		−40°C to +85°C
Impedance Spectroscopy Mode[1]			8.5	10.2	mA	When AC impedance engine (80 kHz) and ADC are active in LP mode, micro also active with 26 MHz clock (−40°C to +85°C)
			13.7	17.8	mA	When AC impedance engine (200 kHz) and ADC are active in HP mode micro also active with 26 MHz clock. (−40°C to +85°C)
Thermal Performance						
Impedance Junction to Ambient			45		°C/W	JEDEC 2S2P

[1] Guaranteed by design, but not production tested.
[2] Code distribution can be reduced if ADC output rate is reduced by using SINC2 filter option.
[3] ADC offset and gain not calibrated for HP mode in production. User calibration can eliminate this error.
[4] ADC offset and gain not calibrated for HP mode in production. User calibration can eliminate this error.
[5] Noise can be reduced if ADC output rate is reduced by using SINC2 filter option.
[6] Measured using the box method.
[7] See Figure 9 for more details.
[8] See Figure 8 for more details.
[9] DAC linearity is calculated using a reduced code range of 0x10 lower limit to 0xF40 upper limit.
[10] The average current from all GPIO pins must not exceed 20 mA per pin.
[11] HSDAC offset calibration can remove this error. See the ADuCM355 Hardware Reference Manual for more details.
[12] It is recommended that the user enables power supply monitoring features to ensure operation only when DVDD or AVDD above 2.8 V.
[13] DAC gain error is calculated using a reduced code range of 100 to an internal 2.5 V V_{REF}.
[14] Power figures exclude load currents from external circuits.

RMS NOISE RESOLUTION OF ADC

The RMS noise specifications for the ADC with different ADC digital filter settings is detailed in Table 2. The internal 1.82 V reference was used for all measurements. Table 3 shows the RMS and pk-pk effective number of bits (ENOB) based on the noise results in Table 2 for various PGA gain settings. Pk-pk ENOB results are shown in parentheses. RMS bits are calculated as follows:

$$\log_2\left(\frac{2\times Input\ Range}{RMS\ Noise}\right)$$

Pk-pk bits are calculated as follows:

$$\log_2\left(\frac{2\times Input\ Range}{6.6\times RMS\ Noise}\right)$$

Table 2. ADC RMS Noise

Update Rate (Hz)	SINC3 Oversampling Rate	SINC2 Oversampling Rate	Gain = 1 RMS Noise (µV)	Gain = 1.5 RMS Noise (µV)	Gain = 2 RMS Noise (µV)	Gain = 4 RMS Noise (µV)	Gain = 9 RMS Noise (µV)
200000	4	NA	72.43	49.732	37.83	18.93	8.62
9090	4	22	29.29	19.59	10.4	6.687	4.42
900	5	178	24.0	17.11	12.832	6.416	1.018

Table 3. ADC ENOB Based on RMS Noise

Update Rate (Hz)	Sinc3 OSR	SINC2 OSR	Gain = 1	Gain = 1.5	Gain = 2	Gain = 4	Gain = 9
200000	4	NA	14.6 (11.9 p-p)	15 (12.4 p-p)	14.95 (12.23 p-p)	14.95 (12.23 p-p)	14.9 (12.15 p-p)
9090	4	22	15 (13.18 p-p)	15 (13.8 p-p)	15 (14.09 p-p)	15 (13.73 p-p)	15 (13.15 p-p)
900	5	178	15 (13.47 p-p)	15 (13.96 p-p)	15 (13.8 p-p)	15 (13.79 p-p)	15 (15 p-p)

TIMING SPECIFICATIONS

Table 4. SPI Master Mode Timing

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Timing requirements						Characterized with respect to double drive strength.
CS to SCLK Edge	t_{CS}	0.5 x t_{PCLK} – 3			ns	
SCLK low pulse width	t_{SL}	t_{PCLK} – 3.5			ns	
SCLK high pulse width	t_{SH}	t_{PCLK} – 3.5			ns	
Data input setup time before SCLK edge	t_{DSU}	5			ns	
Data input hold time after SCLK edge	t_{DHD}	20			ns	
Switching characteristics						
Data output valid after SCLK edge	t_{DAV}		25		ns	
Data output setup before SCLK edge	T_{DOSU}	t_{PCLK} – 2.2			ns	
CS high after SCLK Edge	t_{SFS}	0.5 x t_{PCLK} – 3			ns	

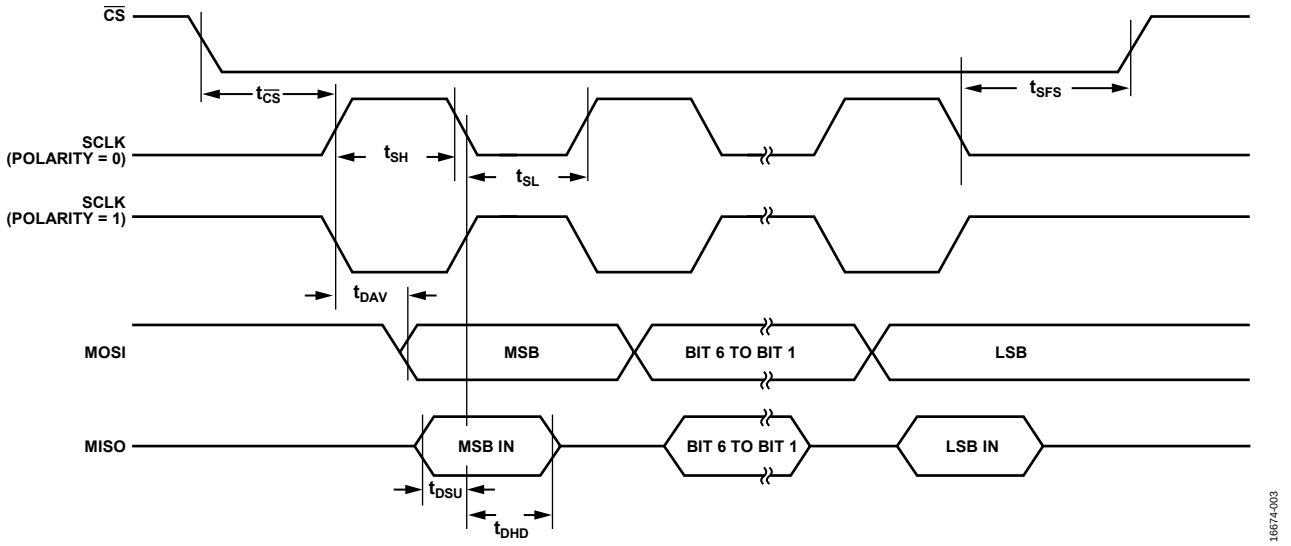

Figure 3. SPI Master Timings (Phase Mode = 1)

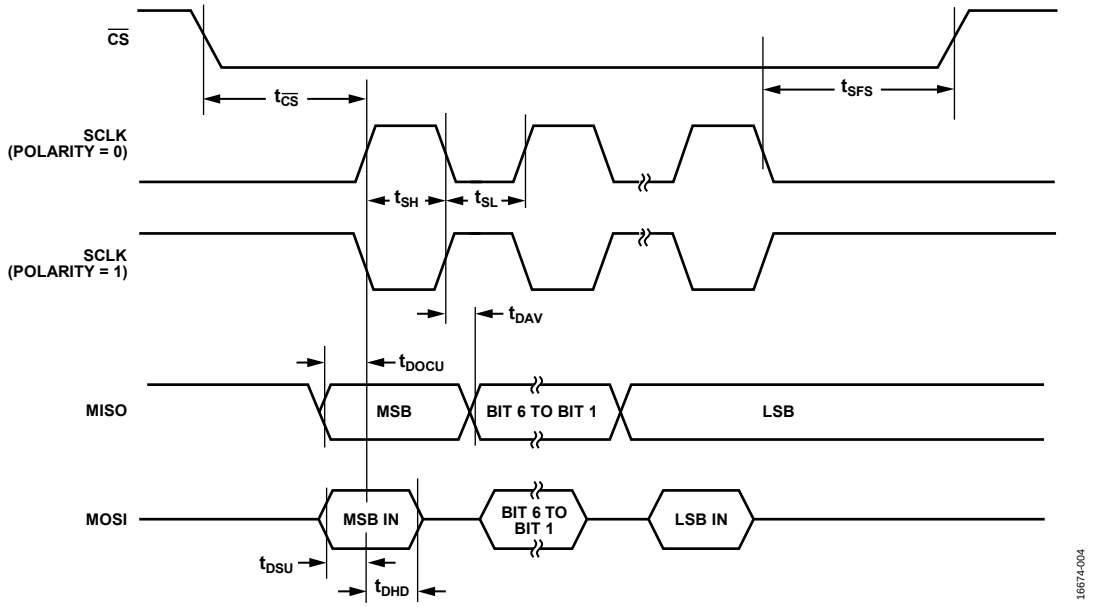

Figure 4. SPI Master Timings (Phase Mode = 0)

Table 5. SPI Slave Mode Timing

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Timing requirements						Characterized with respect to double drive strength
CS to SCLK Edge	t_{CS}	38.5			ns	
SCLK low pulse width	t_{SL}	38.5			ns	
SCLK high pulse width	t_{SH}	38.5			ns	
Data input setup time before SCLK edge	t_{DSU}	6			ns	
Data input hold time after SCLK edge	t_{DHD}	8			ns	
Switching characteristics						
Data output valid after SCLK edge	t_{DAV}	25			ns	
Data output valid after CS edge	T_{DOCS}	38.5			ns	
CS high after SCLK Edge	t_{SFS}	38.5			ns	

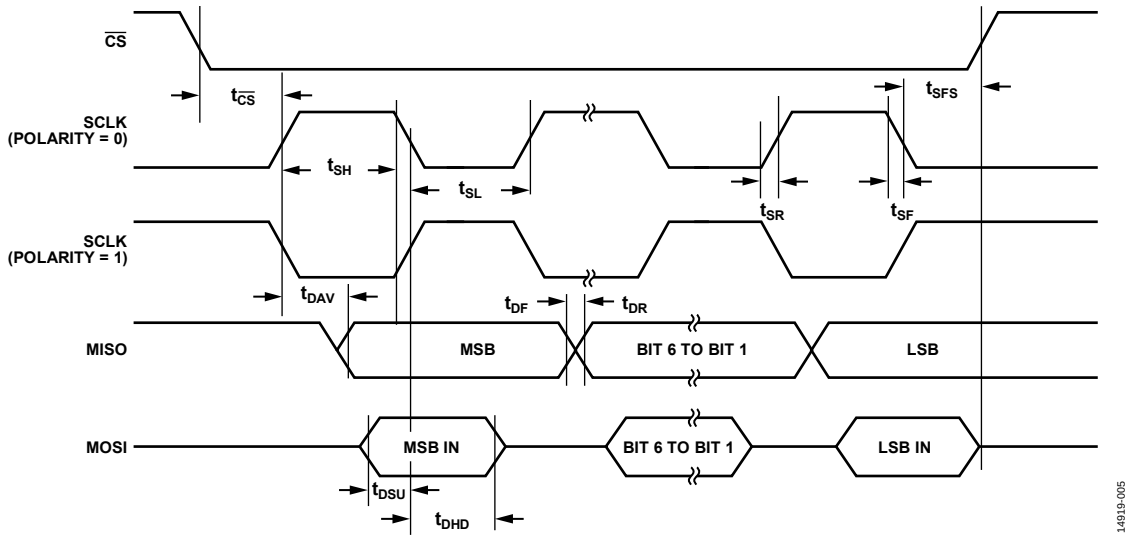

Figure 5. SPI Slave Timings (Phase Mode = 1)

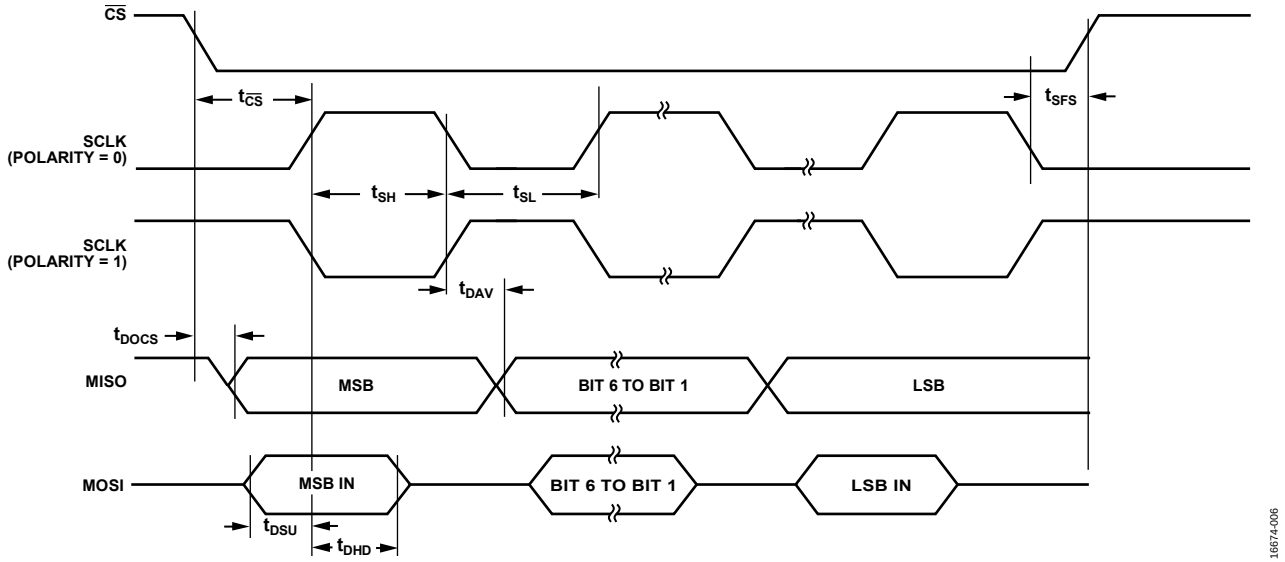

Figure 6. SPI Slave Timings (Phase Mode = 0)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to AGND	−0.3 V to +3.6 V
DVDD to DGND	−0.3 V to +3.6 V
AVDD to DVDD	DVDD ±0.3 V
DVDD_AD to DGND_AD	−0.3 V to +3.6 V
Analog Input Voltage to AGND (AVDD Range is 2.8 V to 3.6 V)	−0.3 V to AVDD +0.3V; must be ≤3.6 V
Digital Input Voltage to DGND (DVDD Range is 2.8 V to 3.6 V)	−0.3 V to DVDD +0.3 V; must be ≤3.6 V
Digital Output Voltage to DGND (DVDD Range is 2.8 V to 3.6 V)	−0.3 V to DVDD +0.3 V; must be ≤3.6 V
AGND to DGND	−0.3 V to +0.3 V
DGND_AD to AGND	−0.3 V to +0.3 V
Total Positive GPIO Pins Current	0 mA to 30 mA
Total Negative GPIO Pins Current	−30 mA to 0 mA
Storage Temperature Range	−65°C to 150°C
Operating Temperature Range	−40°C to 85°C
Reflow Profile	
SnPb Assemblies (10 sec to 30 sec)	240°C
Pb-Free Assemblies (20 sec to 40 sec)	260°C
Junction Temperature	150°C max
Electrostatic Discharge (ESD)	
Human Body Model	2 kV
Field-Induced Charged Device Model	1 kV
Machine Model	100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
72-LGA[1]	45	11 (To be confirmed)	°C/W

[1] Test condition: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11
A	RE0	DEO	SEO	AIN4_LPF0	VREF_1.8V	RCAL1	RCAL0	AIN7_LPF1	SE1	DE1	RE1
B	CE0	VZERO0	AIN6	AIN5	AGND_REF	AIN2	AIN3/ BUF_VREF1V8	AIN1	AIN0	VZERO1	CE1
C	CAP_POT0	VBIAS0								VBIAS1	CAP_POT1
D	RC0_0	RC0_1			BMP1.1	P1.5/SPI1_CS	P1.3/SPI1_MOSI			RC1_1	RC1_0
E	AVDD_REG	VREF_2.5V			DNC		P1.2/SPI1_CLK			DNC	ADCVBIAS_CAP
F	DVDD_AD	DGND_AD			P1.0/SYS_WAKE	P1.4/SPI1_MISO	DGND			AGND	AVDD
G	DVDD_REG_AD	AVDD_DD								GPIO0/PWM0	VDCDC_CAP2P
H	XTALI	AGND_DD	SWCLK	SWDIO	P0.5/I2C_SDA	P0.3/SPI0_CS	P0.2/SPI0_MISO	P0.1/SPI0_MOSI	P0.0/SPI0_MOSI	GPIO1/PWM1	VDCDC_CAP2N
J	XTALO	P0.11/ UART_SIN	P0.10/ UART_SOUT	P2.4	P0.4/I2C_SCL	DVDD	DVDD_REG	VDCDC_CAP1N	VDCDC_CAP1P	$\overline{\text{RESET}}$	VDCDC_CAPOUT

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DNC = DO NOT CONNECT.

Figure 7. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
J10	$\overline{\text{RESET}}$	I	Reset Input (Active Low). An internal pull-up is included and enabled by default on this pin.
Digital I/O Pins			
H3	SWCLK	I	Serial Wire Debug Clock Input Pin. Internal pull-up resistor enabled by default on this pin.
H4	SWDIO	I/O	Serial Wire Debug Data Input/Output Pin. Internal pull-up resistor enabled by default on this pin.
H9	P0.0/SPI0_CLK	I/O	General-Purpose Input/Output Port 0.0/SPI0 Clock. This pin defaults as tristate.
H8	P0.1/SPI0_MOSI	I/O	General-Purpose Input/Output Port 0.1/SPI0 Data Master Output, Slave Input. This pin defaults as tristate.
H7	P0.2/SPI0_MISO	I/O	General-Purpose Input/Output Port 0.2/SPI0 Data Master Input, Slave Output. This pin defaults as tristate.
H6	P0.3/SPI0_CS	I/O	General-Purpose Input/Output Port 0.3/SPI0 Chip Select. Input for slave or output for master. This pin defaults as tristate.
J5	P0.4/I2C_SCL	I/O	General-Purpose Input/Output Port 0.4/I^2C Interface Clock for I^2C. This pin defaults as tristate.
H5	P0.5/I2C_SDA	I/O	General-Purpose Input/Output Port 0.5/ I^2C Interface Data for I^2C. This pin defaults as tristate.
J3	P0.10/UART_SOUT	I/O	General-Purpose Input/Output Port 0.10/UART Output. This pin defaults as tristate.
J2	P0.11/UART_SIN	I/O	General-Purpose Input/Output Port 0.11/UART Input. This pin defaults as tristate.

Pin No.	Mnemonic	Type[1]	Description
F5	P1.0/SYS_WAKE	I/O	General-Purpose Input/Output Port 1.0/External Interrupt Signal. Capable of waking the part from hibernate or shutdown modes. This pin defaults as tristate.
D5	BM/P1.1	I/O	Boot Mode/General-Purpose Input/Output Port 1.1. When this pin is low during and for a short time after any reset, the part enters UART download mode. This pin defaults as an input.
E7	P1.2/SPI1_CLK	I/O	General-Purpose Input/Output Port 1.2/SPI1 Clock. This pin defaults as tristate.
D7	P1.3/SPI1_MOSI	I/O	General-Purpose Input/Output Port 1.3/SPI1 Data Master Out, Slave Input. This pin defaults as tristate.
F6	P1.4/SPI1_MISO	I/O	General-Purpose Input/Output Port 1.4/SPI1 Master In, Slave Out. This pin defaults as tristate.
D6	P1.5/SPI1_CS	I/O	General-Purpose Input/Output Port 1.5/SPI1 Chip Select. This pin defaults as tristate.
J4	P2.4	I/O	General-Purpose Input/Output Port 2.4. This pin defaults as tristate.
G10	GPIO0/PWM0	I/O	General-Purpose Input/Output Port/PWM Output. Features power-on reset output and analog die power mode status. After a power-on reset, this pin will be pulled low for 32 mS after the power-on reset sequence is completed. After this period and after all other reset types, this pin defaults as tristate. This pin defaults as POR status bit after a power-on reset condition.
H10	GPIO1/PWM1	I/O	General-Purpose Input/Output Port/PWM Output. Features optional external 16 MHz clock input. This pin defaults as tristate.
Sensor Channel 0 Pins			
B1	CE0	AIO	Output of Potentiostat 0 Amplifier. Connected to counter electrode when measuring electrochemical sensors. Optionally, can be used as an ADC input. If unused, recommend connecting to AVDD_REG or AGND pin.
A1	RE0	AI	Input to Analog Input Switch Matrix. For electrochemical sensor measurement, connect to potentiostat 0 amplifier, inverting input. Optionally, can be used as an ADC input. If unused, recommend connecting to AVDD_REG or AGND pin.
A3	SE0	AI	Input to Analog Switch Matrix. For electrochemical sensor measurement, connect to TIA, inverting input. If unused, recommend connecting to AVDD_REG or AGND pin.
A2	DE0	AI	Diagnostic Electrode Input 0. Internally connected to the analog input switch matrix. If unused, recommend connecting to AVDD_REG or AGND pin.
C2	VBIAS0	AIO	VBIAS0 to DAC0 Output. Used internally to set common mode voltage of potentiostat 0 amplifier. Connect to AGND via 100 nF capacitor. Optionally, can be used as an ADC input. If unused, recommend connecting to AVDD_REG or AGND pin. Do not use this pin as a voltage source for an external circuit.
B2	VZERO0	AIO	VZERO0 to DAC0 Output. Used internally to set common mode voltage of TIA0. Optionally, can be used as an ADC input. If unused, recommend connecting to AVDD_REG or AGND pin. Do not use this pin as a voltage source for an external circuit.
D1	RC0_0	AI	Connection to External Capacitor for Low Power TIA Input. Connect other side of capacitor to RC0_1. Use 100 nF capacitor during ADI characterization. Optionally, a TIA gain resistor can be connected across RC0_0 and RC0_1.
D2	RC0_1	AI	Connection to External Capacitor for Low Power TIA Input. Connect other side of capacitor to RC0_0. Use 100 nF capacitor during ADI characterization. Optionally, a TIA gain resistor can be connected across RC0_0 and RC0_1.
C1	CAP_POT0	AI	High Frequency Filter Capacitor. Connect this pin to CE0 pin via an external capacitor of 100 nF. Used for RC filter on RE0 input.
Sensor Channel 1 Pins			
B11	CE1	AIO	Output of Potentiostat 1 Amplifier. Connected to counter electrode when measuring electrochemical sensors. Optionally, can be used as an ADC input. If unused, recommend connecting to AVDD_REG or AGND pin.
A11	RE1	AI	Input to Analog Input Switch Matrix. For electrochemical sensor measurement, connect to potentiostat 1 amplifier inverting input. Optionally, can be used as an ADC input. If unused, recommend connecting to AVDD_REG or AGND pin.
A9	SE1	AI	Input to Analog Switch Matrix. For electrochemical sensor measurement, connect to TIA, inverting input. If unused, recommend connecting to AVDD_REG or AGND pin.
A10	DE1	AI	Diagnostic Electrode Input 1. Internally connected to the analog input switch matrix. If unused, recommend connecting to AVDD_REG or AGND pin.
C10	VBIAS1	AIO	VBIAS1 to DAC1 Output. Used internally to set common mode voltage of potentiostat 1 amplifier. Connect to AGND via 100 nF capacitor. Optionally, can be used as an ADC input. If unused, recommend connecting to AVDD_REG or AGND pin. Do not use this pin as a voltage source for an external circuit.

Pin No.	Mnemonic	Type[1]	Description
B10	VZERO1	AIO	VZERO1 to DAC1 Output. Used internally to set common mode voltage of TIA1. Optionally, can be used as an ADC input. If unused, recommend connecting to AVDD_REG or AGND pin. Do not use this pin as a voltage source for an external circuit.
D11	RC1_0	AI	Connection to External Capacitor for Low Power TIA Input. Connect other side of capacitor to RC1_1. Use 100 nF capacitor during ADI characterization. Optionally, a TIA gain resistor can be connected across RC1_0 and RC1_1.
D10	RC1_1	AI	Connection to External Capacitor for Low Power TIA Input. Connect other side of capacitor to RC1_0. Use 100 nF capacitor during ADI characterization. Optionally, a TIA gain resistor can be connected across RC1_0 and RC1_1.
C11	CAP_POT1	AI	High Frequency Filter Capacitor. Connect this pin to CE1 pin via an external capacitor of 100 nF. Used for RC filter on RE1 input.
Other Analog Pins			
A7	RCAL0	AI	Calibration Resistor Connection. Connected to excitation amplifier output. Used for calibration of impedance measurement circuitry.
A6	RCAL1	AI	Calibration Resistor Connection. Connected to high power TIAs, inverting input. Used for calibration of impedance measurement circuitry.
B9	AIN0	AI	ADC Input, AIN0.
B8	AIN1	AI	ADC Input, AIN1.
B6	AIN2	AI	ADC Input, AIN2.
B7	AIN3/BUF_VREF1V8	AIO	ADC Input, AIN3. Buffered 1.8 V bias (BUF_VREF1V8). The maximum load = 200 µA. Connect BUF_VREF1V8 to AGND via a 100 pF capacitor.
A4	AIN4_LPF0	AIO	External Low Pass Filter. Required for TIA0 when measuring electrochemical sensors. A 4.7 µF capacitor is recommended when this pin is used as the low pass filter capacitor connection. Optionally, may be used as an ADC input.
B4	AIN5	AI	ADC Input, AIN5.
B3	AIN6	AI	ADC Input, AIN6.
A8	AIN7_LPF1	AIO	External Low Pass Filter. Required for TIA1 when measuring electrochemical sensors. A 4.7 µF capacitor is recommended when this pin is used as the low pass filter capacitor connection. Optionally, may be used as an ADC input.
A5	VREF_1.8V	AIO	Decoupling Capacitor Connection for 1.8 V Internal Reference. Connect a 4.7 µF capacitor between this pin and AGND.
E2	VREF_2.5V	AIO	Decoupling Capacitor Connection for 2.5 V Internal Reference. Connect a 470 nF capacitor between this pin and AGND.
E11	ADCVBIAS_CAP	AIO	Decoupling Capacitor for PGA Common Mode Reference. Connect a 470 nF capacitor between this pin and AGND.
B5	AGND_REF	S	Reference Ground Pin. Connect to AGND.
Power Pins			
G2	AVDD_DD	S	Supply Pin for Digital Die. Supplies oscillators, power-on reset, and regulator circuits. Do not connect directly to AVDD. Connect this pin to J6 and F1. See Recommended Circuit and Component Values for more details.
H2	AGND_DD	S	Ground Pin for Digital Die.
F1	DVDD_AD	S	Digital Supply for Analog Die. Connect this pin to J6 and G2. See Recommended Circuit and Component Values for more details.
F2	DGND_AD	S	Digital Ground for Analog Die.
J6	DVDD	S	Digital Supply Pin. Do not connect directly to AVDD. Connect this pin to F1 and G2. See Recommended Circuit and Component Values for more details.
F7	DGND	S	Digital Ground Pin for Whole Chip.
F11	AVDD	S	Analog Supply Pin.
F10	AGND	S	Analog Ground Pin.
J7	DVDD_REG	S	Output of 1.2 V On-Chip Low Dropout (LDO) Regulator. Connect a 470 nF capacitor between this pin and DGND.
E1	AVDD_REG	S	Output of 1.8 V On-Chip Low Dropout (LDO) Regulator. Connect a 470 nF capacitor between this pin and AGND.
G1	DVDD_REG_AD	S	Output of 1.8 V On-Chip Low Dropout (LDO) Regulator. Connect a 470 nF capacitor between this pin and DGND.
J8	VDCDC_CAP1N	S	Buck Fly Capacitor Connection to VDCDC_CAP1P (100 nF). Leave this pin unconnected if the buck convertor is disabled.

Pin No.	Mnemonic	Type[1]	Description
J9	VDCDC_CAP1P	S	Buck Fly Capacitor Connection to VDCDC_CAP1N (100 nF). Leave this pin unconnected if the buck convertor is disabled.
H11	VDCDC_CAP2N	S	Buck Fly Capacitor Connection to VDCDC_CAP2P (100 nF). Leave this pin unconnected if the buck convertor is disabled.
G11	VDCDC_CAP2P	S	Buck Fly Capacitor Connection to VDCDC_CAP2N (100 nF). Leave this pin unconnected if the buck convertor is disabled.
J11	VDCDC_CAPOUT	S	Decoupling Capacitor for DC to DC Output. 470 nF is the recommended value. Leave this pin unconnected if the buck convertor is disabled.
XTAL and No Connect Pins			
H1	XTALI	AI	External 16 MHz Crystal Oscillator Input for Analog Die. Optionally, connect to DGND_AD if not using an external crystal.
J1	XTALO	AO	External 16 MHz Crystal Oscillator Output for Analog Die. Optionally, leave unconnected if not using an external crystal.
E5	DNC		Do Not Connect. Do not connect to this pin.
E10	DNC		Do Not Connect. Do not connect to this pin.

[1] A is analog, AI is analog input, AO is analog output, D is digital, DI is digital input, DO is digital output, I is input, I/O is input/output, O is output, and S is supply.

TYPICAL PERFORMANCE CHARACTERISTICS

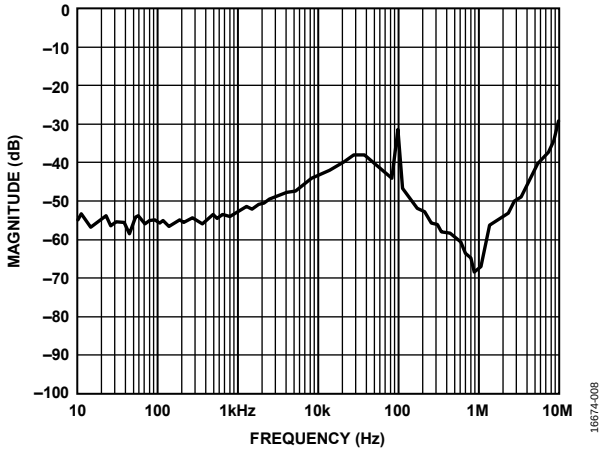

Figure 8. ADC 1.82 V Voltage Reference AC PSRR

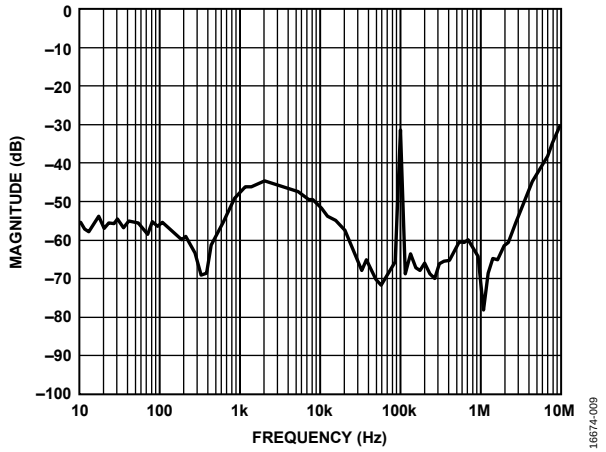

Figure 9. Low Power 2.5 V Voltage Reference AC PSRR

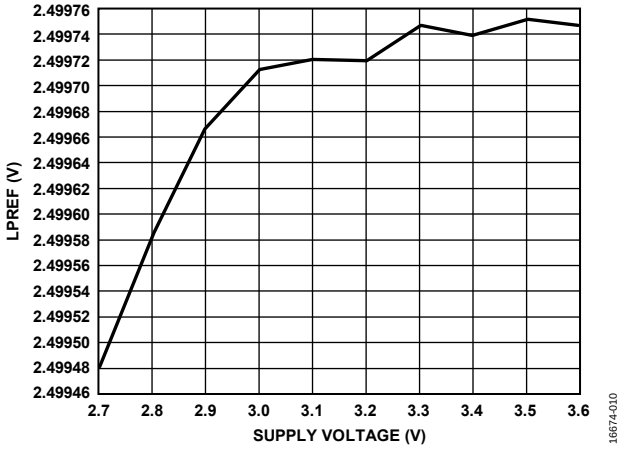

Figure 10. Low Power 2.5 V Voltage Reference DC PSRR

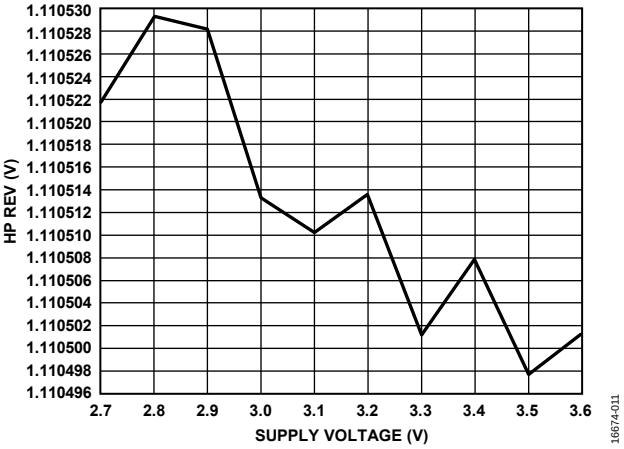

Figure 11. 1.11 V Voltage Reference DC PSRR

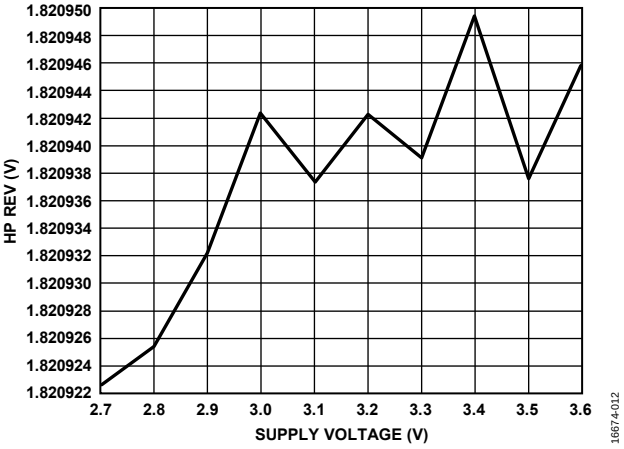

Figure 12. ADC 1.82 V Voltage Reference DC PSRR

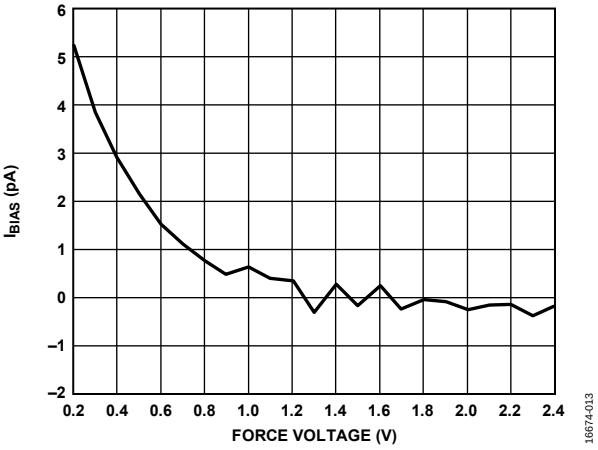

Figure 13. Potentiostat Amplifier 1 Input Bias Current vs. RE1 pin voltage

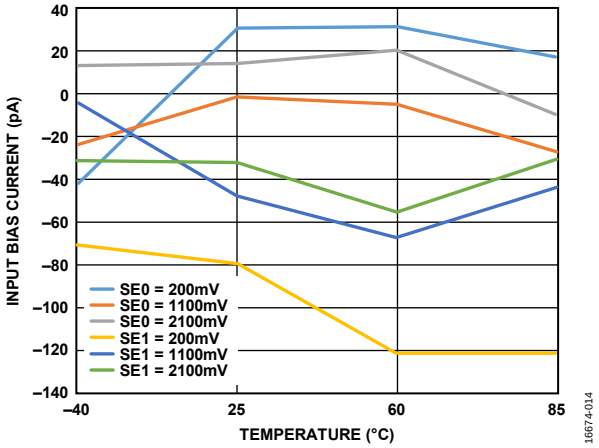

Figure 14. Low Power TIA Input Bias Current vs. Temperature

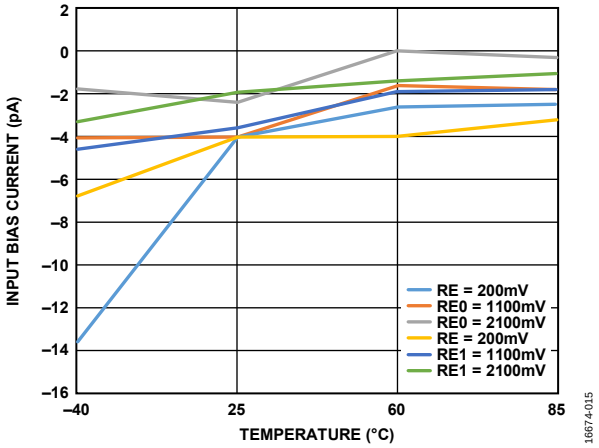

Figure 15. Low Power Potentiostat Amplifier Input Bias Current vs. Temperature

APPLICATIONS INFORMATION

RECOMMENDED CIRCUIT AND COMPONENT VALUES

The external components required by the ADuCM355 are shown in Figure 16.

There are two digital supply pins, DVDD_AD and DVDD. Decouple these pins with a 0.1 µF capacitor placed as close as possible to each of the two pins and a 4.7 µF capacitor at the supply source. Similarly, the analog supply pins, AVDD and AVDD_DD, each require a 0.1 µF capacitor placed as close as possible to each pin with a 4.7 µF capacitor at the supply source.

The ADuCM355 contains three internal regulators. These regulators each require external decoupling capacitors. The pin names for the digital regulators are DVDD_REG and DVDD_REG_AD. Each requires a 0.47 µF capacitor to the digital ground (DGND). The AVDD_REG analog regulator requires a 0.47 µF decoupling capacitor to AGND (if separate GND planes are used).

The ADuCM355 has an optional dc-to-dc convertor (buck convertor) on the digital die that can save power if enabled. When unused, the VDCDC_CAP1N, VDCDC_CAP1P, VDCDC_ CAP2N, VDCDC_CAP2P, and VDCDC_CAPOUT can be left unconnected. If the dc-to-dc converter is used, then a 100 nF capacitor must be connected between VDCDC_CAP1N and VDCDC_CAP1P and between VDCDC_CAP2N and VDCDC_ CAP2P. The VDCDC_CAPOUT pin required a 0.47 µF capacitor to the digital ground when the dc-to-dc converter is enabled.

There are three internal references requiring external capacitors for stability. Connect the ADCVBIAS_CAP and VREF_2.5V pins to AGND via 0.47 µF capacitors. Connect a 4.7 µF capacitor between the VREF_1.8V pin and AGND.

For calibration purposes, an external precision resistor is recommended between the RCAL0 and RCAL1 pins. Typically, this is a 200 Ω resistor but can be different values. A low ppm temperature coefficient (≤10ppm/°C) and 0.1% or better accuracy is better for tightest system calibration.

Figure 16 shows connections between the ADuCM355 and an external 3-lead, electrochemical gas sensor. For EMC purposes, (radiated immunity), a capacitor to GND is recommended for each of the sensor pins. Typically a value between 22 pf and 30 pF is recommended. Also, 100 nF capacitor between the CEx pin of the sensor and the ADuCM355 CAP_POT0 pin is recommended. Similarly, if the ADuCM355 Channel 1 potentiostat is used, a 100 nF capacitor between the CEx pin of the sensor and the ADuCM355 CAP_POT1 is recommended. The output of each of the low power TIAs has a programmable low pass filter. The resistor is internal and is programmable, and the capacitor for each of the low pass filters is external. The capacitor connects between the AIN4_LPF0 pin and AGND for TIA0, and between the AIN7_LPF1 pin and AGND for TIA1. The low power TIAs require a 100 nF capacitor between their inverting input and output terminals for stability purposes. For LPTIA0, the capacitor connects between the RC0_0 and RC0_1 pins. If the LPTIA1 channel is used, connect the capacitor between the RC1_0 and RC1_1 pins.

If the low power DACs are used, each output VBIAS0, VZERO0, VBIAS1, and VZERO1 requires a 100 nF capacitor to AGND.

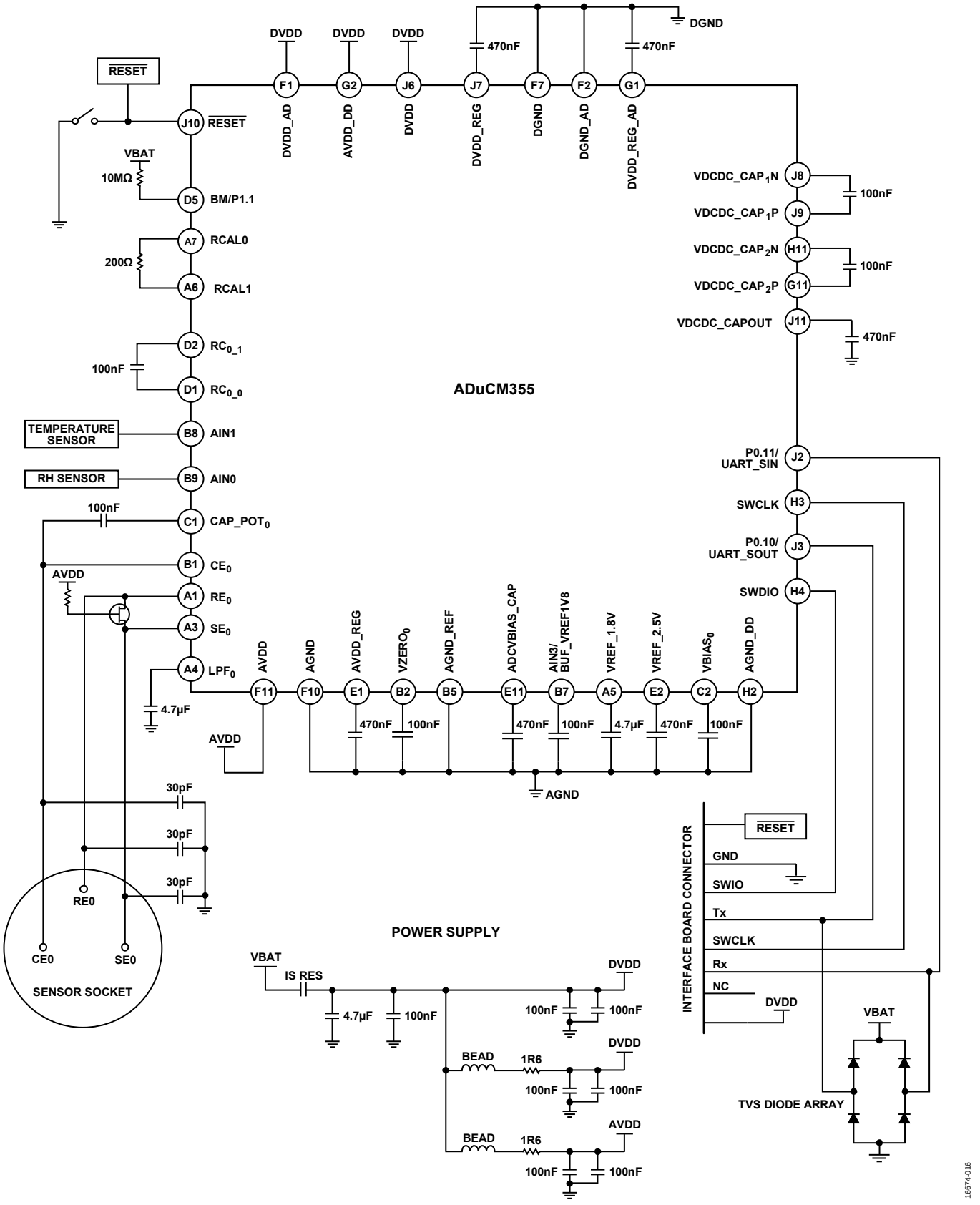

Figure 16. Recommended External Components

OUTLINE DIMENSIONS

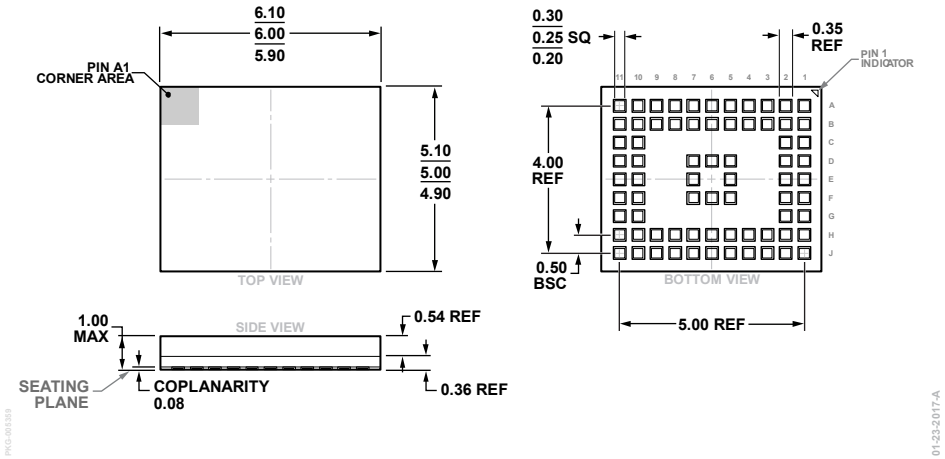

Figure 17. 72-Terminal Land Grid Array [LGA]
(CC-72-2)
Dimensions shown in millimeters

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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