Design Example Report

Title	***65 W Power Supply Using InnoSwitch3™-CE, INN3168C-H101***
Specification	90 VAC – 265 VAC Input; 19 V, 3.4 A Output
Application	Open Frame
Author	Applications Engineering Department
Document Number	DER-535
Date	September 9, 2017
Revision	1.0

Summary and Features

- Built in synchronous rectification for >90% efficiency without NTC at nominal AC input
- All the benefits of secondary side control with the simplicity of primary side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
- Secondary sensed output overvoltage protection (OVP) for accurate fault protection
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 19 V, 3.4 A power supply utilizing INN3168C from the InnoSwitch3-CH family of ICs.

This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

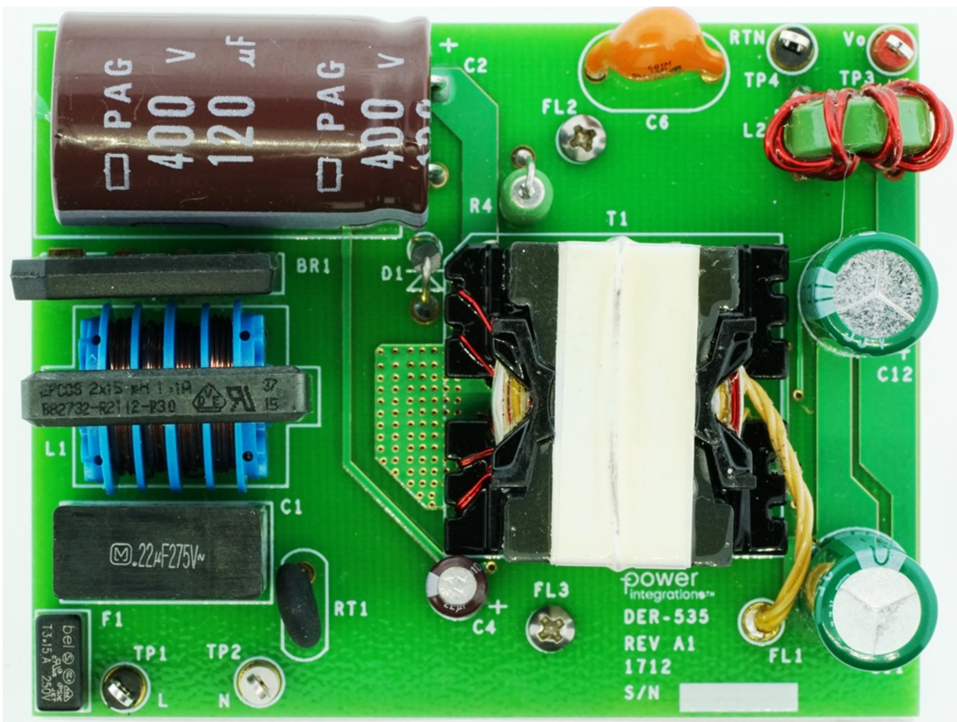

Figure 1 – Populated Circuit Board Photograph, Top.

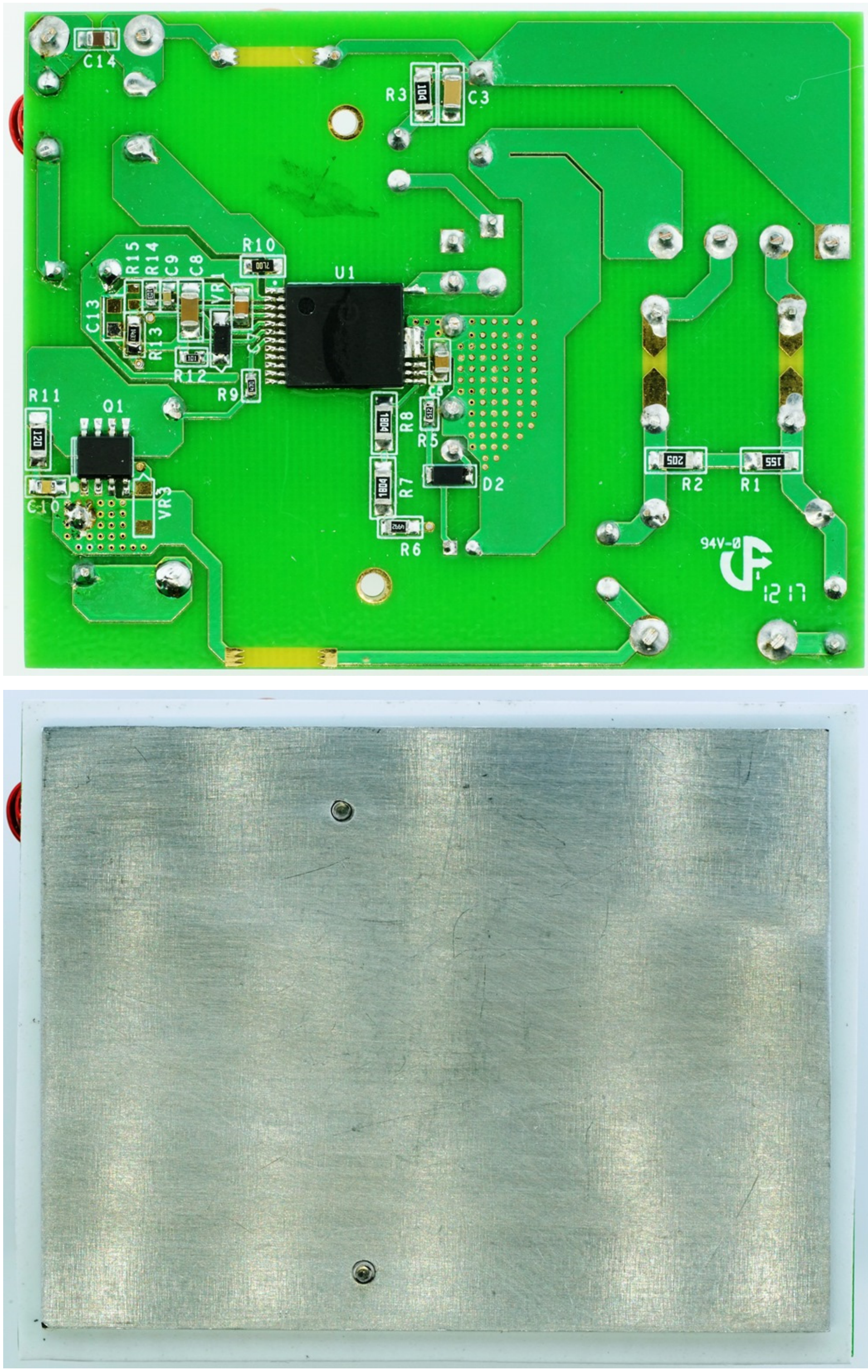

Figure 2 – Populated Circuit Board Photograph, Bottom with Heat Spreader.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage	V_{OUT}	18	19	20	V	±5%.
Output Ripple Voltage	V_{RIPPLE}			380	mV	20 MHz Bandwidth.
Output Current	I_{OUT}	0		3.4	A	
Total Output Power						
Continuous Output Power	P_{OUT}			65	W	
Efficiency						
Full Load	η	89			%	Measured at 115 / 230 VAC, P_{OUT} 25 °C.
No-Load Input Power				75	mW	V_{IN} at 230 VAC.
Leakage current				40	uA	At 250 VAC.
Transient output voltage				5	%	Transient with 90% of Max Current.
Hold up time		5			ms	At 115 VAC and Full Load.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Combination Surge						
Common mode		2.5			kV	
Differential		2.5			kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

3 Schematic

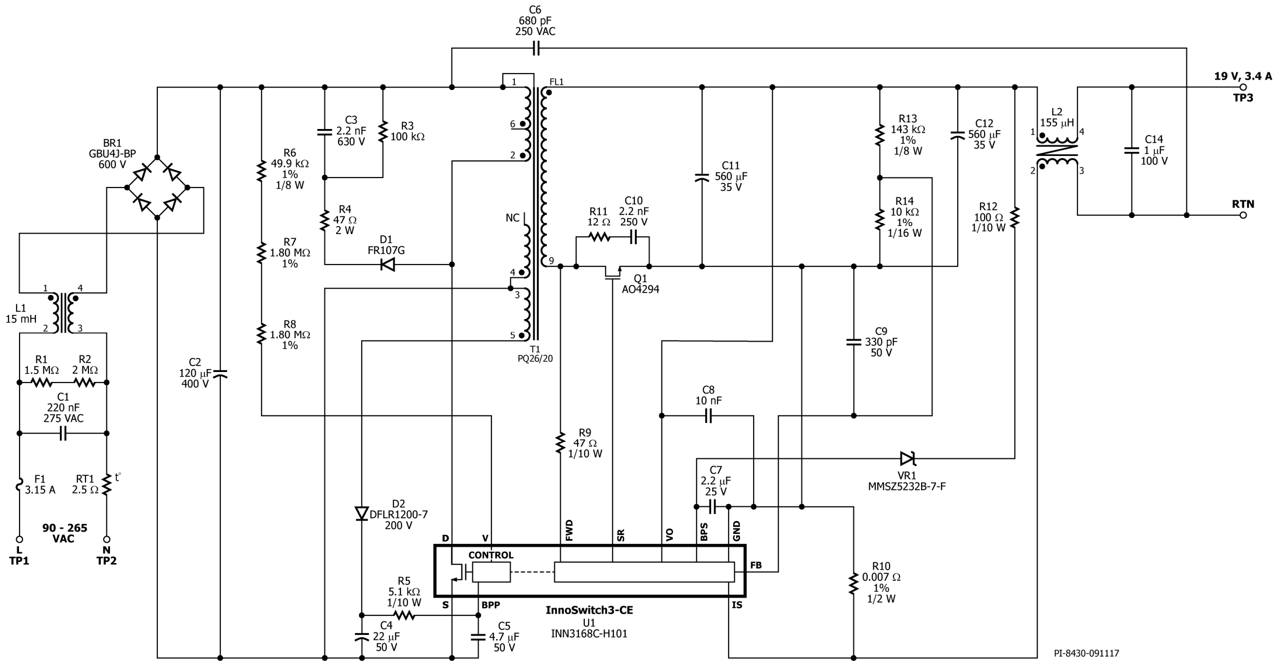

Figure 3 – Schematic.

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4 Circuit Description

4.1 Input EMI Filtering

Fuse F1 isolates the circuit and provides protection from component failure and the common mode choke L1 with X capacitor C1 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input capacitor, C2. Capacitor C6 provides common mode noise filtering.

4.2 INN3168C Primary

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 650 V power MOSFET inside the INN3168C IC (U1).

A low cost RCD clamp formed by D1, R3, R4, and C3 limits the peak Drain voltage due to the effects of transformer leakage reactance and output trace inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C5, when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C4, and fed in the BPP pin via a current limiting resistor R5.

Resistors R6, R7, and R8 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitor C2. At approximately 100 V DC, the current through these resistors exceeds the line under-voltage threshold, which results in enabling of U1. At approximately 420 V DC, the current through these resistors exceeds the line overvoltage threshold, which results in disabling of U1.

4.3 INN3168C Secondary

The secondary side of the INN3168C provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 19 V output is provided by SR FET Q1. Very low ESR capacitors, C11 and C12, provide filtering. Output rectification for the 19 V output is provided by SR FET Q1. RC snubber network comprising R11 and C10 for Q1 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gate of Q1 is turned on based on the winding voltage sensed via R9 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary side control of the primary side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin and charges the decoupling capacitor C7 via an internal regulator. The OVP sensing Zener diode, VR1, provides secondary side output over voltage protection with R12.

Resistors R13 and R14 form a voltage divider network that senses the output voltage. INN3168C IC has an internal reference of 1.265 V. Capacitor C9 provides decoupling from high frequency noise affecting power supply operation. The output current is sensed by R10 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current. Capacitor C8 protects U1 from ESD. Output common mode choke L2 reduces high frequency common mode noise and protect U1 from common mode surge.

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5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 µm) unless otherwise stated

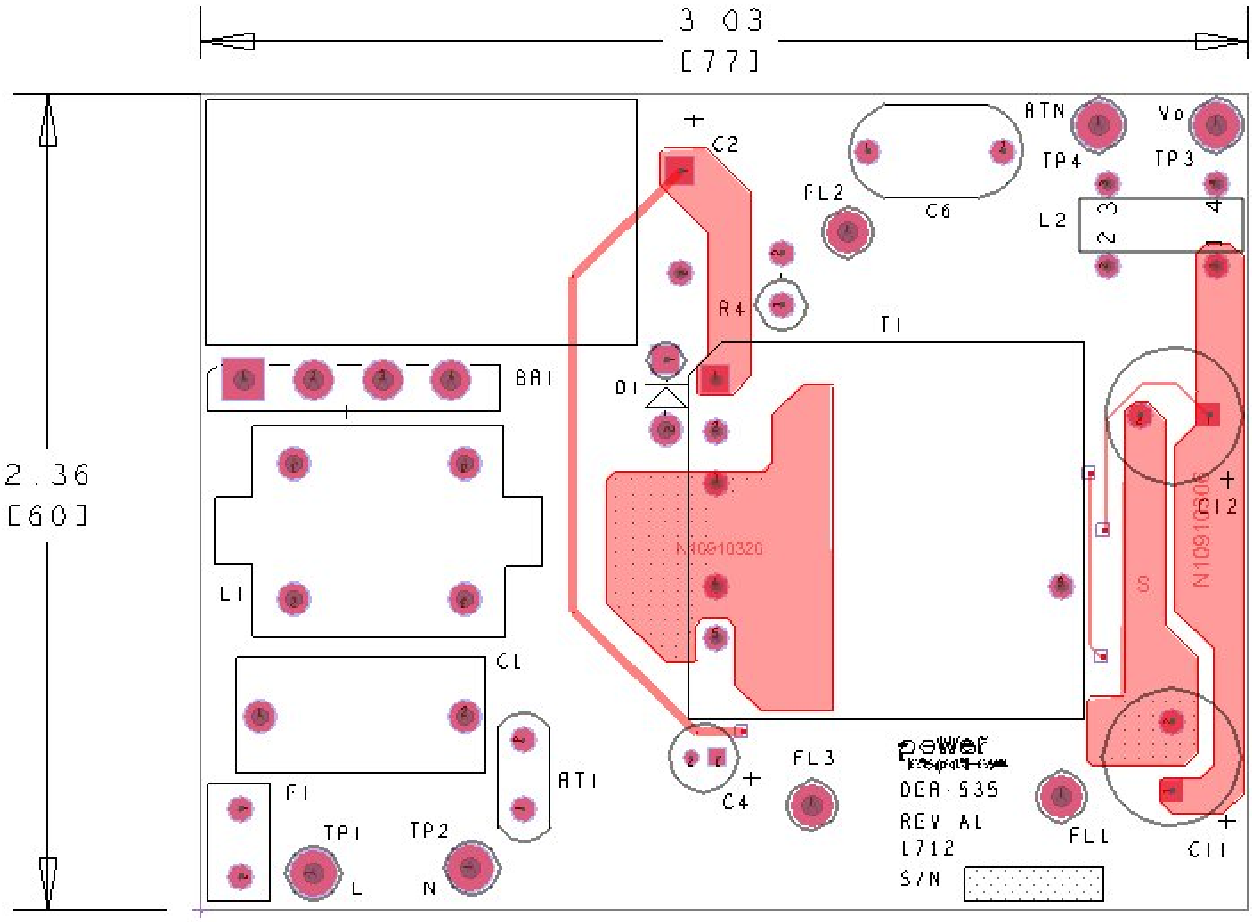

Figure 4 – Printed Circuit Layout, Top.

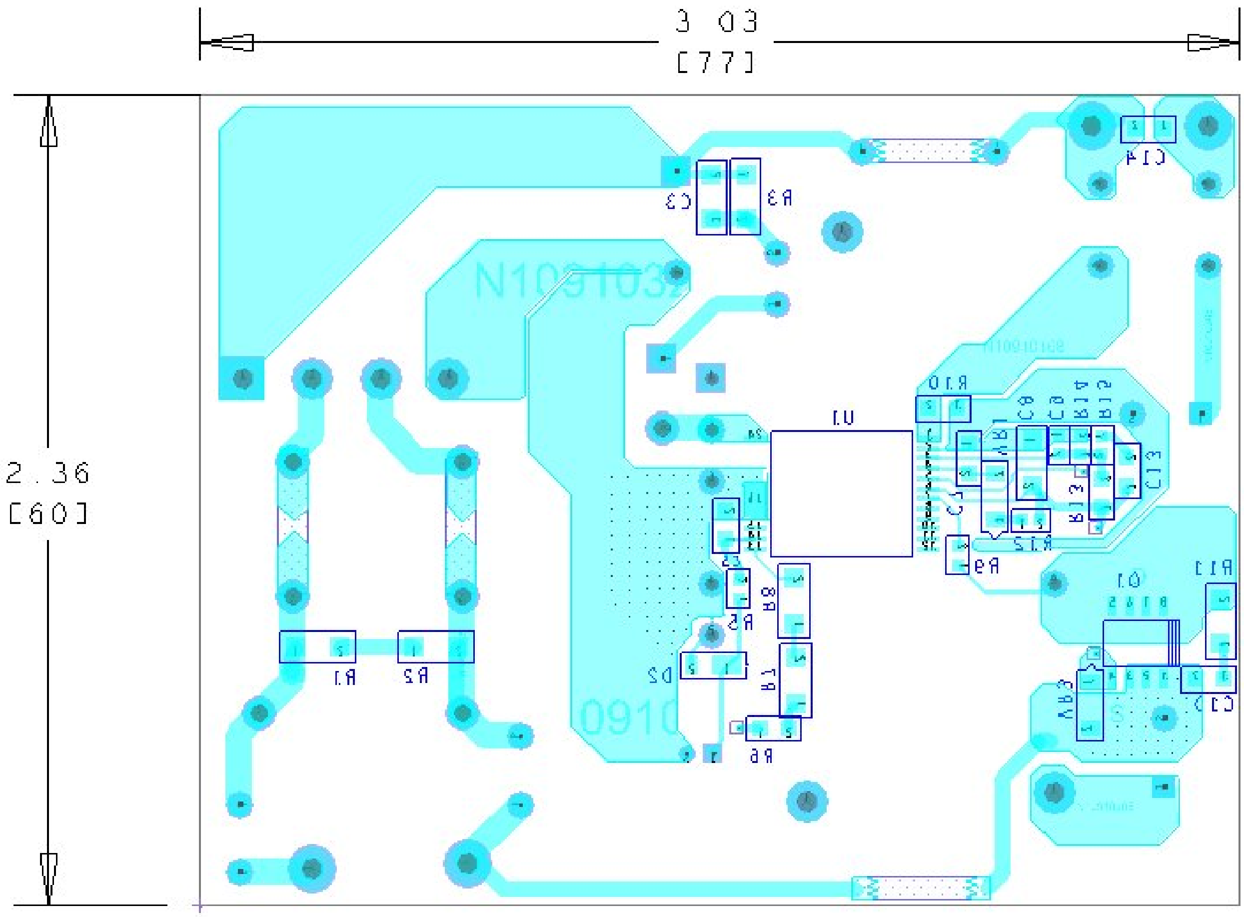

Figure 5 – Printed Circuit Layout, Bottom.

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6 Heat Spreader

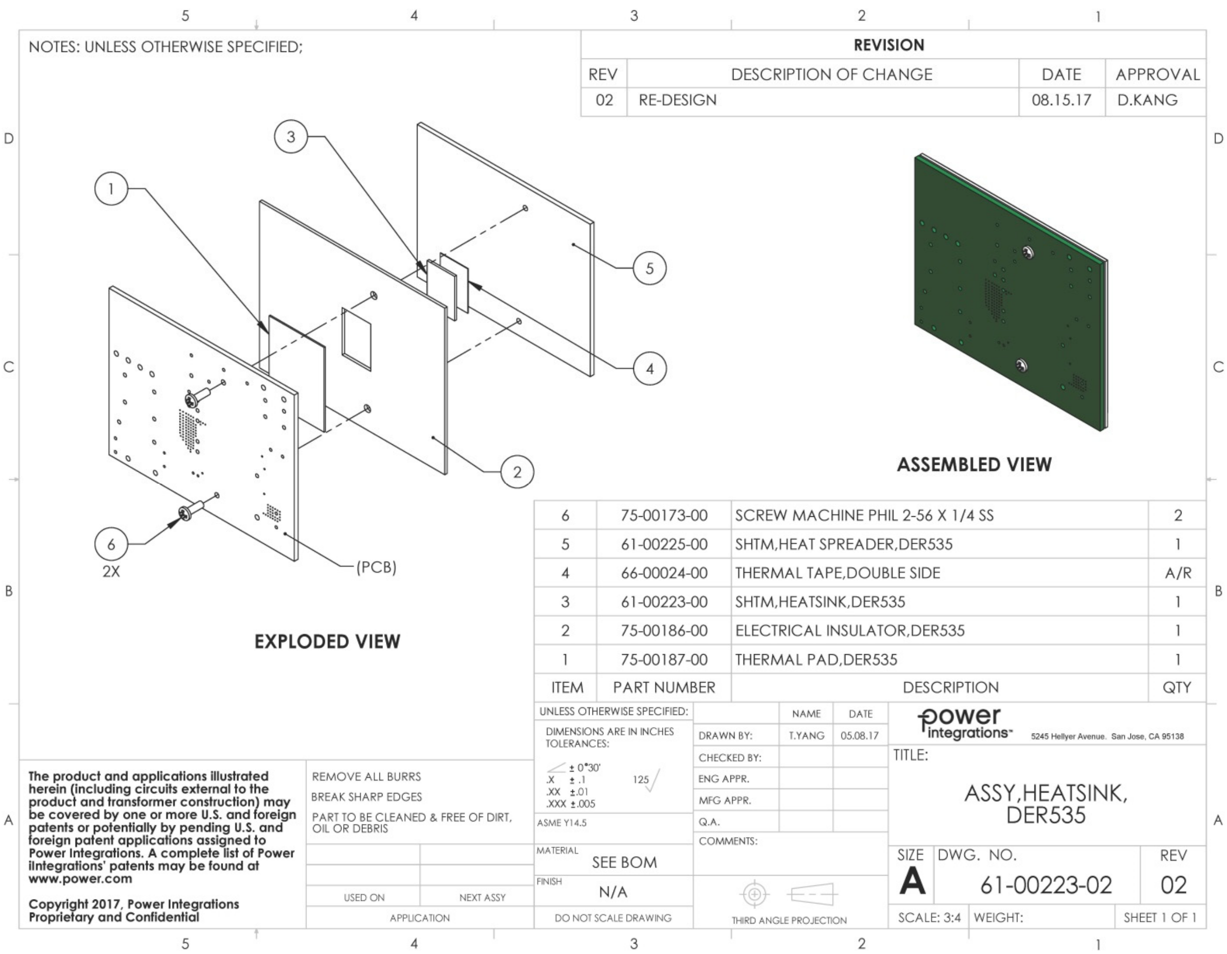

Figure 6 – Heat Spreader.

7 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 4 A, Bridge Rectifier, GBU Case	GBU4J-BP	Micro Commercial
2	1	C1	220 nF, 275 VAC, Film, X2	ECQ-U2A224ML	Panasonic
3	1	C2	120 μF, 400 V, Electrolytic, (18 x 30)	EPAG401ELL121MM30S	Nippon Chemi-Con
4	1	C3	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
5	1	C4	22 μF, 50 V, Electrolytic, Very Low ESR, 340 mΩ, (5 x 11)	EKZE500ELL220ME11D	Nippon Chemi-Con
6	1	C5	4.7 μF, 50 V, Ceramic, X5R, 0805	CL21A475KBQNNNE	Samsung
7	1	C6	680 pF, Ceramic, Y1	440LT68-R	Vishay
8	1	C7	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
9	1	C8	10 nF, 630 V, Ceramic, X7R, 1206	C1206C103KBRACTU	Kemet
10	1	C9	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
11	1	C10	2.2 nF, 250 V, Ceramic, X7R, 0805	C2012X7R2E222K085AA	TDK
12	2	C11 C12	560 μF, 35 V, Electrolytic, Very Low ESR, 22 mΩ, (10 x 25)	EKZE350ELL561MJ25S	Nippon Chemi-Con
13	1	C14	1 μF, 100 V, Ceramic, X7S, 0805	C2012X7S2A105K125AB	TDK
14	1	D1	1000 V,1 A, Fast Recovery Diode, GP DO-41	FR107G-B	Rectron
15	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
16	1	F1	3.15 A, 250V, Slow, RST	507-1181	Belfuse
17	1	L1	15 mH, 1.1 A, Common Mode Choke	B82732R2112B30	Epcos
18	1	L2	155 μH, 20%,Toroidal CM Choke, toroidal core	DER535_Output_CMC	Power Integrations
19	1	Q1	MOSFET, N-CH, 100 V, 11.5 A, 8SOIC,	AO4294	Alpha & Omega Semi
20	1	R1	RES, 1.5 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ155V	Panasonic
21	1	R2	RES, 2 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ205V	Panasonic
22	1	R3	RES, 100 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ104V	Panasonic
23	1	R4	RES, 47 Ω, 5%, 2 W, Wire Wound, Fusible	FW20A47R0JA	Bourns
24	1	R5	RES, 5.1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ512V	Panasonic
25	1	R6	RES, 49.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4992V	Panasonic
26	2	R7 R8	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
27	1	R9	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
28	1	R10	RES, 0.007 Ω, ±1%, 0.5 W, 1/2 W, 0805, Current Sense	PMR10EZPFU7L00	Rohm
29	1	R11	RES, 12 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ120V	Panasonic
30	1	R12	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
31	1	R13	RES, 143 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1433V	Panasonic
32	1	R14	RES, 10 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
33	1	RT1	NTC Thermistor, 2.5 Ω, 3 A	SL08 2R503	Ametherm
34	1	T1	Bobbin, PQ26/20, Vertical, 12 pins	BPQ26/20-1112CPFR	TDK
35	1	U1	InnoSwitch3-CE, InSOP24	INN3168C-H101	Power Integrations
36	1	VR1	DIODE ZENER 18 V 500 mW SOD123	MMSZ5248B-7-F	Diodes, Inc

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8 Transformer (T1) Specification

8.1 Electrical Diagram

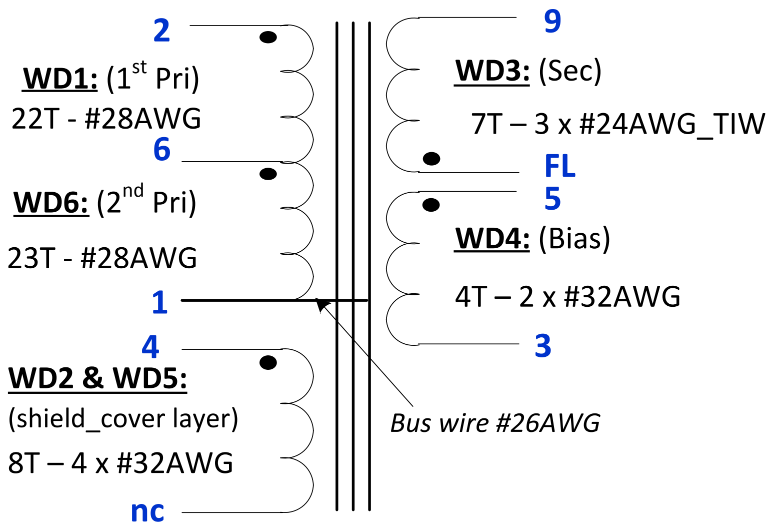

Figure 7 –Transformer Electrical Diagram

8.2 Electrical Specifications

Parameter	Condition	Spec.
Electrical Strength	1 second, 60 Hz, from pins 1- 6 to pins 7-12.	3000 VAC
Primary Inductance	Pins 1-2, all other open, measured at 100 kHz, 0.4 V_{RMS}.	880 μH, ± 7%
Resonant Frequency	Pins 1-2, all other open.	1200 kHz (Min.)
Primary Leakage	Pins 1-2, with FL-9 shorted, measured at 100 kHz, 0.4 V_{RMS}.	8μH (Max.)

8.3 Materials List

Item	Description
[1]	Core: PQ26/20, TDK-PC95, gapped for ALG of 434nH/T².
[2]	Bobbin: PQ26/20, Vertical, 12 pins(6/6), TDK; or Equivalent.
[3]	Magnet Wire: #28 AWG Double Coated, Solderable.
[4]	Magnet Wire: #32 AWG Double Coated, Solderable.
[5]	Magnet Wire: #24 AWG Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 9.0mm Wide.
[7]	Bus Wire: #26 AWG, Belden Electronics Div.; or Equivalent.
[8]	Varnish: Dolph BC-359.

8.4 Transformer Build Diagram

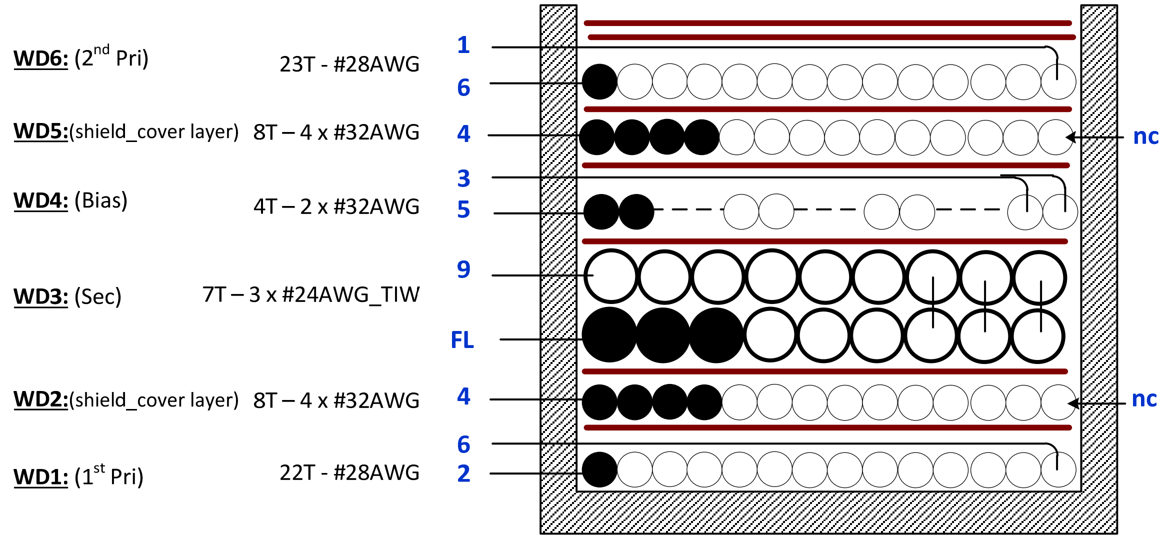

Figure 8 – Transformer Build Diagram

8.5 Transformer Construction

Winding Preparation	Place the bobbin Item [2] on the mandrel with the pin side is on the left side Winding direction is clockwise direction.
WD1 1st Primary	Start at pin 2, wind 22 turns of wire Item [3] in 1 layer. At the last turn bring the wire back to the left and finish at pin 6.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD2 Shield Cover Layer	Start at pin 4, wind 8 quafilar turns of wire Item [4] in 1 layer. At the last turn, cut short wires for no-connect nc.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD3 Secondary	Use 2 wires Item [5] temporarily hang on pin 10 as start lead FL, leave ~ 1" floating, wind 7 turns in 2 layers and finish at pin 9.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD4 Bias	Start at pin 5, wind 4 bifilar turns of wire Item [4] in 1 layer, spread the wires evenly along the width of bobbin. At the last turn bring the wires back to the left and finish at pin 3.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD5 Shield Cover Layer	Wind the same as WD2, start at pin 4, wind 8 quafilar turns of wire Item [4] in 1 layer. At the last turn, cut short wires for no-connect nc .
Insulation	Place 1 layer of tape Item [6] for insulation.
WD6 2nd Primary	Start at pin 6, wind 23 turns of wire Item [3] in 1 layer. At the last turn, bring the wire back to the left and finish at pin 1.
Insulation	Place 3 layers of tape Item [6] for insulation and secure the windings.
Finish Assembly	Gap core halves to get 880 μH inductance. Wrap around the core halves with bus wire Item [7] then connect to pin 1, and secure all together with tape. Varnish Item [8].

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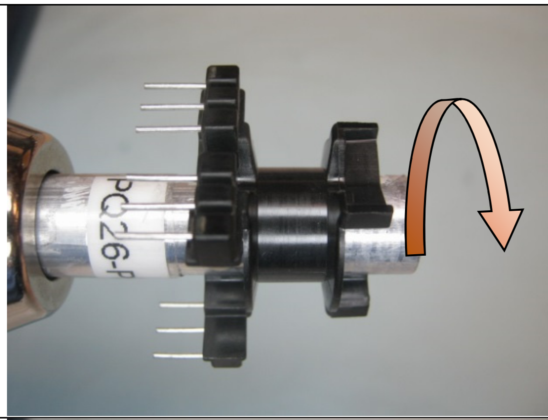
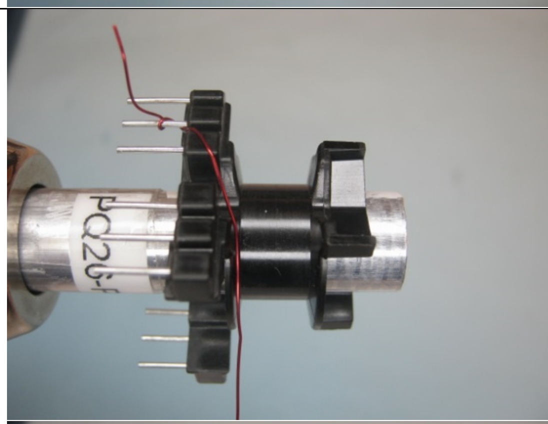
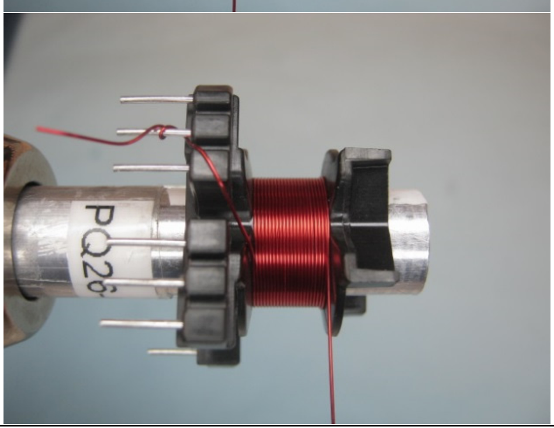
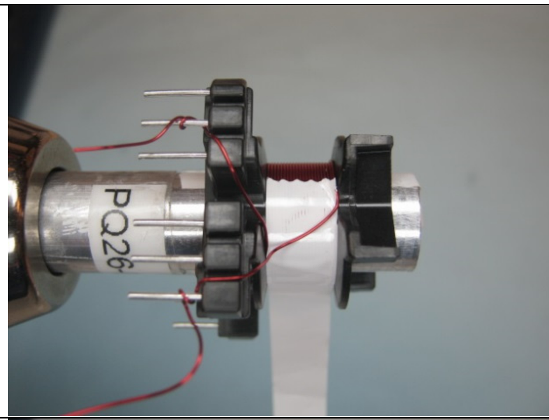
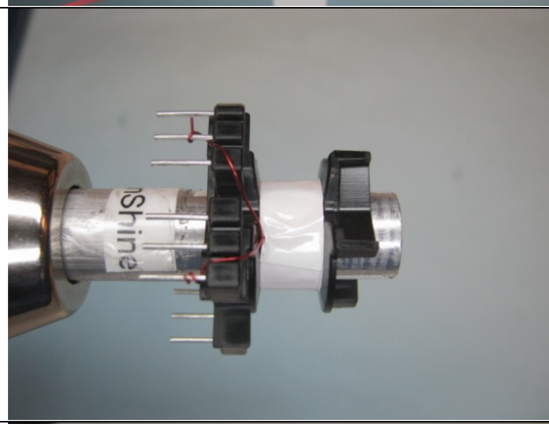
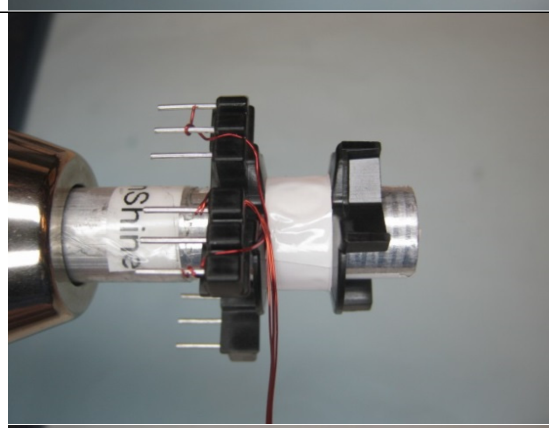
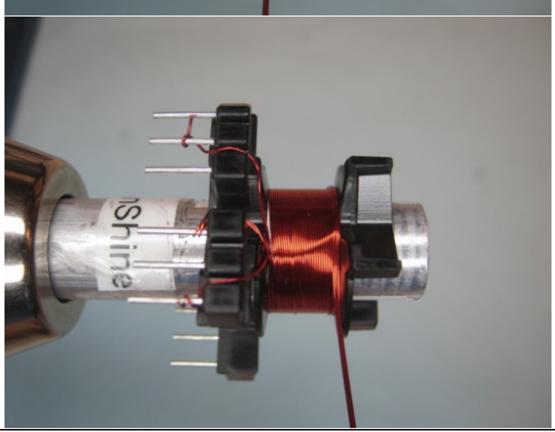
8.6 Winding Illustrations

Winding Preparation		Place the bobbin Item [2] on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
WD1 **1st Primary**	 	Start at pin 2, wind 22 turns of wire Item [3] in 1 layer. At the last turn bring the wire back to the left and finish at pin 6.

		
Insulation		Place 1 layer of tape Item [6] for insulation.
WD2 **Shield Cover Layer**	 	Start at pin 4, wind 8 quafilar turns of wire Item [4] in 1 layer. At the last turn, cut short wires for no-connect nc.

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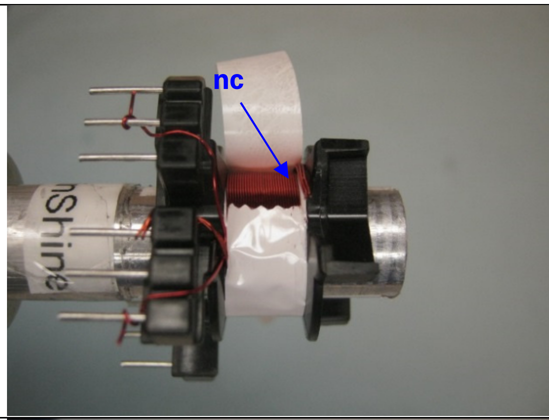
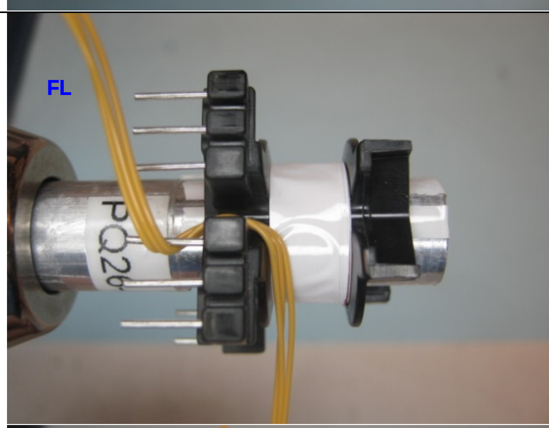
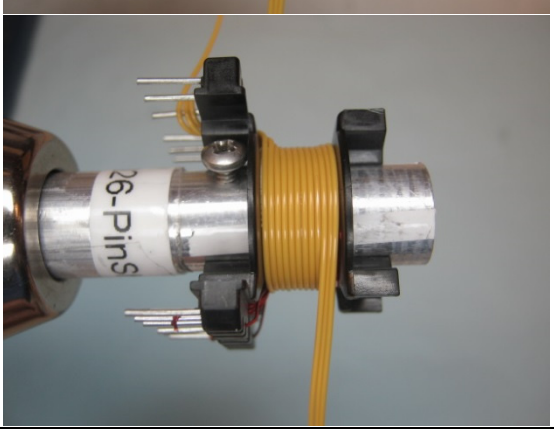
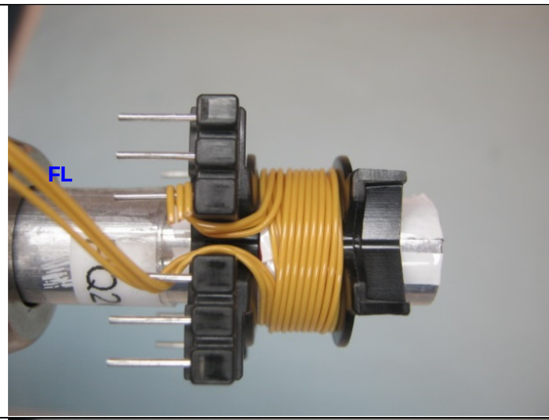
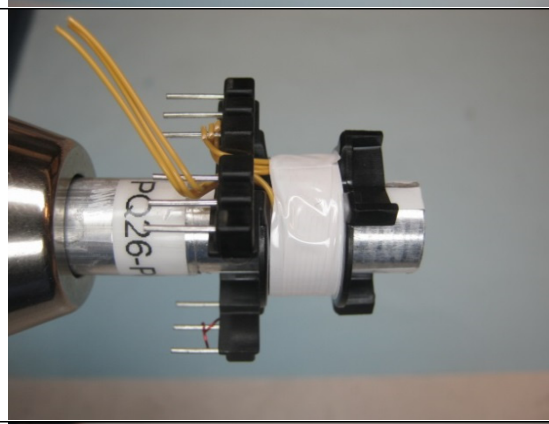
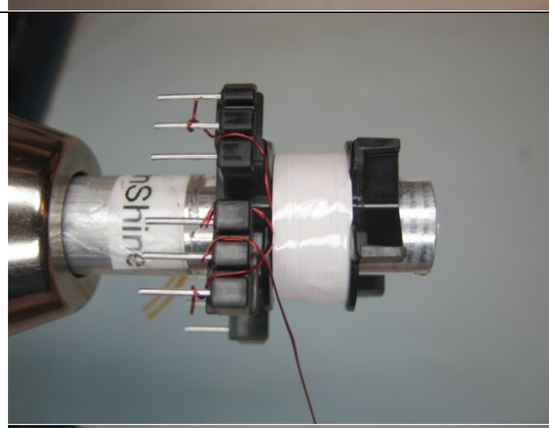
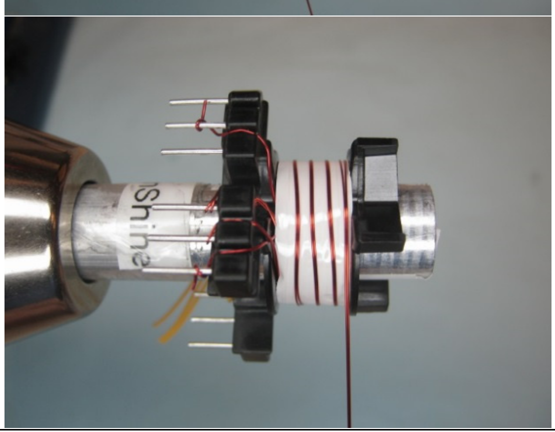
		
Insulation		Place 1 layer of tape Item [6] for insulation.
WD3 **Secondary**	 	Use 2 wires Item [5] temporarily hang on pin 10 as start lead FL, leave ~ 1” floating, wind 7 turns in 2 layers and finish at pin 9.

		
Insulation		Place 1 layer of tape Item [6] for insulation.
WD4 **Bias**	 	Start at pin 5, wind 4 bifilar turns of wire Item [4] in 1 layer, spread the wires evenly along the width of bobbin. At the last turn bring the wires back to the left and finish at pin 3.

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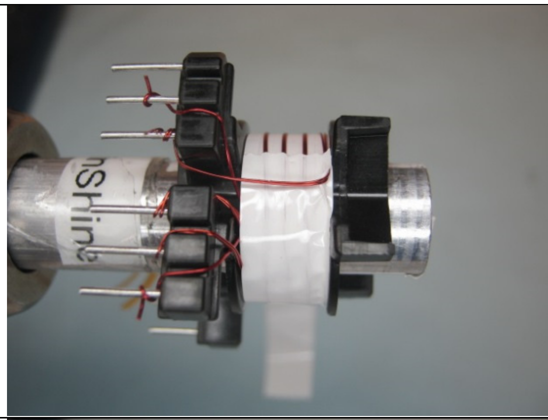
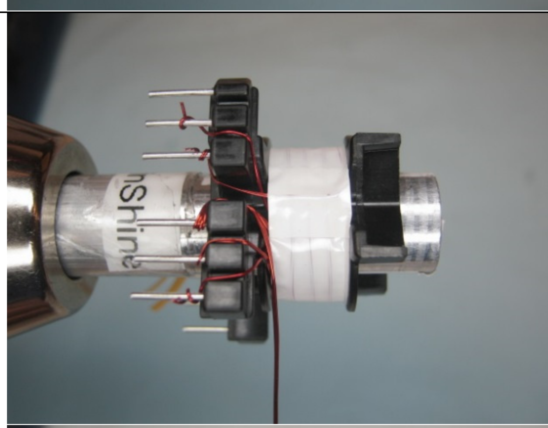
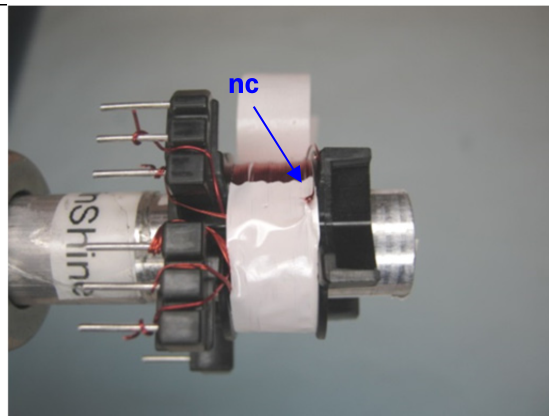
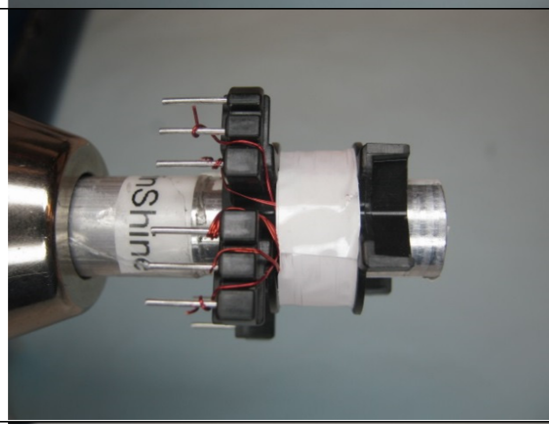
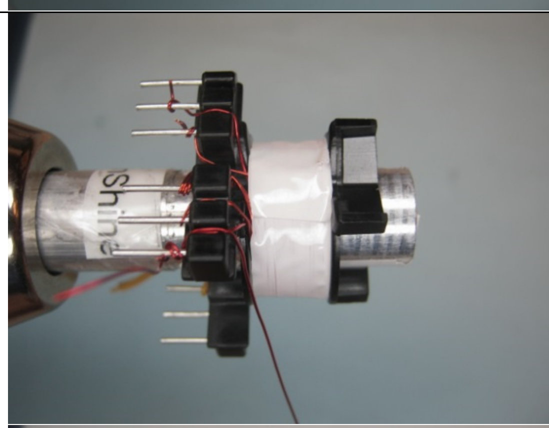
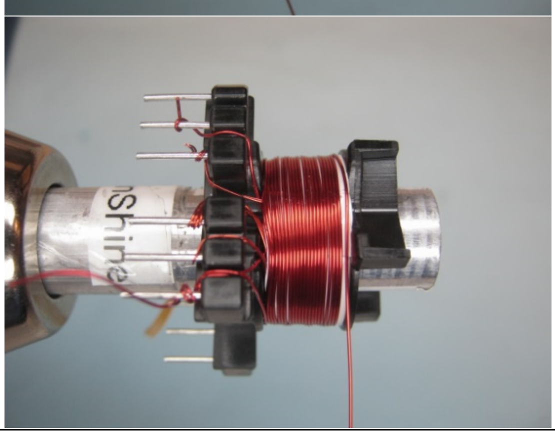
		
Insulation		Place 1 layer of tape Item [6] for insulation.
WD5 **Shield Cover Layer**	 	Start at pin 4, wind 8 quafilar turns of wire Item [4] in 1 layer. At the last turn, cut short wires for no-connect nc.

		
Insulation		Place 1 layer of tape Item [6] for insulation.
WD6 **2nd Primary**	 	Start at pin 6, wind 23 turns of wire Item [3] in 1 layer. At the last turn bring the wire back to the left and finish at pin 1.

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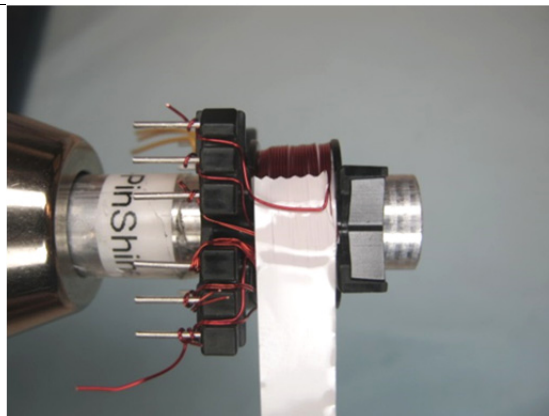
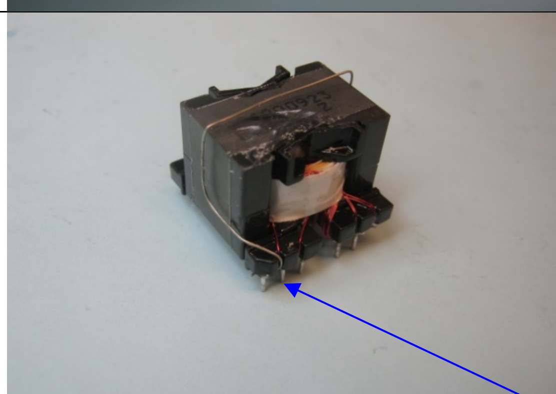
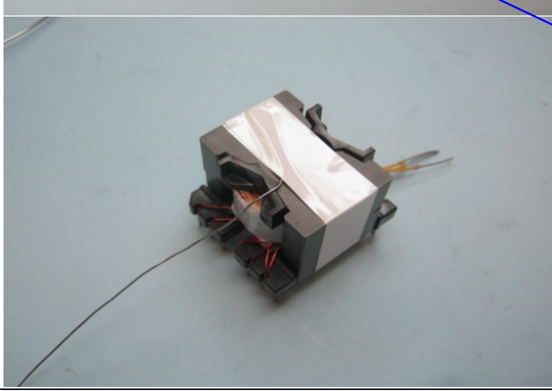
		
Insulation		Place 3 layers of tape Item [6] for insulation and secure the windings.
Finish Assembly	 	Gap core halves to get 880 µH inductance. Wrap around the core halves with bus wire Item [7] then connect to pin 1, and secure all together with tape.

9 Output CMC Specification

9.1 Electrical Diagram

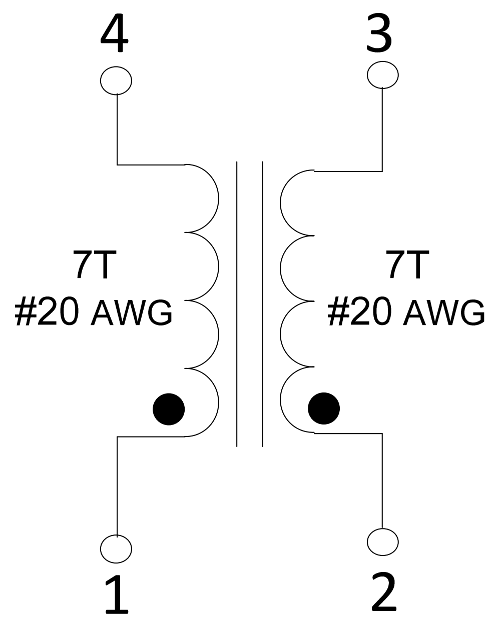


Figure 9 – Inductor Electrical Diagram.

9.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and pin 4 or pin 2 and pin 3 with all other windings open.	155 μH
Tolerance	Tolerance of Primary Inductance.	±20%

9.3 Material List

Item	Description
[1]	Toroid Core: 32-00315-00.
[2]	Magnet Wire: #20 AWG.

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9.4 Inductor Build Diagram

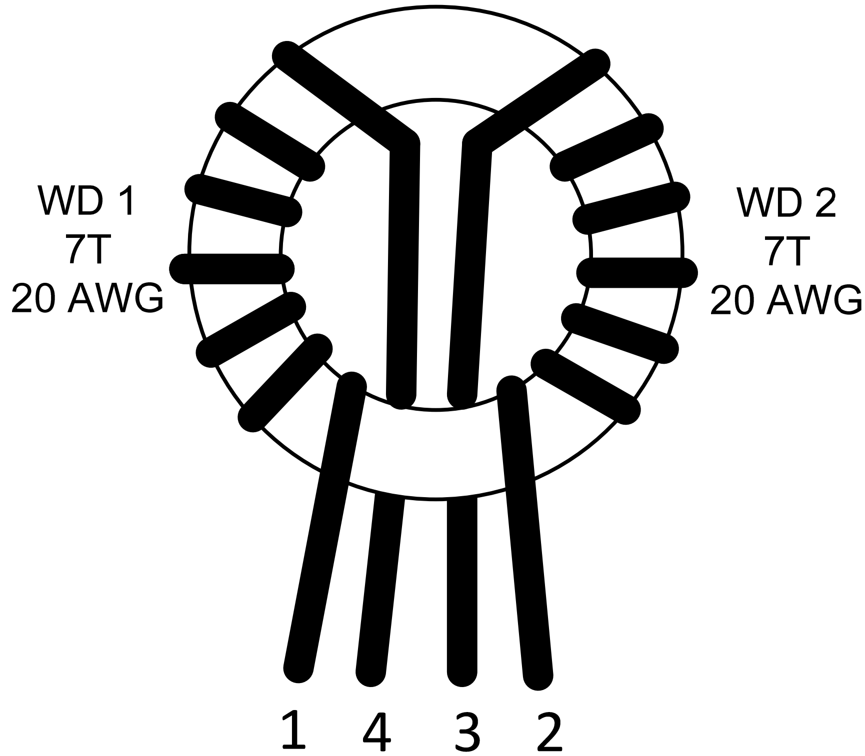

Figure 10 – Inductor Build Diagram.

9.5 Inductor Construction

1. Winding 1 - Wind 7 turns of Item [2] as shown in above figure.
2. Winding 2 - Wind 7 turns of Item [2] as shown in above figure.
3. Apply Varnish.

10 Transformer Design Spreadsheet

ACDC_InnoSwitch3-CE_Flyback_083017; Rev.1.0; Copyright Power Integrations 2017	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 CE Flyback Design Spreadsheet
APPLICATION VARIABLES					
VIN_MIN	90		90	V	Minimum AC input voltage
VIN_MAX			265	V	Maximum AC input voltage
VIN_RANGE			UNIVERSAL		Range of AC input voltage
LINEFREQ			60	Hz	AC Input voltage frequency
CAP_INPUT	120.0		120.0	uF	Input capacitor
VOUT	19.00		19.00	V	Output voltage at the board
PERCENT_CDC	0%		0%		Percentage (of output voltage) cable drop compensation desired at full load
IOUT	3.40		3.40	A	Output current
POUT		Info	64.60	W	The specified output power exceeds the device power capability: Verify thermal performance
EFFICIENCY	0.89		0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
FACTOR_Z			0.50		Z-factor estimate
ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
PRIMARY CONTROLLER SELECTION					
ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
DEVICE_GENERIC	Auto		INN31X8		Generic device code
DEVICE_CODE			INN3168C		Actual device code
POUT_MAX			55	W	Power capability of the device based on thermal performance
RDSON_100DEG			1.53	Ω	Primary MOSFET on time drain resistance at 100 degC
ILIMIT_MIN			1.68	A	Minimum current limit of the primary MOSFET
ILIMIT_TYP			1.85	A	Typical current limit of the primary MOSFET
ILIMIT_MAX			2.02	A	Maximum current limit of the primary MOSFET
VDRAIN_BREAKDOWN			650	V	Device breakdown voltage
VDRAIN_ON_MOSFET			1.15	V	Primary MOSFET on time drain voltage
VDRAIN_OFF_MOSFET			565.4	V	Peak drain voltage on the primary MOSFET during turn-off
WORST CASE ELECTRICAL PARAMETERS					
FSWITCHING_MAX	89000		89000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
VOR	122.0		122.0	V	Seconday voltage reflected to the primary when the primary MOSFET turns off
VMIN			92.55	V	Valley of the rectified minimum AC input voltage at full power
KP			0.41		Measure of continuous/discontinuous mode of operation
MODE_OPERATION			CCM		Mode of operation
DUTYCYCLE			0.572		Primary MOSFET duty cycle
TIME_ON			10.79	us	Primary MOSFET on-time
TIME_OFF			4.81	us	Primary MOSFET off-time
LPRIMARY_MIN			836.3	uH	Minimum primary inductance
LPRIMARY_TYP			880.4	uH	Typical primary inductance
LPRIMARY_TOL	5.0		5.0	%	Primary inductance tolerance

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LPRIMARY_MAX			924.4	uH	Maximum primary inductance
PRIMARY CURRENT					
IPEAK_PRIMARY			1.87	A	Primary MOSFET peak currrent
IPEDESTAL_PRIMARY			0.97	A	Primary MOSFET current pedestal
IAVG_PRIMARY			0.75	A	Primary MOSFET average current
IRIPPLE_PRIMARY			1.11	A	Primary MOSFET ripple current
IRMS_PRIMARY			1.02	A	Primary MOSFET RMS current
SECONDARY CURRENT					
IPEAK_SECONDARY			12.01	A	Secondary winding peak current
IPEDESTAL_SECONDARY			6.26	A	Secondary winding current pedestal
IRMS_SECONDARY			6.31	A	Secondary winding RMS current
TRANSFORMER CONSTRUCTION PARAMETERS					
CORE SELECTION					
CORE	Custom	Info	Custom		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
CORE CODE	PQ2620		PQ2620		Core code
AE	121.00		121.00	mm^2	Core cross sectional area
LE	45.00		45.00	mm	Core magnetic path length
AL	5530		5530	nH/turns^2	Ungapped core effective inductance
VE	5470.0		5470.0	mm^3	Core volume
BOBBIN	PQ2620		PQ2620		Bobbin
AW	31.00		31.00	mm^2	Window area of the bobbin
BW	9.00		9.00	mm	Bobbin width
MARGIN	0.0		0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
PRIMARY WINDING					
NPRIMARY			45		Primary turns
BPEAK			3505	Gauss	Peak flux density
BMAX			3134	Gauss	Maximum flux density
BAC			643	Gauss	AC flux density
ALG			435	nH/turns^2	Typical gapped core effective inductance
LG			0.322	mm	Core gap length
LAYERS_PRIMARY	3		3		Number of primary layers
AWG_PRIMARY			24	AWG	Primary winding wire AWG
OD_PRIMARY_INSULATED			0.577	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.511	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			395	Cmil/A	Primary winding wire CMA
SECONDARY WINDING					
NSECONDARY	7		7		Secondary turns
AWG_SECONDARY			19	AWG	Secondary winding wire AWG
OD_SECONDARY_INSULATED			1.217	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.912	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			227	Cmil/A	Secondary winding wire CMA
BIAS WINDING					
NBIAS			5		Bias turns
PRIMARY COMPONENTS SELECTION					
Line undervoltage					
BROWN-IN REQURED			76.5	V	Required AC RMS line voltage brown-in threshold
RLS			4.52	MΩ	Connect two 2.26 MOhm resistors to the V-pin for the required UV/OV threshold
BROWN-IN ACTUAL			77.0	V	Actual AC RMS brown-in threshold
BROWN-OUT ACTUAL			70.6	V	Actual AC RMS brown-out threshold
Line overvoltage					
OVERVOLTAGE_LINE			339.2	V	Actual AC RMS line over-voltage threshold

Bias diode					
VBIAS			12.0	V	Rectified bias voltage
VF_BIAS			0.70	V	Bias winding diode forward drop
VREVERSE_BIASDIODE			53.49	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS			22	uF	Bias winding rectification capacitor
CBPP			4.70	uF	BPP pin capacitor
SECONDARY COMPONENTS					
RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
RFB_LOWER			7.15	kΩ	Lower feedback resistor
CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
MULTIPLE OUTPUT PARAMETERS					
OUTPUT 1					
VOUT1			19.00	V	Output 1 voltage
IOUT1	3.40		3.40	A	Output 1 current
POUT1			64.60	W	Output 1 power
IRMS_SECONDARY1			5.68	A	Root mean squared value of the secondary current for output 1
IRIPPLE_CAP_OUTPUT1			4.56	A	Current ripple on the secondary waveform for output 1
AWG_SECONDARY1			19	AWG	Wire size for output 1
OD_SECONDARY1_INSULATED			1.217	mm	Secondary winding wire outer diameter with insulation for output 1
OD_SECONDARY1_BARE			0.912	mm	Secondary winding wire outer diameter without insulation for output 1
CM_SECONDARY1			1137	Cmils	Bare conductor effective area in circular mils for output 1
NSECONDARY1			7		Number of turns for output 1
VREVERSE_RECTIFIER1			77.08	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
SRFET1	Auto		SIR804DP		SRFET selection for output 1
VF_SRFET1			0.035	V	SRFET on-time drain voltage for output 1
VBREAKDOWN_SRFET1			100	V	SRFET breakdown voltage for output 1
RDSON_SRFET1			10.3	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
TOLERANCE ANALYSIS					
CORNER_VAC			90	V	Input AC RMS voltage corner to be evaluated
CORNER_ILIMIT	TYP		1.85	A	Current limit corner to be evaluated
CORNER_LPRIMARY	TYP		880.4	uH	Primary inductance corner to be evaluated
MODE_OPERATION			CCM		Mode of operation
KP			0.509		Measure of continuous/discontinuous mode of operation
FSWITCHING			66266	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
DUTYCYCLE			0.572		Steady state duty cycle
TIME_ON			8.63	us	Primary MOSFET on-time
TIME_OFF			6.46	us	Primary MOSFET off-time
IPEAK_PRIMARY			1.76	A	Primary MOSFET peak currrent
IPEDESTAL_PRIMARY			0.86	A	Primary MOSFET current pedestal
IAVERAGE_PRIMARY			0.75	A	Primary MOSFET average current
IRIPPLE_PRIMARY			0.90	A	Primary MOSFET ripple current
IRMS_PRIMARY			1.01	A	Primary MOSFET RMS current
CMA_PRIMARY			399	Cmil/A	Primary winding wire CMA
BPEAK			3061	Gauss	Peak fux density
BMAX			2846	Gauss	Maximum flux density

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11 Performance Data

11.1 Efficiency vs. Line at Full Load

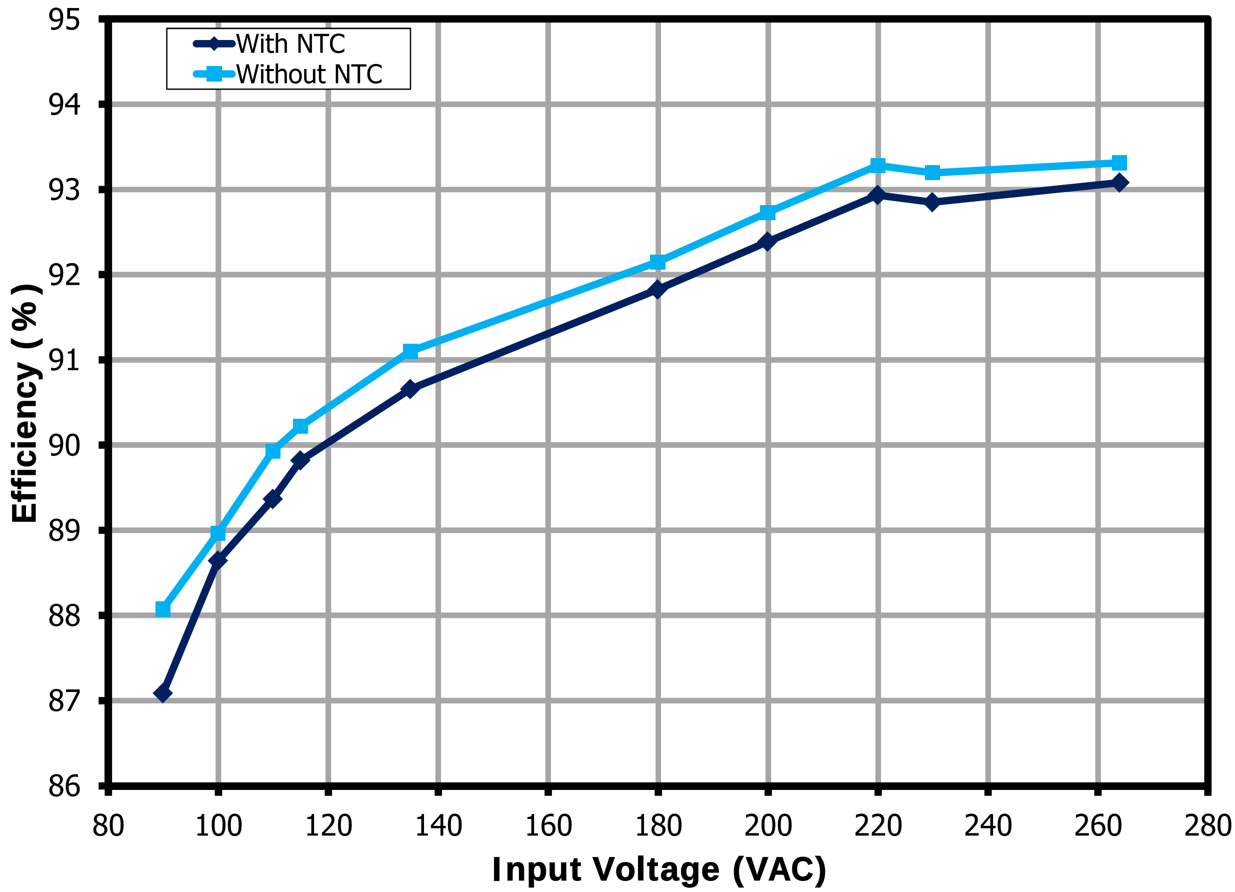

Figure 11 – Efficiency vs. Line Voltage, Room Temperature.

11.2 Efficiency vs. Line at 10 % - 100 % Load

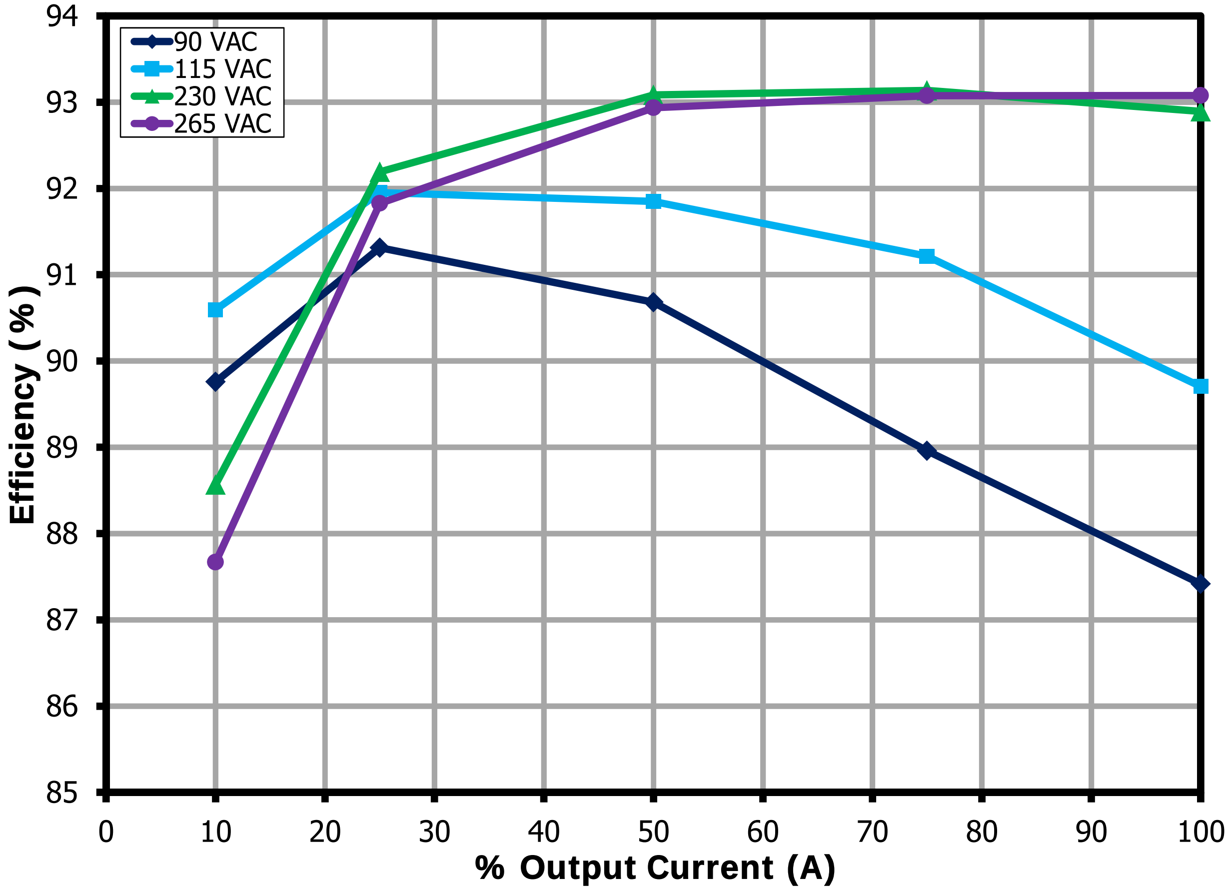

Figure 12 – Efficiency vs. Load, Room Temperature.

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11.3 Average Efficiency

Requirement	
Average	88% (DOE6) 89% (CoC)
10%	79%

11.3.1 115 VAC Input

% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	114.93	1.10	72.01	19.06	3.39	64.60	89.7%	
75%	114.94	0.86	53.47	19.11	2.55	48.77	91.2%	
50%	114.96	0.60	35.33	19.15	1.70	32.45	91.9%	
25%	114.97	0.33	17.48	19.18	0.84	16.07	92.0%	**91.2%**
10%	114.98	0.15	6.98	19.17	0.33	6.33	**90.6%**	

11.3.2 230 VAC Input

% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	229.89	0.67	69.75	19.10	3.39	64.79	92.9%	
75%	229.90	0.52	52.37	19.13	2.55	48.78	93.1%	
50%	229.90	0.37	34.88	19.16	1.70	32.47	93.1%	
25%	229.91	0.21	17.48	19.19	0.84	16.12	92.2%	**92.8%**
10%	229.91	0.09	7.10	19.17	0.33	6.29	**88.6%**	

11.4 No-Load Input Power

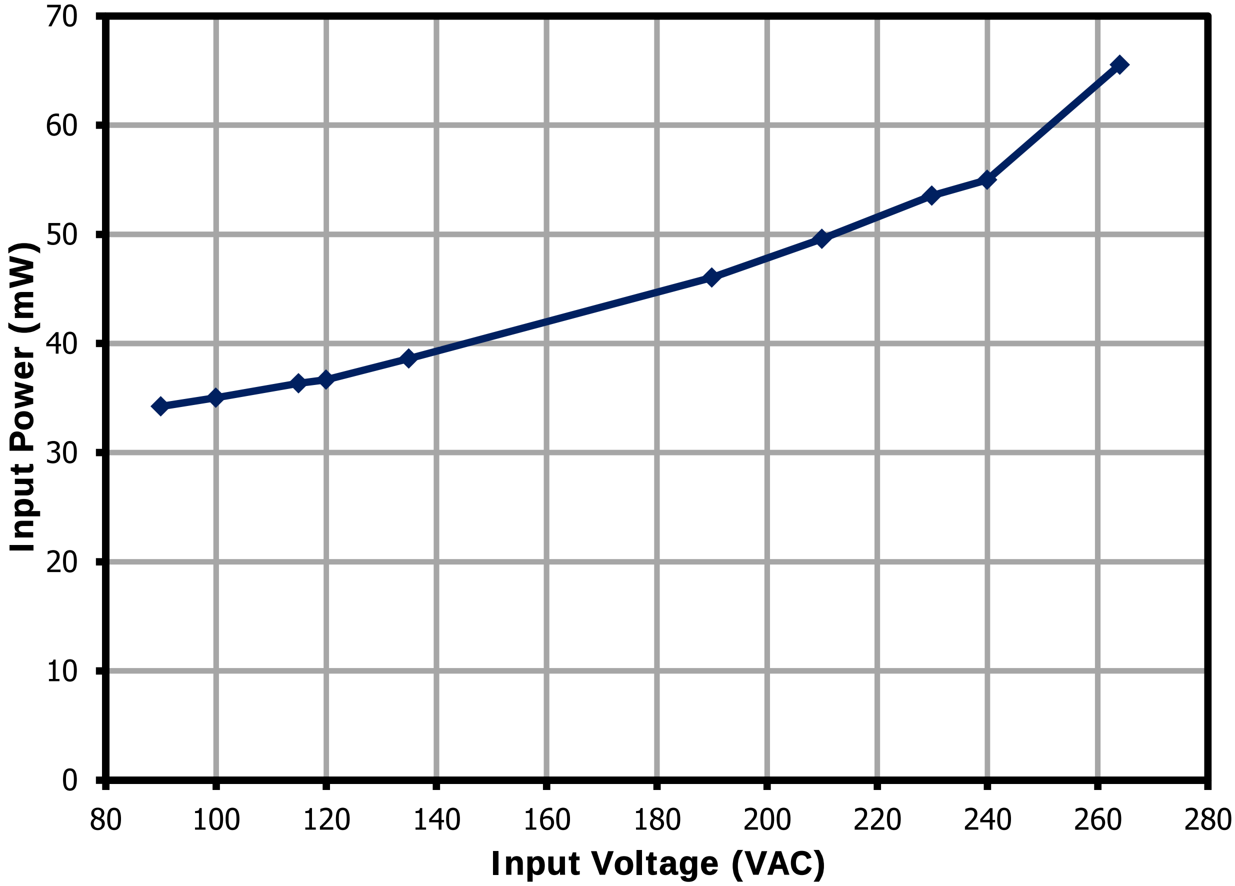

Figure 13 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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11.5 Load Regulation

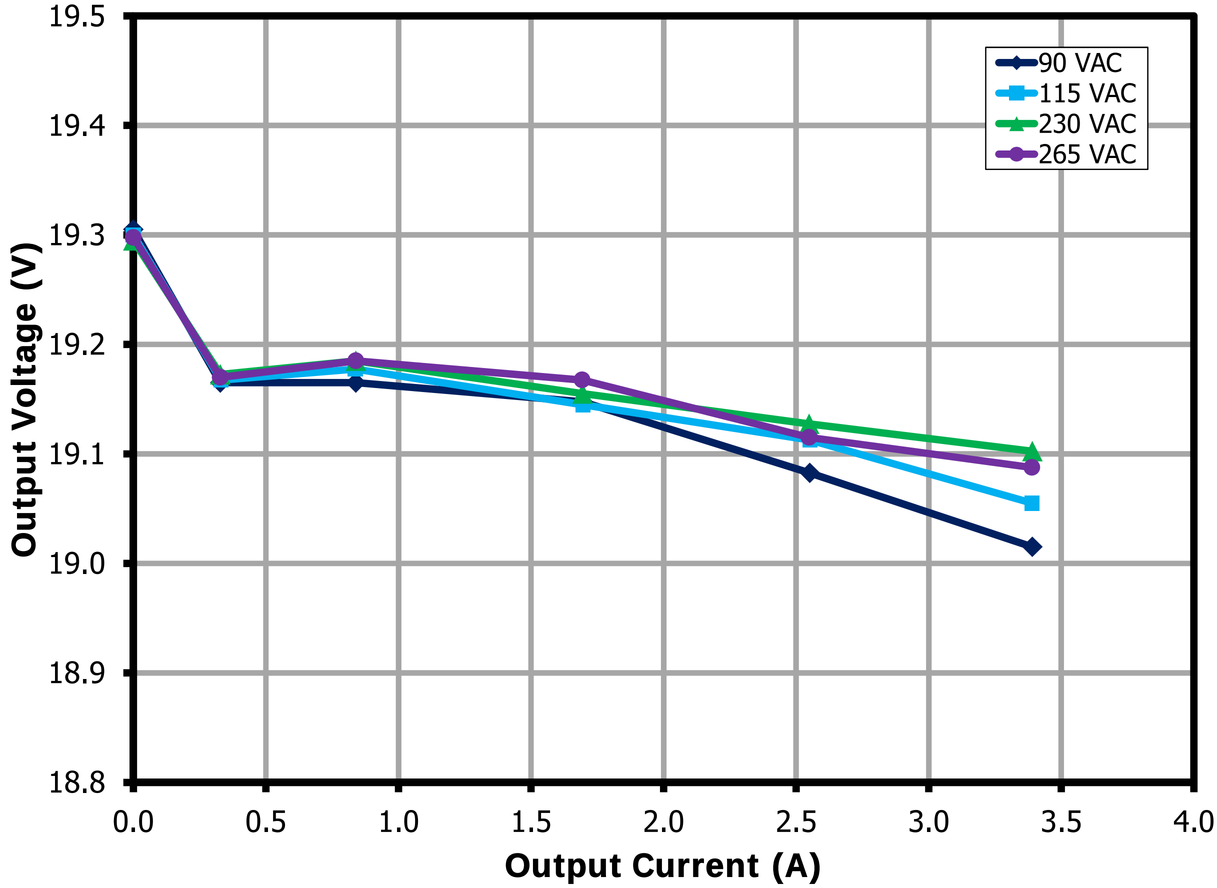

Figure 14 – Output voltage vs. Load, Room Ambient.

11.6 Line Regulation at Full Load

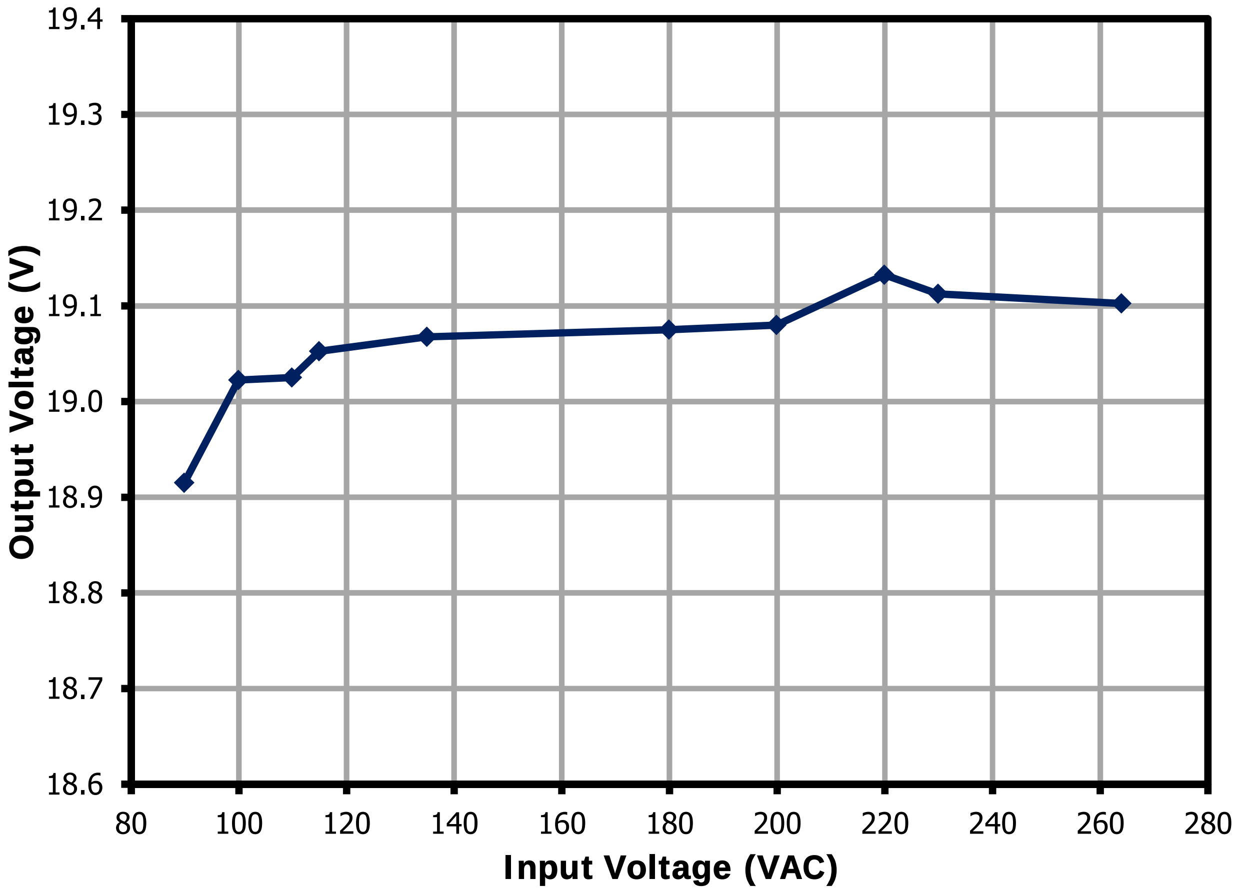

Figure 15 – Output voltage vs. Line, Room Ambient.

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12 Thermal Performance

12.1 90 VAC, 3.4 A Load

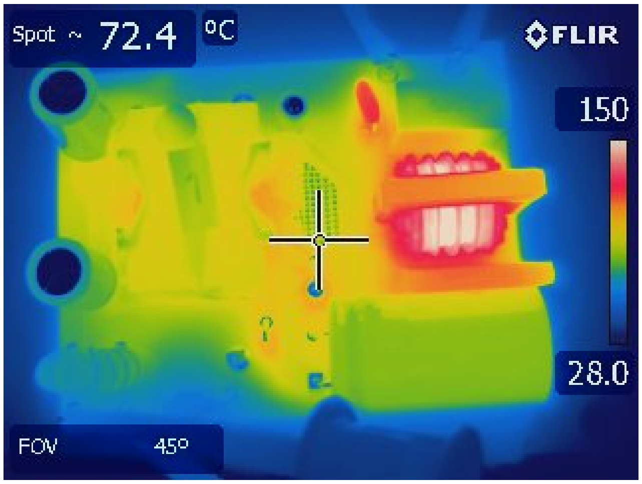

Figure 16 – Transformer Side. 90 VAC, Full Load.

	Reference	°C
Ambient		30
Transformer Core	T1	82.3
Input Capacitor	C2	73
CMC Core	L1	94
Clamp Diode	D1	85
Bridge Rectifier	BR1	99

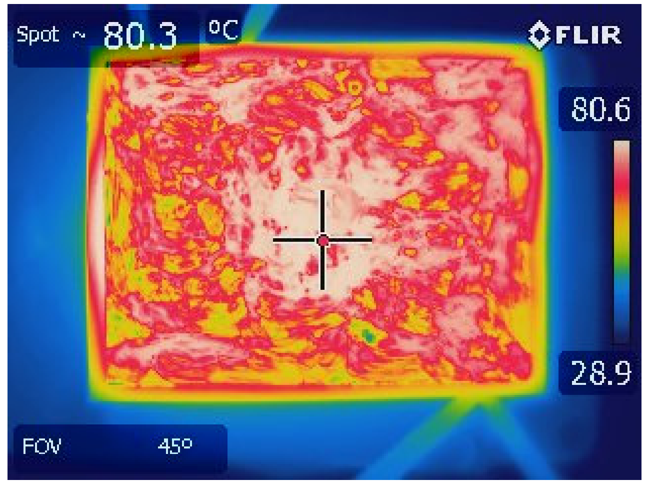

Figure 17 – InnoSwitch3-CE Side. 90 VAC, Full Load.

	Reference	°C
Ambient		30.9
Heat Spreader		80.3
INN3168C (TC)	U1	92.5
SR FET (TC)	Q1	94.7

- TC : Thermal coupler measurement

12.2 115 VAC, 3.4 A Load

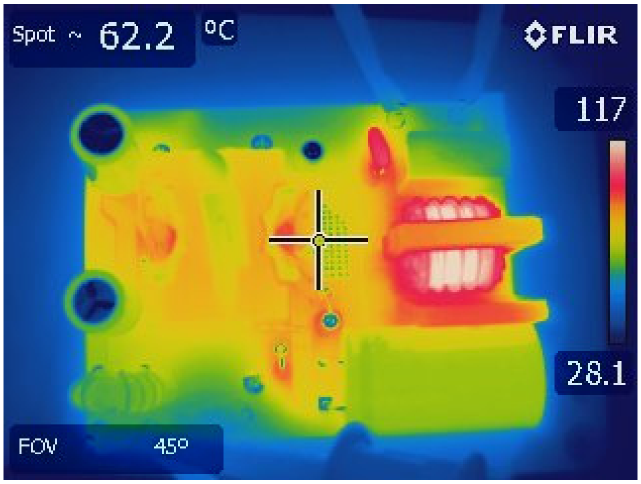

Figure 18 – Transformer Side. 115 VAC, Full Load.

	Reference	°C
Ambient		29.5
Transformer	T1	74.6
Input Capacitor	C2	64.9
CMC Core	L1	77.3
Clamp Diode	D1	78.7
Bridge Rectifier	BR1	82.7

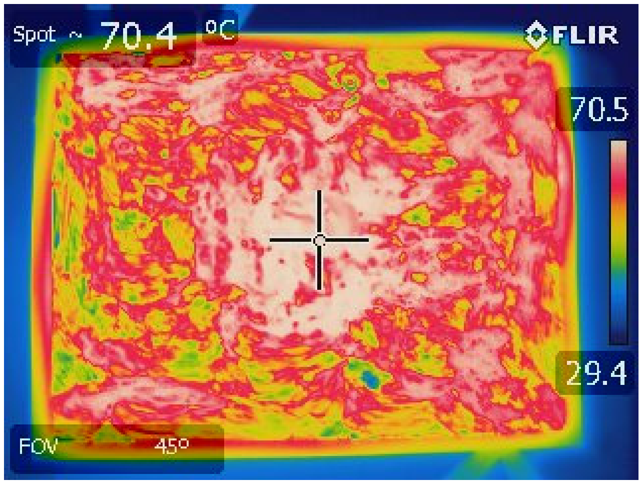

Figure 19 – InnoSwitch3-CE Side. 115 VAC, Full Load.

	Reference	°C
Ambient		31.0
Heat Spreader		71.6
INN3168C (TC)	U1	79.5
SR FET (TC)	Q1	83.3

- TC : Thermal coupler measurement

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12.3 230 VAC, 3.4 A Load

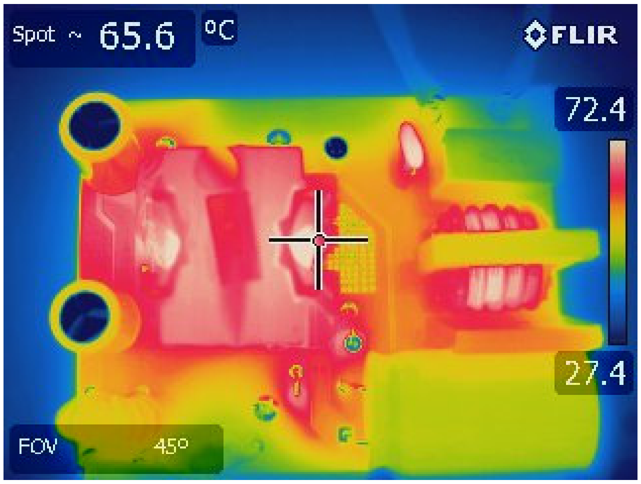

Figure 20 – Transformer Side. 230 VAC, Full Load.

	Reference	°C
Ambient		28.9
Transformer Core	T1	67.9
Input Capacitor	C2	50.8
CMC Core	L1	53.8
Clamp Diode	D1	65.3
Bridge Rectifier	BR1	62.9

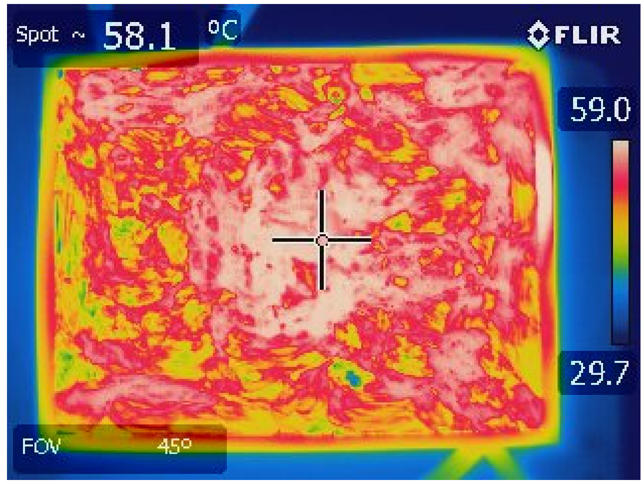

Figure 21 – InnoSwitch3-CE Side. 230 VAC, Full Load.

	Reference	°C
Ambient		30.1
Heat Spreader		59.5
INN3168C (TC)	U1	64.2
SR FET (TC)	Q1	83.3

- TC : Thermal coupler measurement

12.4 265 VAC, 3.4 A Load

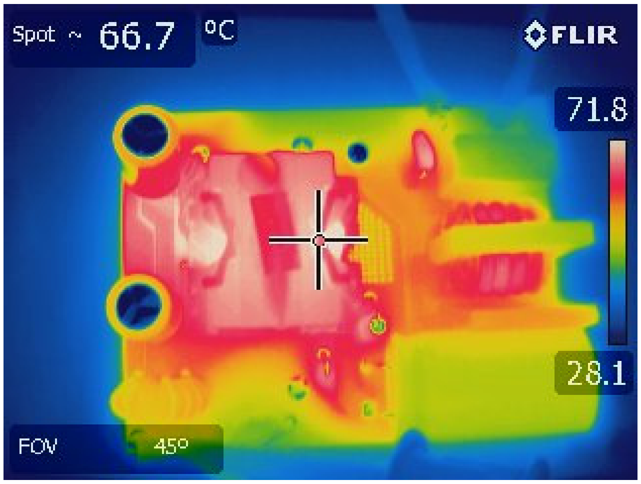

Figure 22 – Transformer Side. 265 VAC, Full Load.

	Reference	°C
Ambient		29.2
Transformer Core	T1	69.7
Input Capacitor	C2	49.7
CMC Core	L1	50.5
Clamp Diode	D1	65.2
Bridge Rectifier	BR1	56.8

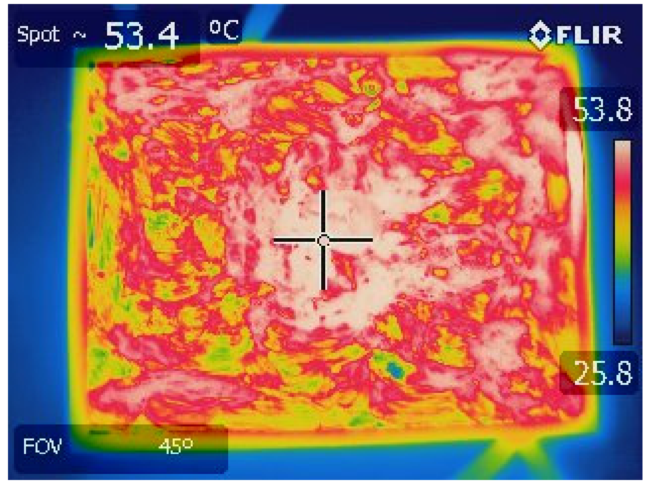

Figure 23 – InnoSwitch3-CE Side. 265 VAC, Full Load.

	Reference	°C
Ambient		29.8
Heat Spreader		59.8
INN3168C (TC)	U1	64.1
SR FET (TC)	Q1	73.3

- TC : Thermal coupler measurement

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13 Waveforms

13.1 Load Transient Response

13.1.1 Load Transient

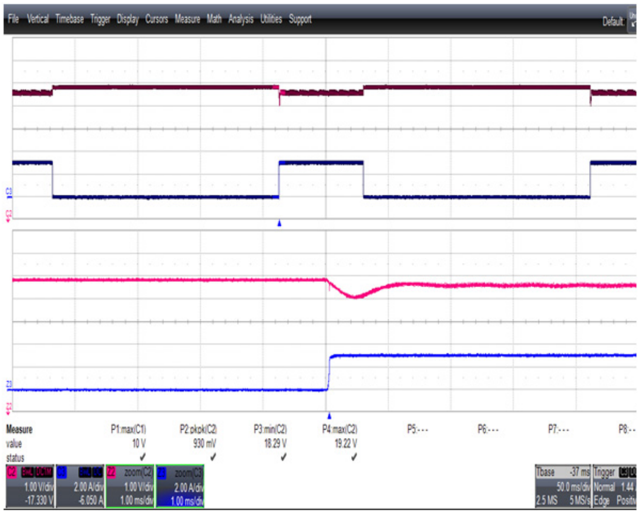

Figure 24 – 0 A – 3.1 A, Load Step Transient Response, 90 VAC.
V_{MIN}: 18.3 V, V_{MAX}: 19.3V.
Upper: V_{OUT}, 1 V / div.
Lower: Load, 2 A, 50 ms, 1 ms / div.

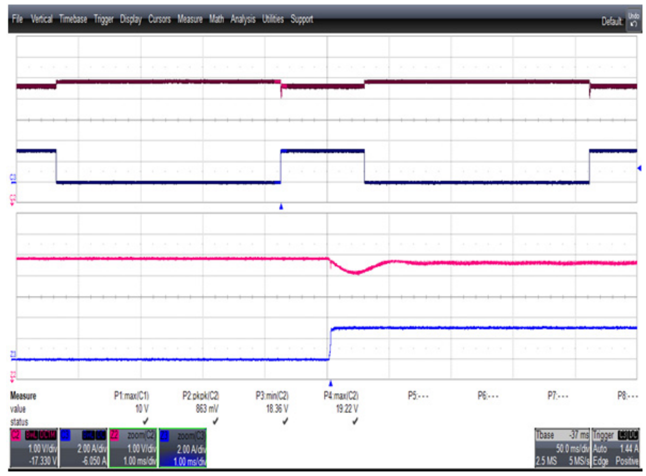

Figure 25 – 0 A – 3.1 A, Load Step Transient Response, 115 VAC.
V_{MIN}: 18.4 V, V_{MAX}: 19.2 V.
Upper: V_{OUT}, 1 V / div.
Lower: Load, 2 A, 50 ms, 1 ms / div.

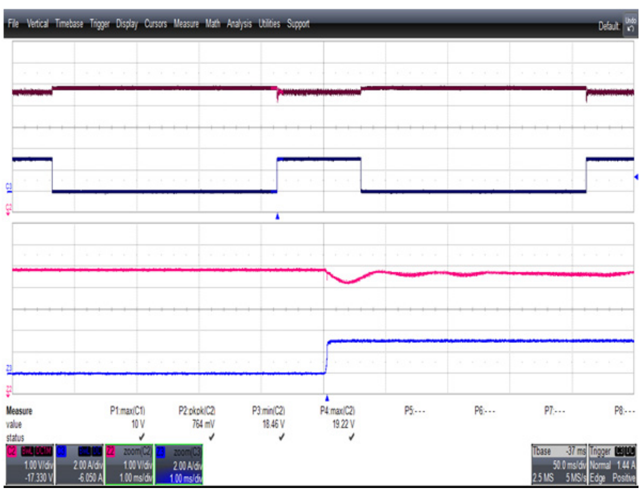

Figure 26 – 0 A – 3.1 A, Load Step Transient Response, 230 VAC.
V_{MIN}: 18.5 V, V_{MAX}: 19.2 V.
Upper: V_{OUT}, 1 V / div.
Lower: Load, 1 A, 50 ms, 1 ms / div.

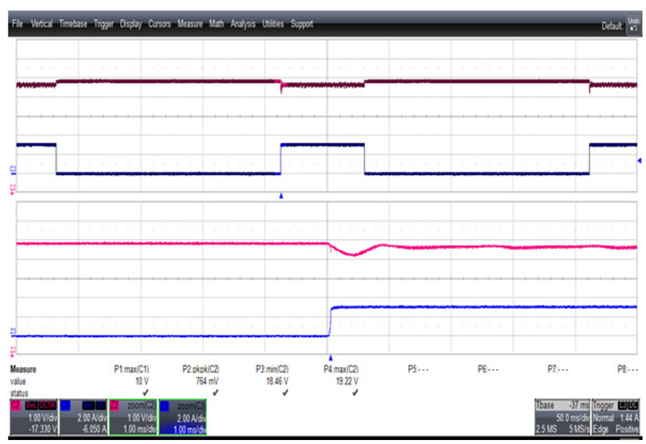

Figure 27 – 0 A – 3.1 A, Load Step Transient Response, 265 VAC.
V_{MIN}: 18.5 V, V_{MAX}: 19.2 V.
Upper: V_{OUT}, 1 V / div.
Lower: Load, 1 A, 50 ms, 1 ms / div.

13.2 Switching Waveforms

13.2.1 INN3168C Drain and Current Waveforms

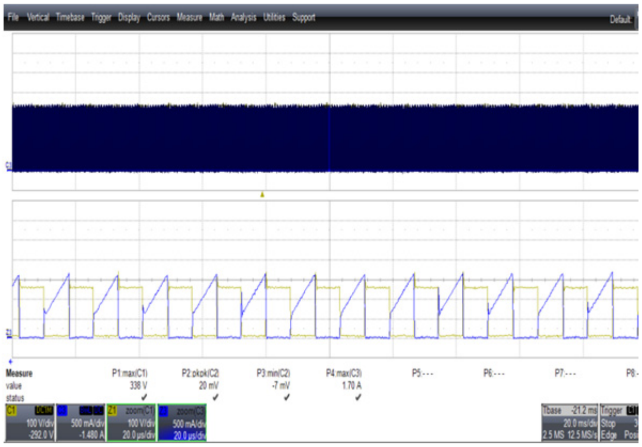

Figure 28 – Drain Voltage and Current Waveforms.
90 VAC Input, Full Load.
Upper: I_{DRAIN}, 1 A , 20 ms, 20 μs / div.
Lower: V_{DRAIN}, 100 V.

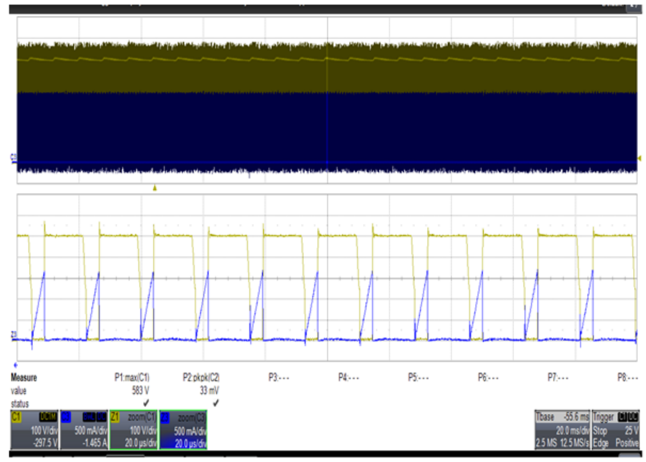

Figure 29 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (583 V_{MAX}).
Upper: I_{DRAIN}, 0.5 A, 20 ms, 20 μs / div.
Lower: V_{DRAIN}, 100 V.

13.2.2 INN3168C Drain and Current Waveforms Start-up

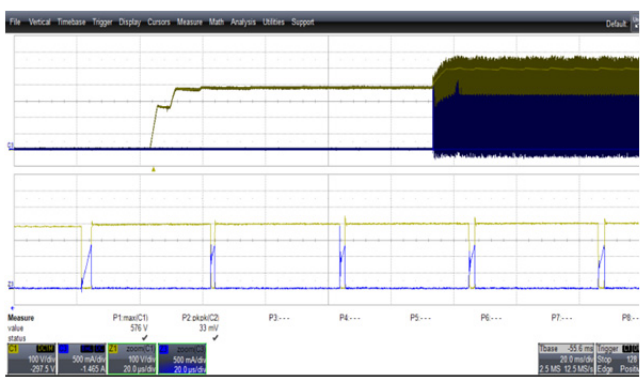

Figure 30 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (576 V_{MAX}).
Upper: I_{DRAIN}, 1 A, 20 ms, 20 μs / div.
Lower: V_{DRAIN}, 100 V.

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13.2.3 SR FET Waveforms

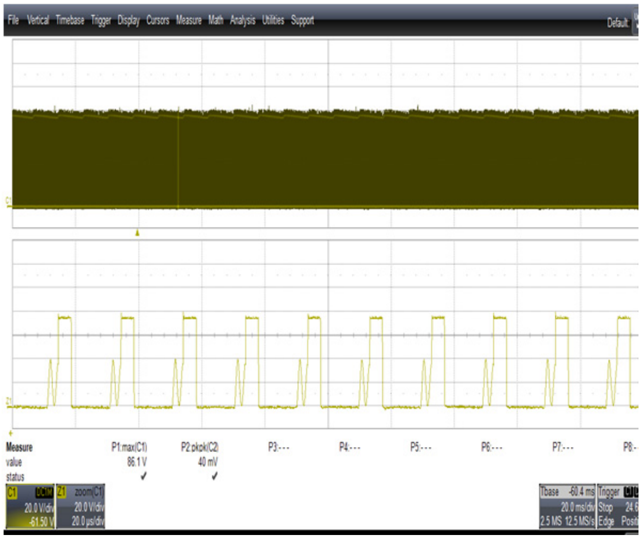

Figure 31 – SR FET Voltage Waveforms.
265 VAC Input, Full Load.
(86.1 V_{MAX} for SR FET.)
V_{DS}: 20 V / 10 ms, 20 μs / div.

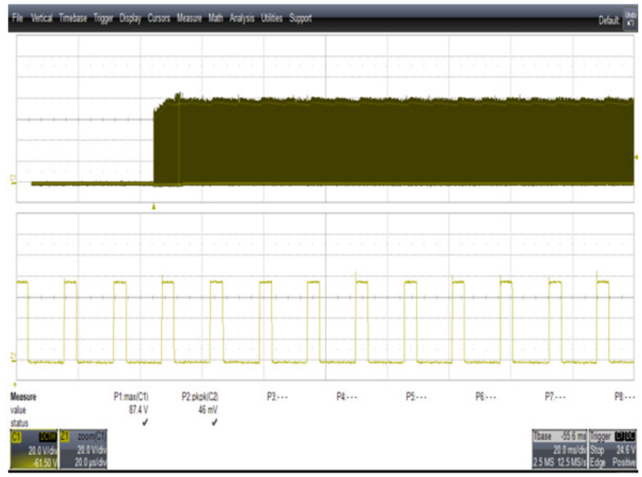

Figure 32 – During start up SR FET Waveforms
265 VAC Input, Full Load.
(87.4 V_{MAX} for SR FET.)
V_{DS}: 20 V /, 20 ms, 20 μs / div.

Hold up time (> 5 ms at 115 VAC)

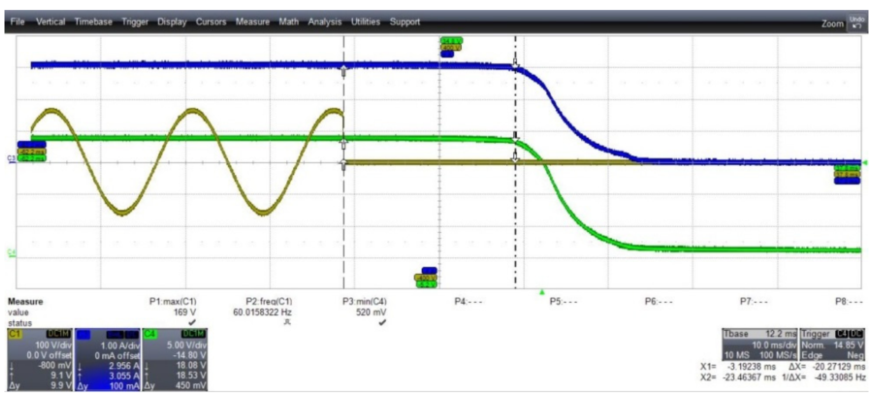

Figure 33 – Input Voltage and Output Voltage Waveforms.
110 VAC Input, Full Load (Hold-up Time = 20.2 ms).
Upper: I_{OUT}, 1 A, 10 ms / div
Middle: V_{INPUT}, 100 V.
Lower: V_{OUT}, 5 V.

13.2.4 Output Voltage and Current Waveforms at Start-up

13.2.4.1 Full Load (3.25 A)

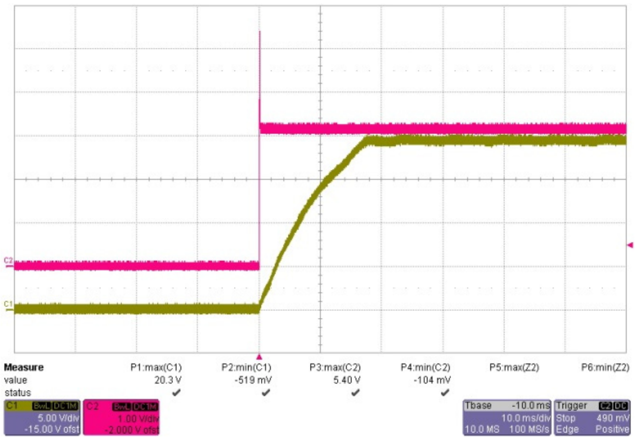

Figure 34 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: I_{OUT}, 1 A, 10 ms / div.
Lower: V_{OUT}, 5 V / div.

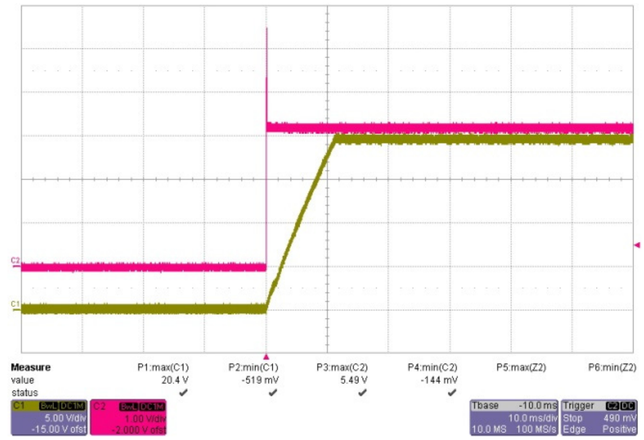

Figure 35 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: I_{OUT}, 1 A, 10 ms / div.
Lower: V_{OUT}, 5 V.

13.2.4.2 No-Load

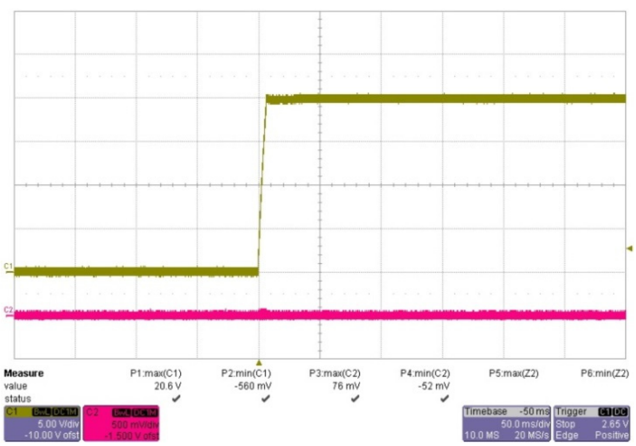

Figure 36 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: V_{OUT}, 5 V / div.
Lower: I_{OUT}, 0.5 A, 50 ms / div.

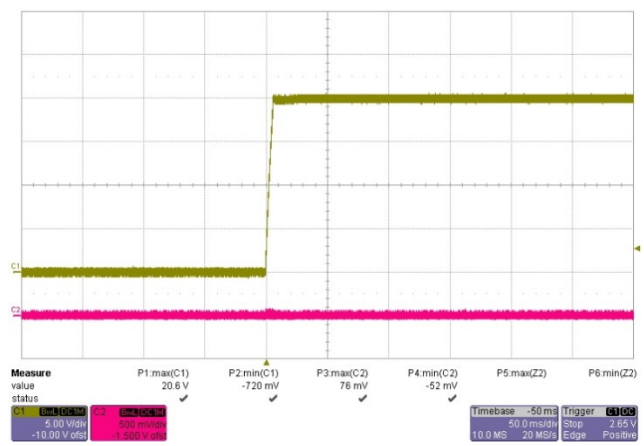

Figure 37 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: V_{OUT} , 5 V / div.
Lower: I_{OUT}, 0.5 A, 50 ms / div.

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13.2.5 Output Voltage and Current Waveforms with Shorted Output

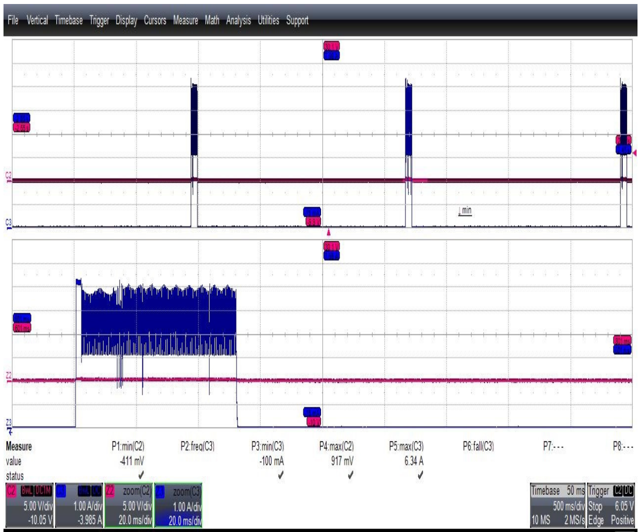

Figure 38 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: V_{OUT}, 5 V.
Lower: I_{OUT}, 1 A, 0.5 s, 20 ms / div.

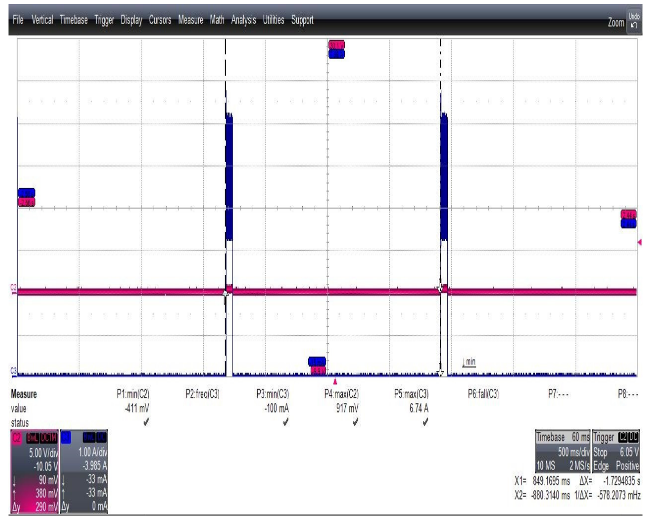

Figure 39 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: V_{OUT}, 5 V.
Lower: I_{OUT}, 1 A, 0.5 s / div.

13.2.6 Output Voltage and Current Waveforms with Open 5 V Feedback

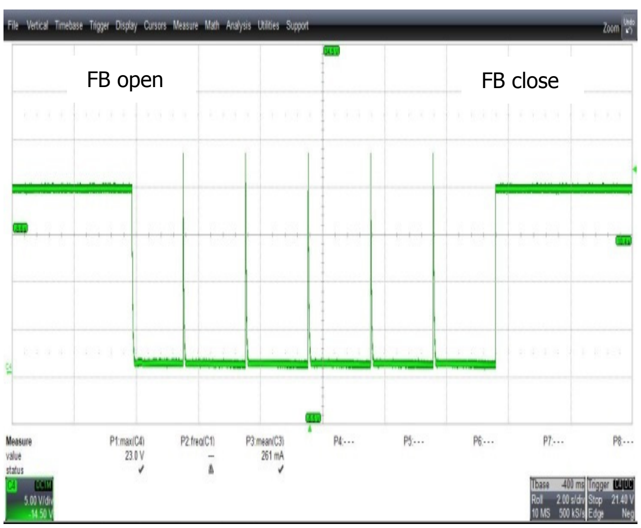

Figure 40 – Output Voltage Waveform.
90 VAC Input. (OVP = 23 V.)
V_{OUT}: 5 V, 2 s / div..

Figure 41 – Output Voltage Waveform.
265 VAC Input. (OVP = 23 V.)
V_{OUT}: 5 V , 2 s / div.

13.3 Output Ripple Measurements

13.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/100 V ceramic type and one (1) 10 μF/100 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

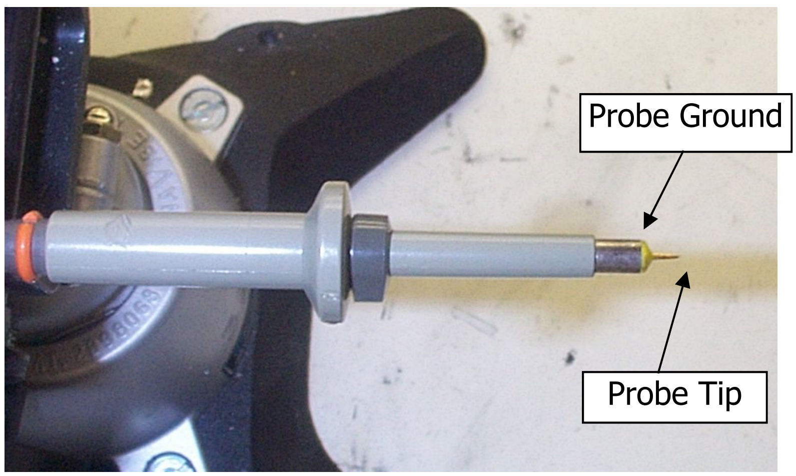

Figure 42 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

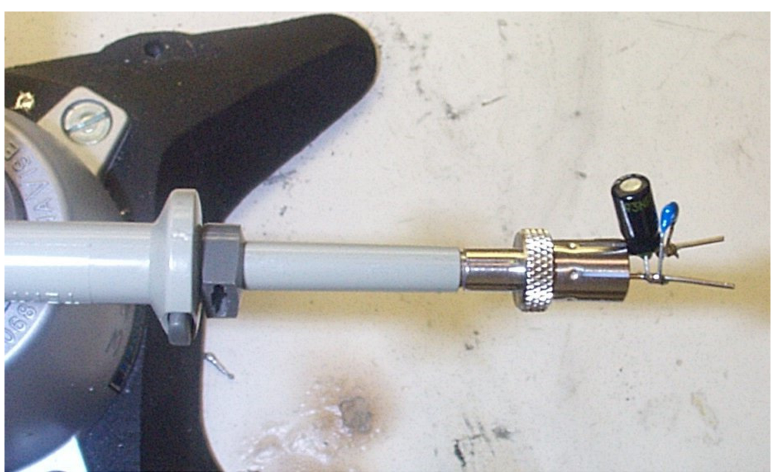

Figure 43 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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13.3.2 Ripple Voltage Waveforms

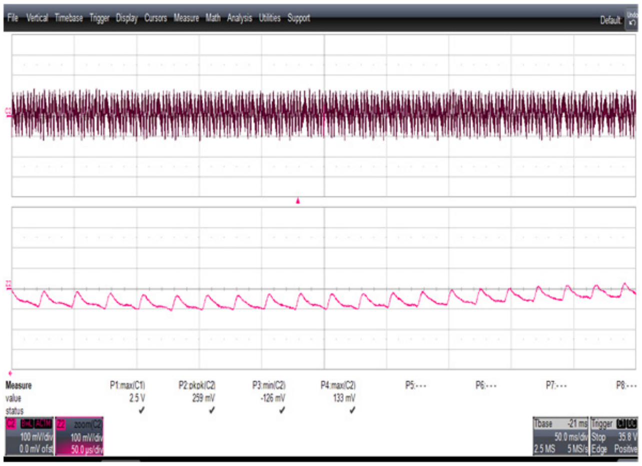

Figure 44 – Output Voltage Ripple Waveform.
90 VAC Input, 2 A Load, 259 mV_{P-P}.
V_{OUT}: 100 mV, 50 ms, 50 µs / div.

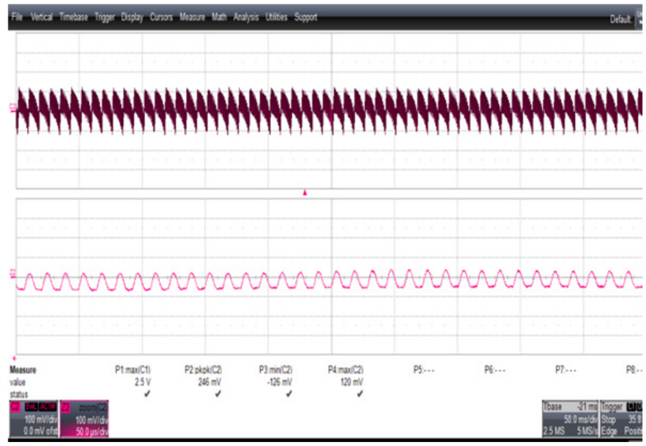

Figure 45 – Output Ripple Voltage Waveform.
90 VAC Input. 3.4 A Load, 246 mV_{P-P}.
V_{OUT}: 100 mV, 50 ms, 50 µs / div.

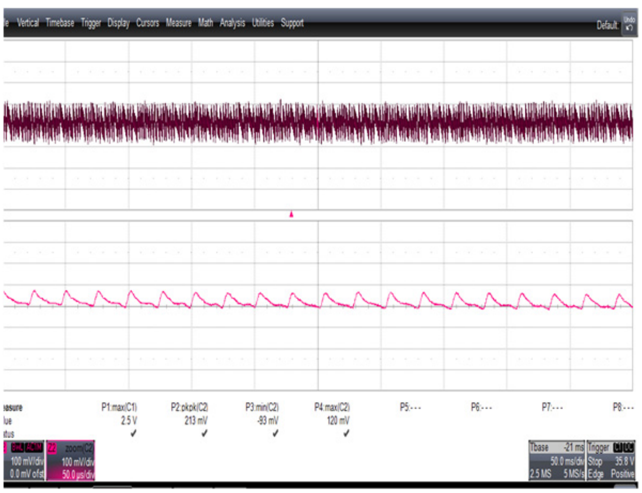

Figure 46 – Output Voltage ripple Waveform
115 VAC Input, 2 A Load, 213 mV_{P-P}.
V_{OUT}: 100 mV, 50 ms, 50 µs / div.

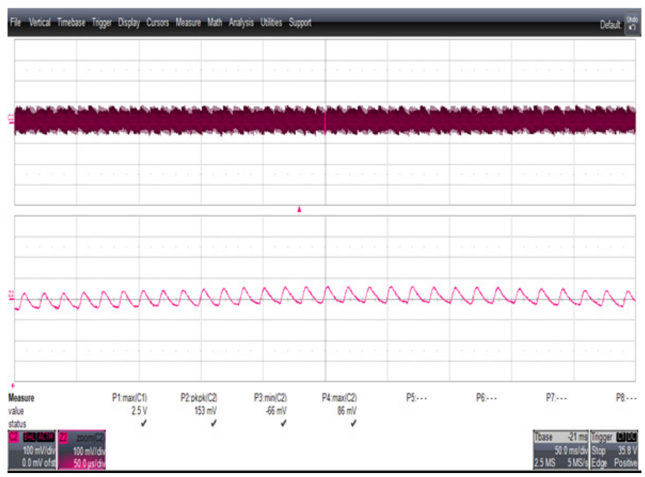

Figure 47 – Output Ripple Voltage Waveform
115 VAC Input. 3.4 A Load, 153 mV_{P-P}.
V_{OUT}: 100 mV, 50 ms, 50 µs / div.

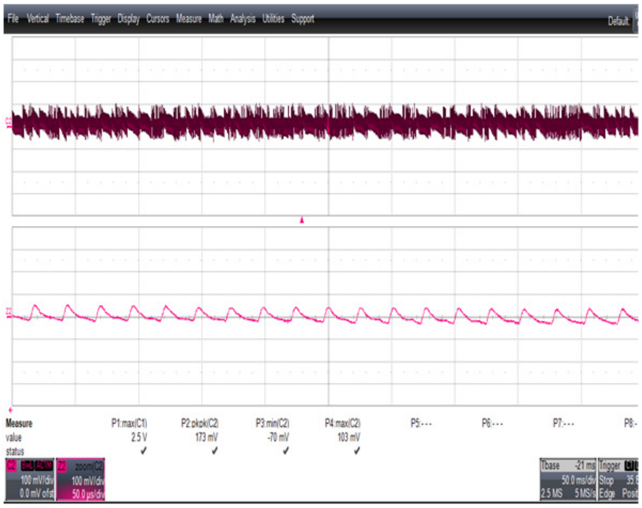

Figure 48 – Output Voltage Ripple Waveform.
230 VAC Input, 2 A Load, 173 mV_{P-P}.
V_{OUT}: 100 mV, 50 ms , 50 µs / div.

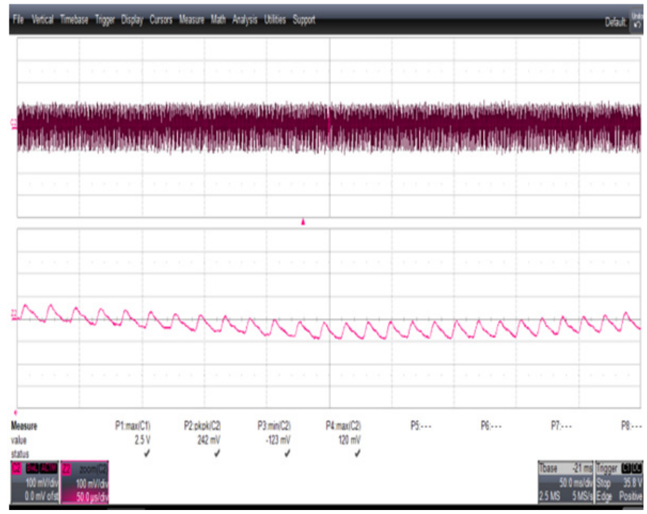

Figure 49 – Output Ripple Voltage Waveform.
230 VAC Input. 3.4 A Load, 242 mV_{P-P}.
V_{OUT}: 100 mV, 50 ms , 50 µs / div.

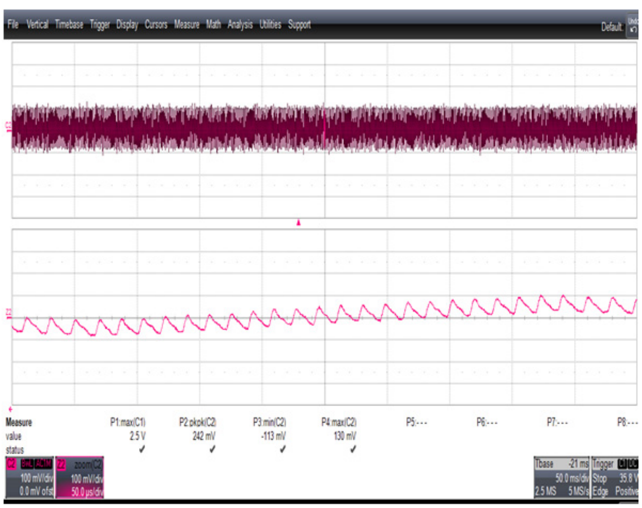

Figure 50 – Output Voltage Ripple Waveform.
265 VAC Input, 2 A Load, 242 mV_{P-P}.
V_{OUT}: 100 mV, 50 ms , 50 µs / div.

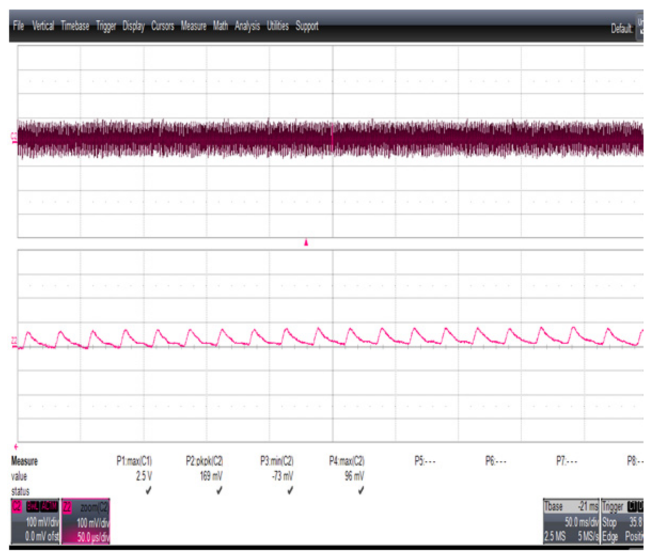

Figure 51 – Output Ripple Voltage Waveform.
265 VAC Input. 3.4 A Load, 169 mV_{P-P}.
V_{OUT}: 100 mV, 50 ms , 50 µs / div.

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13.4 Line Undervoltage and Overvoltage (DC Input)

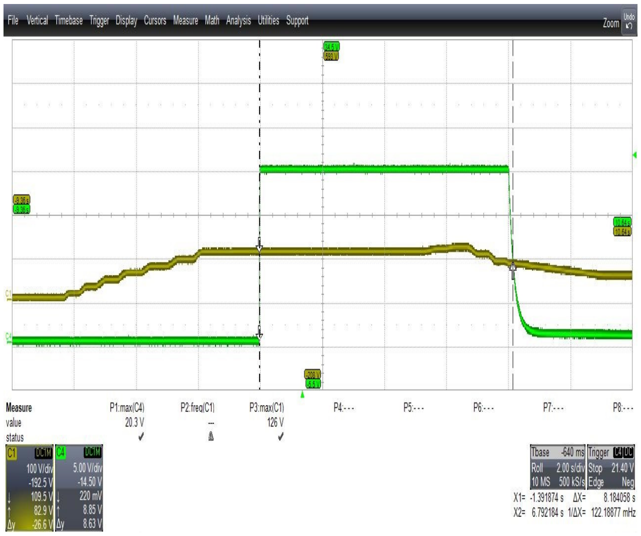


Figure 52 – Line Undervoltage.
DC Input, No-Load.
V_{UV+}: 109.5 V, V_{UV-}: 82.9 V.
Upper: Input, 100 V.
Lower: V_{OUT}, 5 V, 2 s / div.

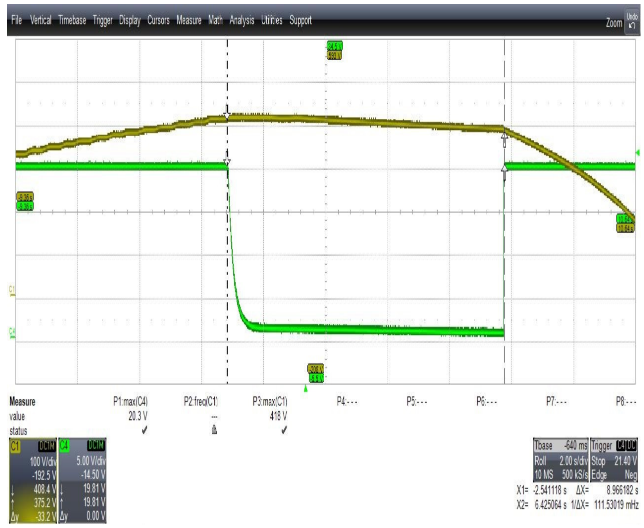


Figure 53 – Line Overvoltage.
DC Input, No-Load.
V_{OV+}: 408.4 V, V_{OV-}: 375.2 V.
Upper: Input, 100 V.
Lower: V_{OUT}, 5 V, 2 s / div.

13.5 Brown-in and Brown-out

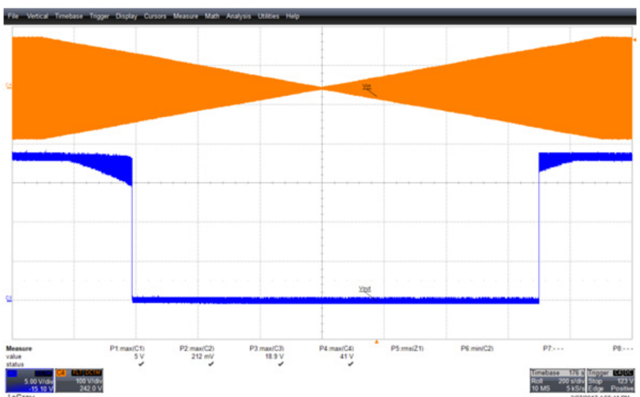


Figure 54 – Brown-in and Brown-out at Full Load.
90 VAC Input and 6 V / Min.
Upper: Input, 100 V.
Lower: V_{OUT}, 5 V, 200 s / div.

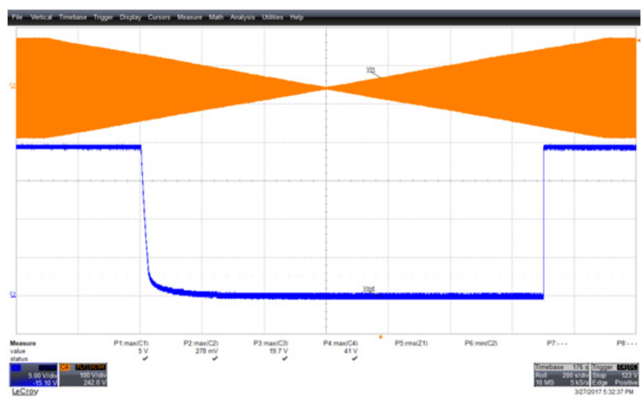
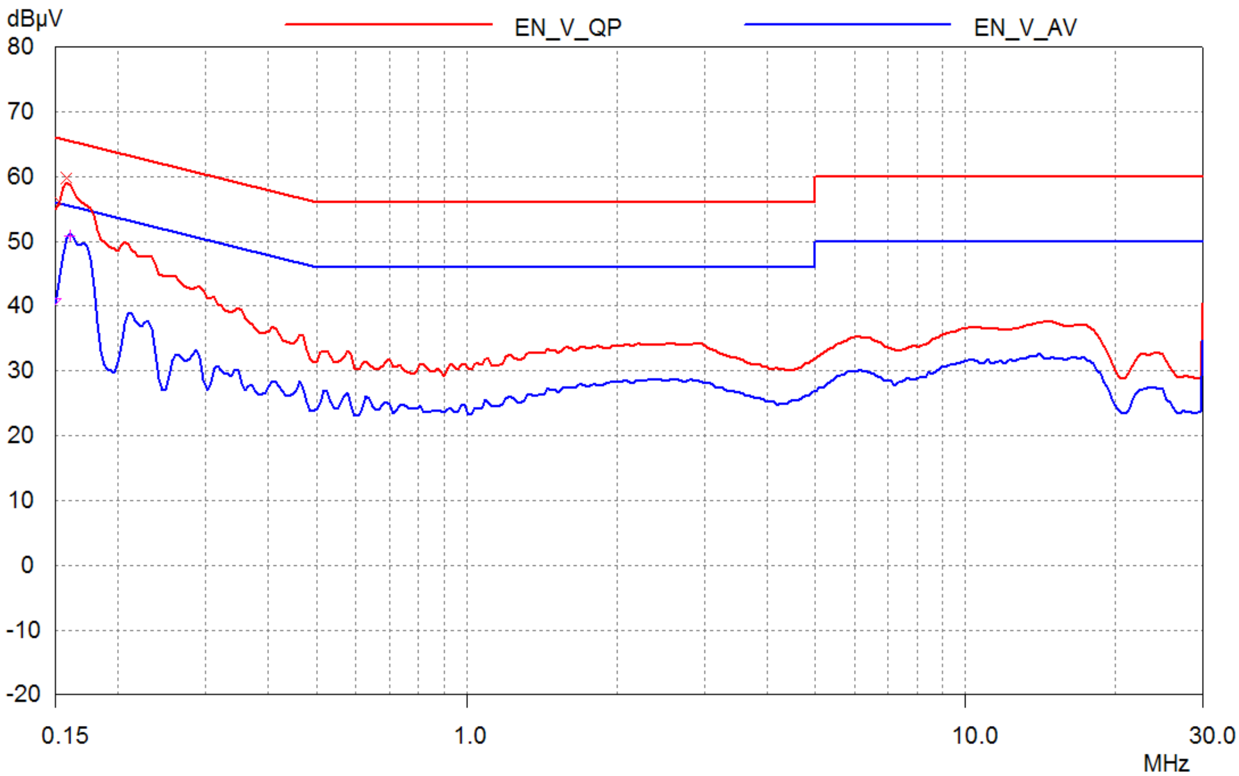


Figure 55 – Brown-in and Brown-out at No-Load.
90 VAC Input and 6 V / Min.
Upper: Input, 100 V.
Lower: V_{OUT}, 5 V, 200 s / div

14 Conductive EMI with Earth Grounded Output

14.1 110 VAC Input



	Freq (MHz)	Measurement (dBuV)	Limit (dBuV)	Margin (dBuV)
QP	0.157	59.81	65.6	5.79
Ave	0.160	50.89	55.47	4.58

Figure 56 – Earth Ground at 110 VAC.

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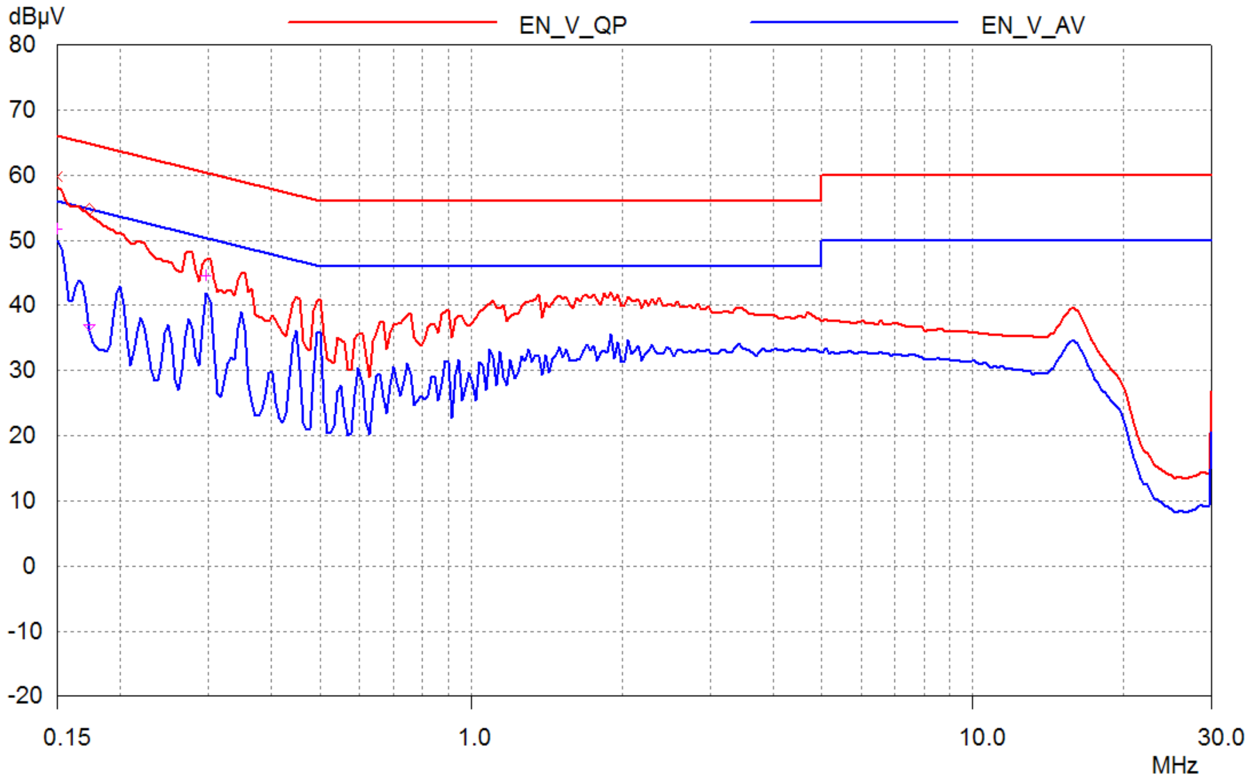
14.2 230 VAC Input



	Freq (MHz)	Measurement (dBuV)	Limit (dBuV)	Margin (dBuV)
Ave	0.15	51.75	56	4.25
Ave	0.29	44.54	50.33	5.79

Figure 57 – Earth Ground a 230 VAC.

15 Lighting Surge Test

15.1 Common Mode Test

Passed ±3.5 kV, Combination test.

Ring Wave Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
3.5	90	12	10	PASS
-3.5	90	12	10	PASS
3.5	270	12	10	PASS
-3.5	270	12	10	PASS

15.2 Differential Mode Test

Passed ±2.5 kV, Combination test.

Differential Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
2.5	90	2	10	PASS
-2.5	90	2	10	PASS
2.5	270	2	10	PASS
-2.5	270	2	10	PASS

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16 ESD Test

Passed ±8 kV contact test.

Contact Voltage (kV)	Applied to	Number of Strikes	Test Result
8	19V	10	PASS
-8	19V	10	PASS
8	RTN	10	PASS
-8	270	10	PASS

Passed ±16.5 kV air test.

Differential Voltage (kV)	Applied to	Number of Strikes	Test Result
16.5	19V	10	PASS
-16.5	19V	10	PASS
16.5	RTN	10	PASS
-16.5	RTN	10	PASS

17 Revision History

Date	Author	Revision	Description & Changes	Reviewed
09-Sep-17	DK	1.0	Initial Release	Apps & Mktg

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