Si5386 Rev E Data Sheet

12-channel, Any Frequency, Wireless Jitter Attenuating Clock

The Si5386 is a high performance, integer and fractional clock generator for wireless applications which demand the highest level of integration and phase noise perform-ance. Based on Silicon Laboratories' 4th generation DSPLL technology, the Si5386 combines frequency synthesis and jitter attenuation in a highly integrated digital sol-ution that eliminates the need for external VCXO and loop filter components. A fixed-frequency crystal that provides frequency stability for free-run and holdover modes is integrated within the package saving valuable PCB space. This all-digital solution provides superior performance that is highly immune to external board disturbances such as power supply noise.

Modern C-RAN remote radio heads and fixed wireless systems require a diverse set of clocks such as ADC/DAC, RF LOs, eCPRI/CPRI, and Ethernet clocks. The Si5386 architecture is designed to deliver high-performance JESD204B DCLK and SYSREF clock pairs and flexible any-rate clocks for non-LTE clocks such as Ether-net and system reference clocks all from a single IC.

Applications:

- Cloud Radio Access Network RRHs
- Small cells
- Fixed wireless
- Wireless base stations
- Active antenna systems
- Distributed antenna systems

KEY FEATURES

- Flexible timing in a single IC
  - Generates any combination of output frequencies from any input frequency
- Input frequency range:
  - Differential: 7.68 MHz to 750 MHz
  - LVCMOS: 7.68 MHz to 250 MHz
- Output frequency range (Integer):
  - Differential: up to 3 GHz
- Output frequency range (fractional):
  - Differential: up to 735 MHz
  - LVCMOS: up to 250 MHz
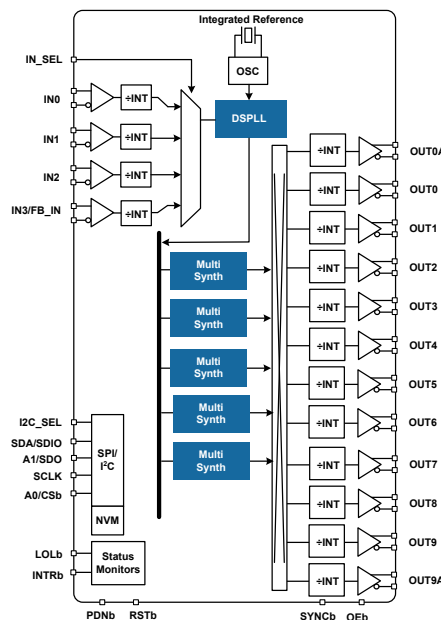- Ultra-low jitter:
  - 80 fs typ (12 kHz–20 MHz)

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1. Features List

The Si5386 Rev. E features are listed below:

- Flexible timing in a single IC
  - Generates any combination of output frequencies from any input frequency
- Input frequency range:
  - Differential: 7.68 MHz to 750 MHz
  - LVCMOS: 7.68 MHz to 250 MHz
- Output frequency range (Integer):
  - Differential: up to 2.94912 GHz with JESD204B support
- Output frequency range (fractional):
  - Differential: up to 735 MHz
  - LVCMOS: up to 250 MHz
- Ultra-low jitter: 80 fs typ (12 kHz–20 MHz)
- Programmable jitter attenuation bandwidth from 1 Hz to 4 kHz
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude from 200 - 3200 mV

- Status monitoring (LOS, OOF, LOL)
- Pin controlled input switching
- DSPLL with special wireless calibration
- Optional zero delay mode
- Hitless input clock switching: automatic or manual
- Automatic free-run and holdover modes
- Fastlock feature
- Glitchless on the fly output frequency changes
- Core voltage:
  - VDD: 1.8 V ±5%
  - VDDA: 3.3 V ±5%
- Independent output clock supply pins: 3.3 V, 2.5 V, or 1.8 V
- Output-output skew: 20 ps typ
- Serial interface: I2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder ProTM software simplifies device configuration
- Temperature range: –40 to +85 °C

2. Ordering Guide

Ordering Part Number (OPN)	Reference	Number of Input/Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis Modes	Package	Temperature Range
Si5386						
Si5386A-E-GM[1, 2]	External Crystal	4/10	0.001 to 2949.12 MHz	Integer and Fractional	64-QFN 9×9 mm	–40 to 85 °C
Si5386E-E-GM[1, 2]	Internal Crystal	4/10	0.001 to 2949.12 MHz	Integer and Fractional	64-LGA 9×9 mm	–40 to 85 °C

Notes:
1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available. Ordering part numbers are assigned by Silicon Labs and the ClockBuilder Pro software utility. Custom part number format is "Si5386E-Exxxxx-GM" where "xxxxx" is a unique numerical sequence representing the preprogrammed configuration.

Si538fg-Rxxxxx-GM

Timing product family

f = 6 (single PLL LTE + Ethernet clock)

g = Device grade A (external crystal), E (integrated 48.0231 MHz crystal)

Product **R**evision (E)*

Custom ordering part number (OPN) sequence ID**

Package, ambient temperature range (QFN, -40°C to +85°C)
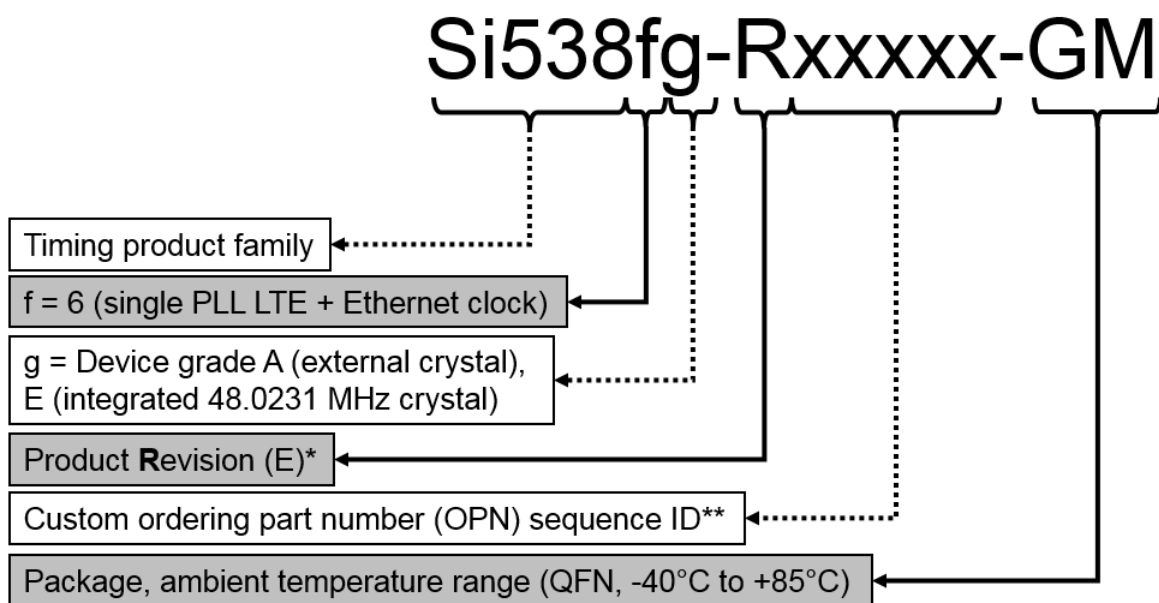
*See Ordering Guide table for current product revision.
** (Optional) 5 digits; assigned by ClockBuilder Pro for Custom, factory-preprogrammed OPN devices only;
(The "xxxxx" field is not included for "Base" OPNs).

Figure 2.1. Ordering Part Number Fields

3. Functional Description

The Si5386's internal DSPLL provides jitter attenuation and any-frequency multiplication of the selected input frequency without the need for external VCXOs or loop filters. Input switching is controlled manually or automatically using an internal state machine. The oscillator circuit (OSC) provides a frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode using the integrated crystal provided inside the Si5386 package. The integrated crystal is not only convenient, but saves valuable PCB area. The high-performance MultiSynthdividers (N) generate integer or fractionally related output frequencies for the output stage. A crosspoint switch connects any of the MultiSynth generated frequencies to any of the outputs. Additional integer division (R) determines the final output frequency. Further, the DSPLL is specially calibrated for ultra-low phase noise when configured for LTE frequencies with JESD204B outputs. This integration provides a clock-tree-on-a-chip solution for applications that need a mix of 4G/LTE and general-purpose frequencies.

3.1 Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (P_n/P_d), fractional frequency multiplication (M_n/M_d), fractional output MultiSynth division (N_n/N_d), and integer output division (R_n) allows the generation of virtually any output frequency on any of the outputs with very low-phase noise suitable for wireless applications when synthesizing LTE frequencies. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

3.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings in the range of 1 Hz to 4 kHz are available for selection. Since the loop bandwidth is controlled digitally, the DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

3.3 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g., 1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings of in the range of 100 Hz to 4 kHz are available for selection. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

3.4 Modes of Operation

Once initialization is complete the DSPLL operates in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in . The following sections describe each of these modes in greater detail.

3.4.1 Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits including the serial interface will be restored to their initial state. A hard reset is initiated using the RSTb pin or by asserting the hard reset register bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.
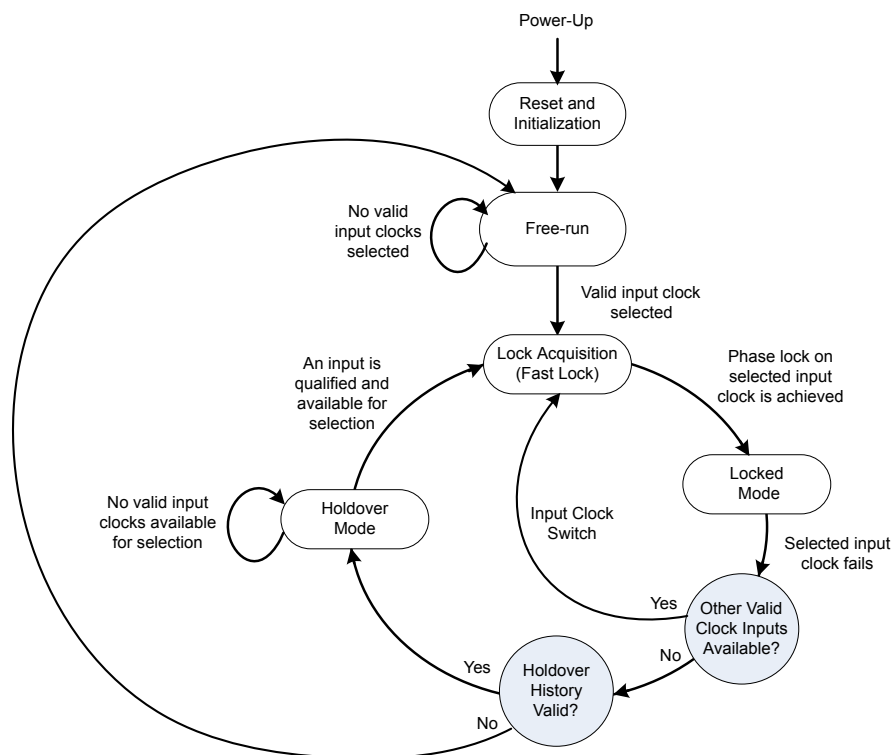
Figure 3.1. Modes of Operation

3.4.2 Freerun Mode

The DSPLL will automatically enter freerun mode once power is applied to the device and initialization is complete. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes.

3.4.3 Lock Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls in to the input clock frequency.

3.4.4 Locked Mode

Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point, any XTAL frequency drift will not affect the output frequency. A loss of lock pin (LOL) and status bit indicate when lock is achieved. See 3.6.4 LOL Detection for more details on the operation of the loss-of-lock circuit.

3.4.5 Holdover Mode

The DSPLL will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.
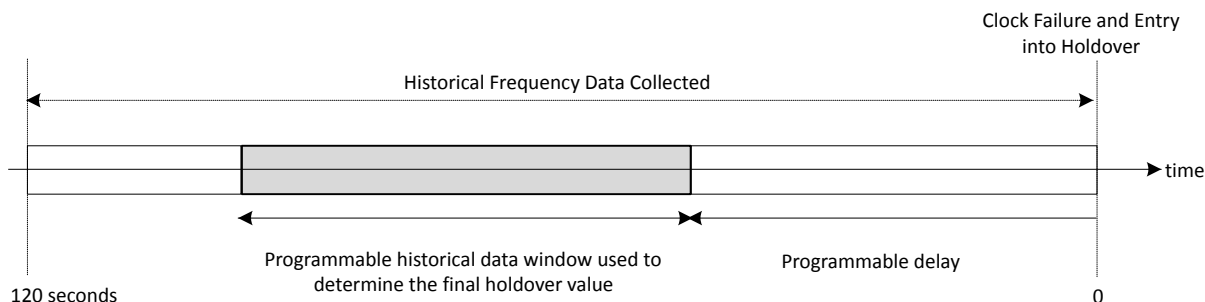
Figure 3.2. Programmable Holdover Window

When entering holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, the DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL or the Fastlock bandwidth.

The DSPLL output frequency when exiting holdover can be ramped (recommended). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching, see 3.5.4 Ramped Input Switching.

Note: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

3.5 Inputs (IN0, IN1, IN2, IN3)

There are four inputs that can be used to synchronize the DSPLL. The inputs accept both differential and single-ended clocks. Input selection can be manual (pin or register controlled) or automatic with user definable priorities.

3.5.1 Manual Input Switching (IN0, IN1, IN2, IN3)

Input clock selection can be made manually using the IN_SEL[1:0] pins or through a register. A register bit determines input selection as pin selectable or register selectable. The IN_SEL pins are selected by default. If there is no clock signal on the selected input, the device will automatically enter free-run or holdover mode. When the zero delay mode is enabled, IN3 becomes the feedback input (FB_IN) and is not available for selection as a clock input.

Table 3.1. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input	
		Zero Delay Mode Disabled	Zero Delay Mode Enabled
0	0	IN0	IN0
0	1	IN1	IN1
1	0	IN2	IN2
1	1	IN3	Reserved

3.5.2 Automatic Input Selection (IN0, IN1, IN2, IN3)

An automatic input selection state machine is available in addition to the manual switching option. In automatic mode, the selection criteria is based on input clock qualification, input priority, and the revertive option. Only input clocks that are valid can be selected by the automatic clock selection state machine. If there are no valid input clocks available the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid an automatic switchover to a valid input with the highest priority will be initiated.

3.5.3 Hitless Input Switching

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or at a fractional frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during a input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 7.68 MHz.

3.5.4 Ramped Input Switching

When switching between two plesiochronous input clocks (i.e., the frequencies are "almost the same" but not quite), ramped input switching should be enabled to ensure a smooth transition between the two inputs. Ramped input switching avoids frequency transients and overshoot when switching between frequencies and so is the default switching mode in CBPro. The feature should be turned off when switching between input clocks that are always frequency locked (i.e., are always the same exact frequency). The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover see 3.4.5 Holdover Mode.

3.5.5 Glitchless Input Switching

The DSPLL has the ability of switching between two input clock frequencies that are up to ±20 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no abrupt phase change at the output during the transition.

3.5.6 Input Configuration and Terminations

Each of the inputs can be configured as differential or single-ended LVCMOS. The recommended input termination schemes are shown in Figure 14. Differential signals must be ac-coupled, while single-ended LVCMOS signals can be ac or dc-coupled. Unused inputs can be disabled and left unconnected when not in use.

Standard AC Coupled Differential LVDS

Standard AC Coupled Differential LVPECL

Standard AC Coupled Single Ended

DC Coupled CMOS

IN_CMOS_USE1P8 = 1, at address 0x094F

Pulsed CMOS DC Coupled Single Ended

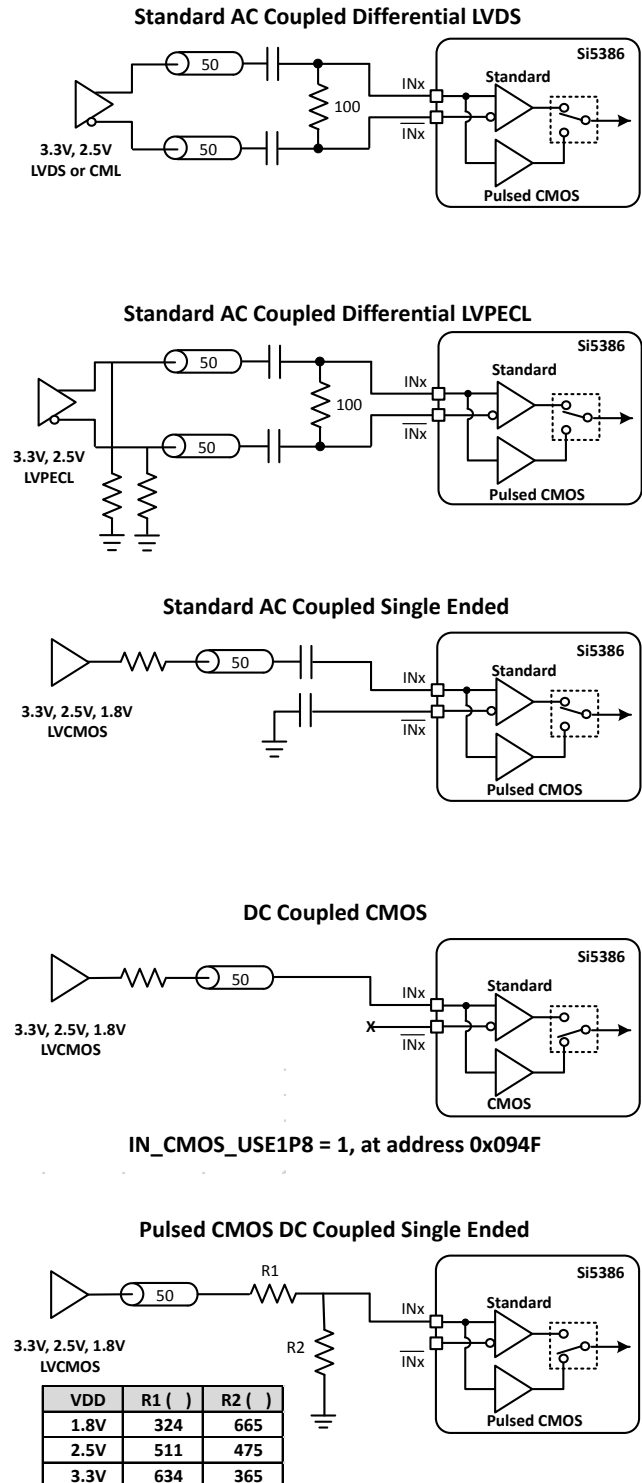| VDD	R1 ( )	R2 ( )
1.8V	324	665
2.5V	511	475
3.3V	634	365

Figure 3.3. Termination of Differential and LVCMOS Input Signals

3.6 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3/FB_IN) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins (grade A) or internal 48.0231 MHz crystal (grade E) is also monitored for LOS since it provides a critical reference clock for the DSPLL. There is also a Loss Of Lock (LOL) indicator which is asserted when the DSPLL loses synchronization.
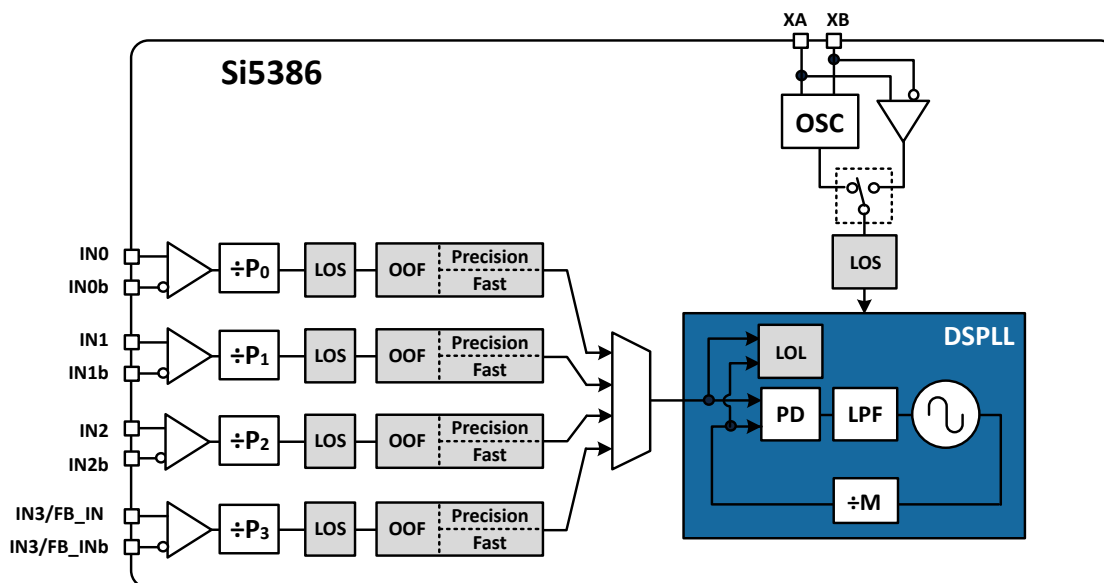
Figure 3.4. Si5386 Fault Monitors (Grade A)

3.6.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility.

The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.
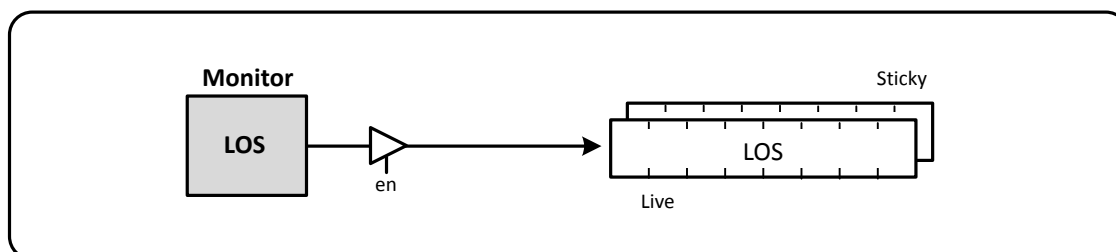
Figure 3.5. LOS Status Indicators

3.6.2 Reference Clock LOS Detection

A LOS monitor is available to ensure that the internal 48.0231 MHz crystal (grade E) or external reference (grade A) clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

3.6.3 OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its "0_ppm" reference. This OOF reference can be selected as either:

- The XA/XB (grade A) or internal crystal (grade E) reference
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.
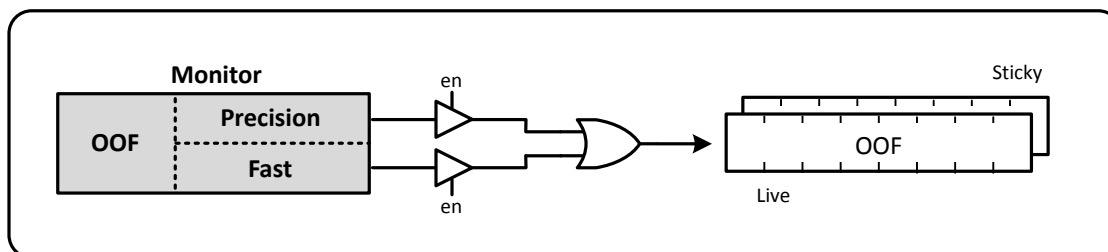
Figure 3.6. OOF Status Indicator

3.6.3.1 Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range which is register configurable up to ±20 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the internal crystal reference is available. This option is register configurable.
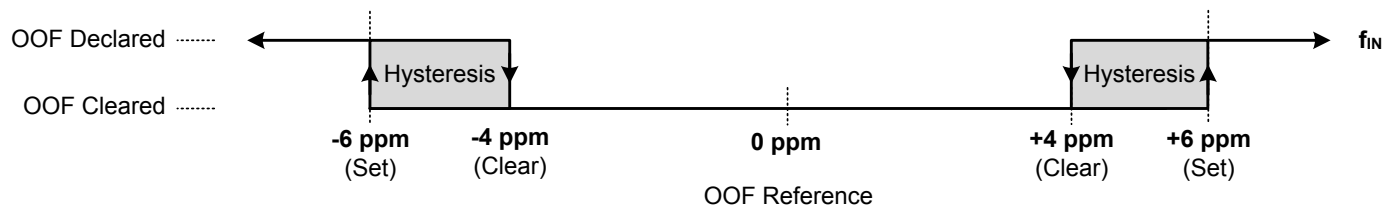
Figure 3.7. Example of Precise OOF Monitor Assertion and Deassertion Triggers

3.6.3.2 Fast OOF Monitor

Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

3.6.4 LOL Detection

The Loss Of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock.

There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.
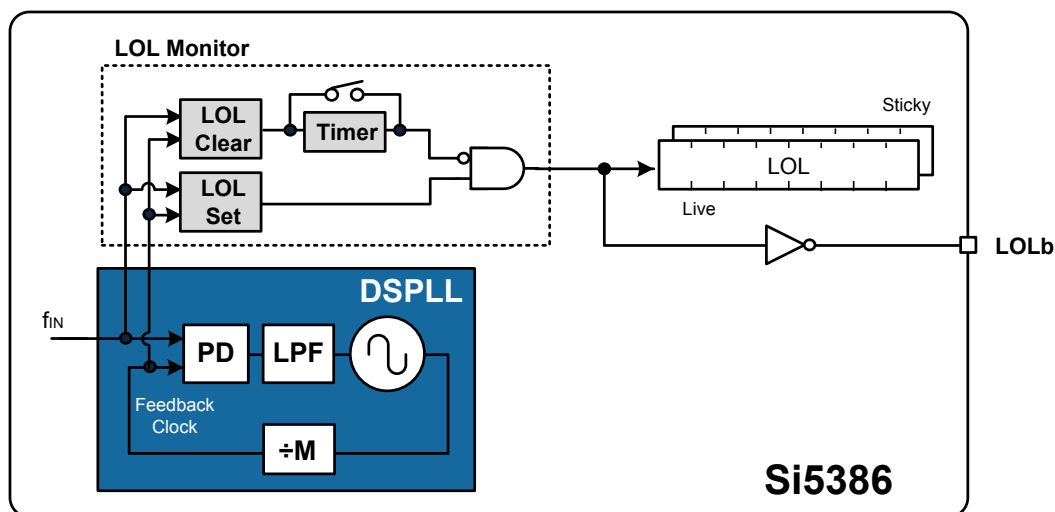
Figure 3.8. LOL Status Indicators

The LOL frequency monitors have an adjustable sensitivity which is register configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status.

An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 1 ppm frequency difference is shown in the following figure.

Figure 3.9. LOL Set and Clear Thresholds

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

3.6.5 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state of the status indicators (LOS, OOF, LOL, HOLD). Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the status register that caused the interrupt.

3.7 Outputs

Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

3.7.1 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the MultiSynths as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.
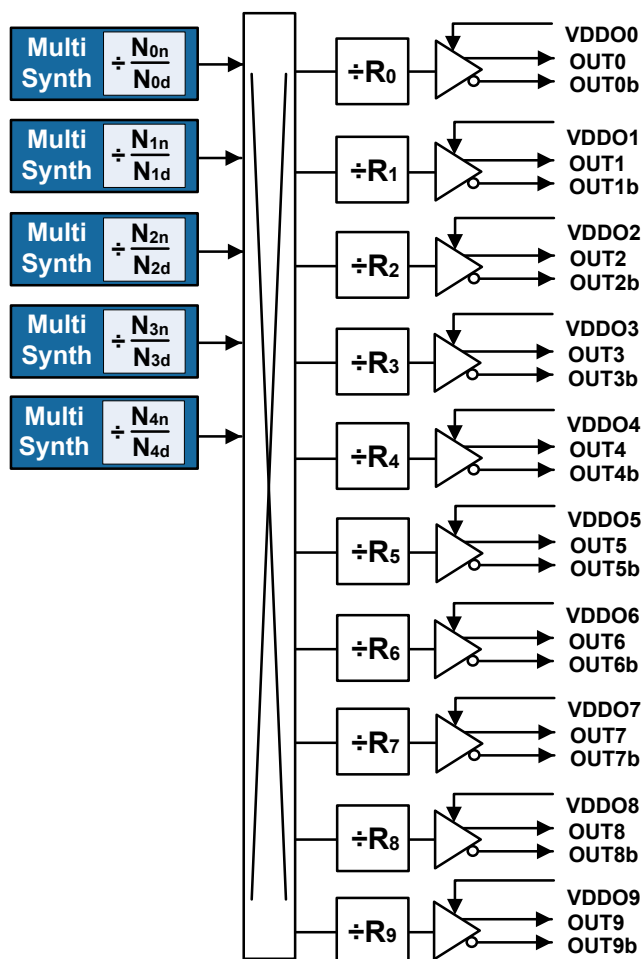
Figure 3.10. MultiSynth to Output Driver Crosspoint

3.7.2 Output Signal Format

The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

3.7.3 Differential Output Terminations

The differential output drivers support both ac-coupled and dc-coupled terminations as shown in the figure below.
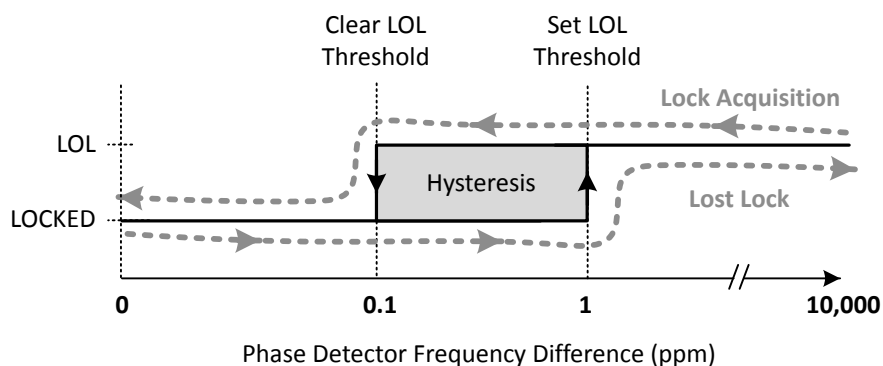
Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

DC Coupled LVDS/LVPECL

AC Coupled LVPECL

AC Coupled LVDS/LVPECL
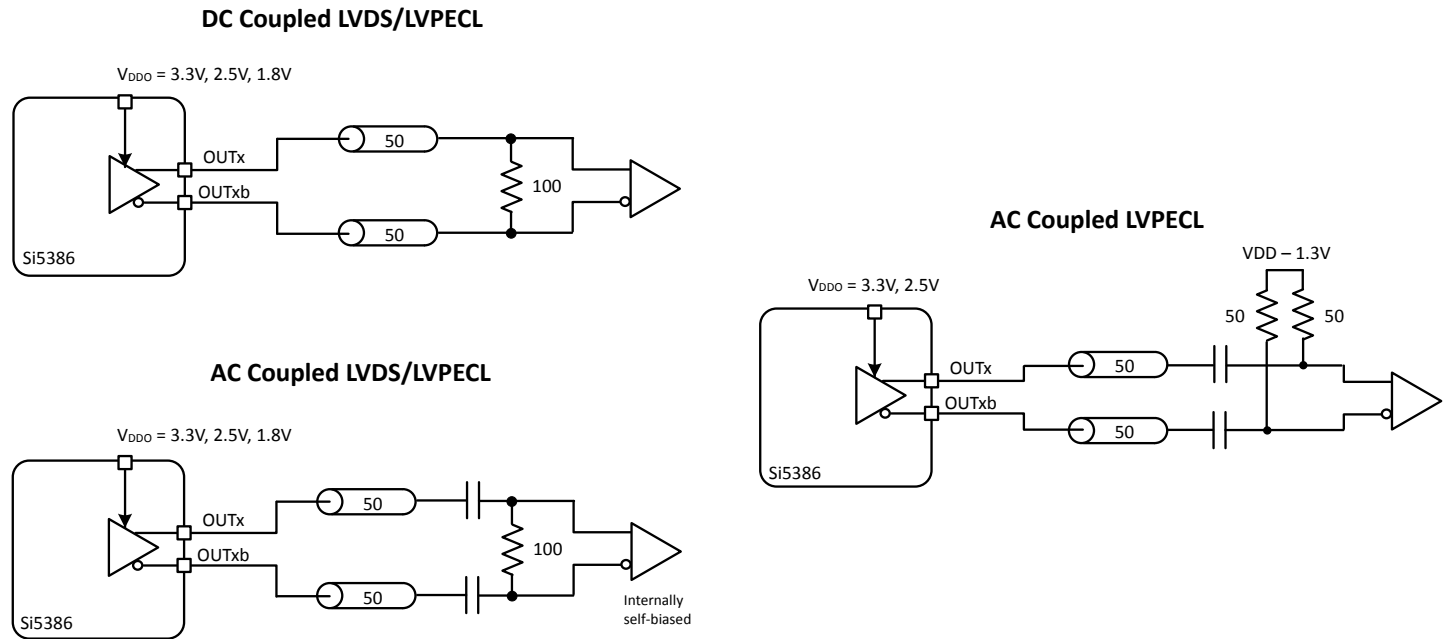
Figure 3.11. Supported Differential Output Terminations

3.7.4 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled, as shown in the following figure.

DC Coupled LVCMOS
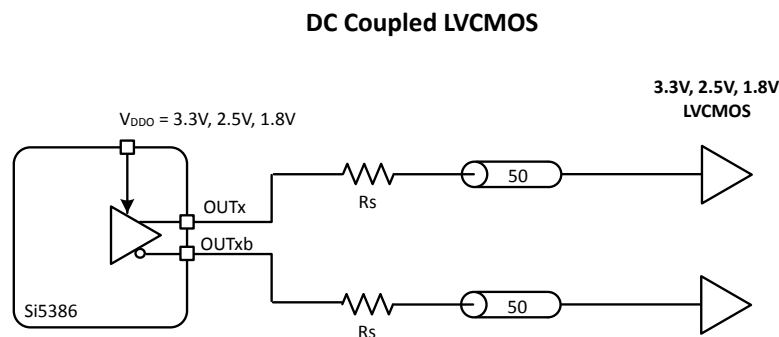
Figure 3.12. LVCMOS Output Terminations

3.7.5 Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential modes are programmable so that LVDS specifications can be met and for the best signal integrity with different supply voltages. When dc coupling the output driver, it is essential that the receiver have a relatively high common mode impedance so that the common mode current from the output driver is very small.

3.7.6 LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances. A source termination resistor is recommended to help match the selected output impedance to the trace impedance, where Rs = Transmission line impedance – Z_O. There are three programmable output impedance selections (CMOS1, CMOS2, CMOS3) for each VDDO option as shown in the following table.

Table 3.2. Typical Output Impedance (Z_S)

VDDO	CMOS Drive Selections		
	OUTx_CMOS_DRV = 1	OUTx_CMOS_DRV = 2	OUTx_CMOS_DRV = 3
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

3.7.7 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

3.7.8 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default, the clock on the OUTx pin is generated with the same polarity (in phase) as the clock on the OUTxb pin. The polarity of these clocks is configurable, enabling complementary clock generation and/or inverted polarity with respect to other output drivers.

3.7.9 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling the output drivers. When the OEb pin is held high, all outputs are disabled. When held low, the outputs are enabled. Outputs in the enabled state can be individually disabled through register control.

3.7.10 Output Driver State When Disabled

The disabled state of an output driver is configurable as disable low or disable high.

3.7.11 Synchronous Output Disable Feature

The output drivers provide a selectable synchronous disable feature. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete.

3.7.12 Zero Delay Mode

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in the figure below.

This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9 and FB_IN pins are recommended for the external feedback connection. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance. Note that the hitless switching feature is not available when zero delay mode is enabled.
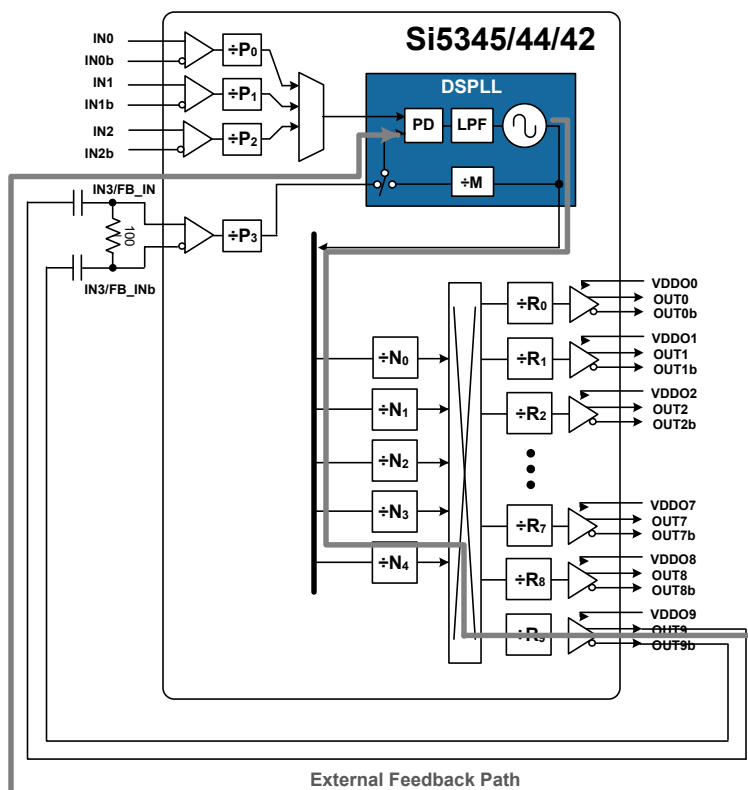
Figure 3.13. Si5386 Zero Delay Mode Setup

3.7.13 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result.

3.8 Power Management

Unused inputs and output drivers can be powered down when unused. Consult the Reference Manual and ClockBuilder Pro configuration utility for details.

3.9 In-Circuit Programming

The Si5386 is fully configurable using the serial interface (I^{2}C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Reference Manual for a detailed procedure for writing registers to NVM.

3.10 Serial Interface

Configuration and operation of the Si5386 is controlled by reading and writing registers using the I^{2}C or SPI interface. The I2C_SEL pin selects I^{2}C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire. See the Reference Manual for details.

3.11 Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory preprogrammed part will generate clocks at power-up. Custom, factory-preprogrammed devices are available. The ClockBuilder Pro custom part number wizard can be used to quickly and easily generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your preprogrammed device will typically ship in about two weeks.

3.12 Enabling Features and/or Configuration Settings Unavailable in ClockBuilder Pro for Factory Preprogrammed Devices

As with essentially all modern software utilities, ClockBuilder Pro is continually being updated and enhanced. By registering at www.si-labs.com, you will be notified about changes and their impact. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Reference Manual.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is not yet available in CBPro, you must contact a Silicon Labs applications engineer for assistance. One example of this type of feature or custom setting is the customizable output amplitude and common voltages for the clock outputs. After careful review of your project file and requirements, the Silicon Labs applications engineer will email back your CBPro project file with your specific features and register settings enabled using what's referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown in the following table.

Table 3.3. Setting Overrides

Location	Name	Type	Target	Dec Value	Hex Value
0x0535[0]	FORCE_HOLD	No NVM	N/A	1	0x1
0x0B48[0:4]	OOF_DIV_CLK_DIS	User	OPN&EVB	0	0x00

Once you receive the updated design file, simply open it in CBPro. The device will begin operation after startup with the values in the NVM file. The flowchart for this process is shown in the following figure.
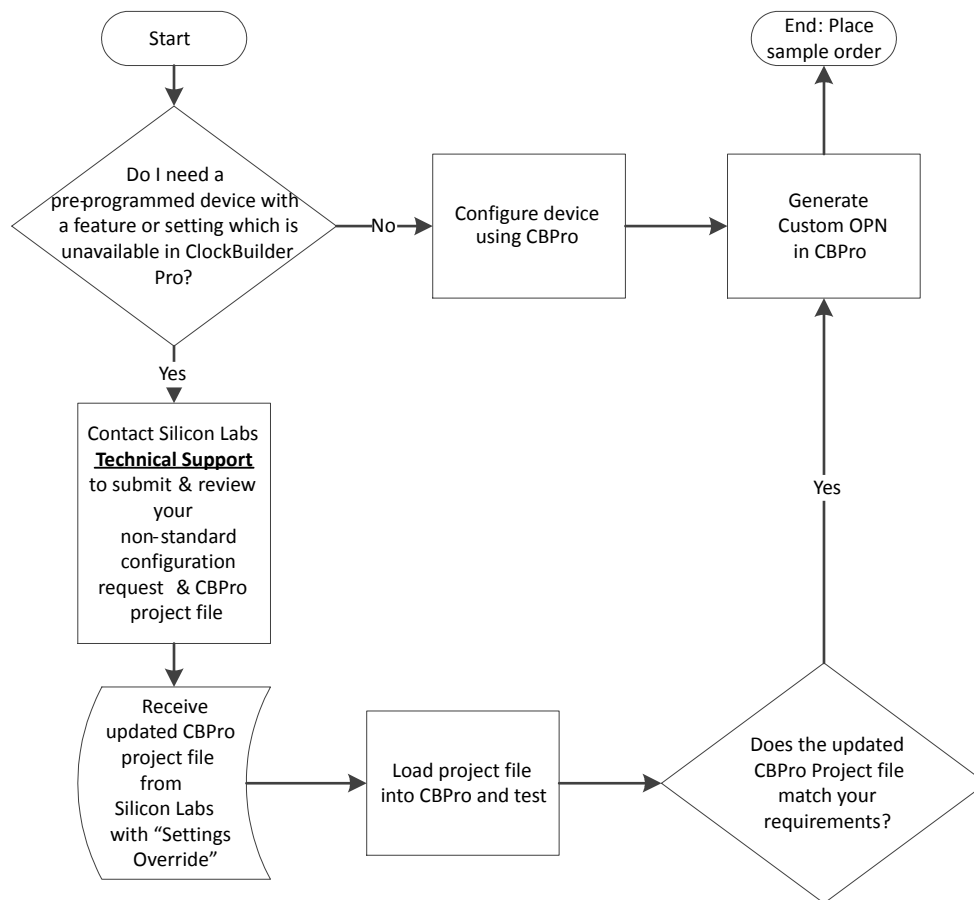
Figure 3.14. Process for Requesting Non-Standard CBPro Features

Note: Contact Silicon Labs Technical Support at www.silabs.com/support/Pages/default.aspx.

4. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible registers, such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. A high level map of the registers is shown in "6.2. High-Level Register Map" . Refer to the Reference Manual for a complete list of register descriptions and settings. Silicon Labs strongly recommends using Clock-Builder Pro to create and manage register settings.

4.1 Addressing Scheme

The device registers are accessible using a 16-bit address that consists of an 8-bit page address plus an 8-bit register address. By default, the page address is set to 0x00. Changing to another page is accomplished by writing to the "Set Page Address" byte located at address 0x01 of each page.

4.2 High-Level Register Map

Table 4.1. High-Level Register Map

16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
00	00	Revision IDs
	01	Set Page Address
	02–0A	Device IDs
	0B–15	Alarm Status
	17–1B	INTR Masks
	1C	Reset controls
	1D	FINC, FDEC Control Bits
	2B	SPI (3-Wire vs 4-Wire)
	2C–E1	Alarm Configuration
	E2–E4	NVM Controls
	FE	Device Ready Status
01	01	Set Page Address
	08–3A	Output Driver Controls
	41–42	Output Driver Disable Masks
	FE	Device Ready Status
02	01	Set Page Address
	02–05	XTAL Frequency Adjust
	08–2F	Input Divider (P) Settings
	30	Input Divider (P) Update Bits
	47–6A	Output Divider (R) Settings
	6B–72	User Scratch Pad Memory
	FE	Device Ready Status

16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
03	01	Set Page Address
	02–37	MultiSynth Divider (N0–N4) Settings
	0C	MultiSynth Divider (N0) Update Bit
	17	MultiSynth Divider (N1) Update Bit
	22	MultiSynth Divider (N2) Update Bit
	2D	MultiSynth Divider (N3) Update Bit
	38	MultiSynth Divider (N4) Update Bit
	39–58	FINC/FDEC Settings N0–N4
	59–62	Output Delay (Δt) Settings
	FE	Device Ready Status
04	87	Zero Delay Mode Set Up
05	0E–14	Fast Lock Loop Bandwidth
	15–1F	Feedback Divider (M) Settings
	2A	Input Select Control
	2B	Fast Lock Control
	2C–35	Holdover Settings
	36	Input Clock Switching Mode Select
	38–39	Input Priority Settings
	3F	Holdover History Valid Data
06–08	00–FF	Reserved
09	01	Set Page Address
	1C	Zero Delay Mode Settings
	43	Control I/O Voltage Select
	49	Input Settings
10–FF	00–FF	Reserved

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Ambient Temperature	T_A	–40	25	85	°C
Maximum Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V

Note:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5.2. DC Characteristics

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Core Supply Current	I_{DD}	Notes 1, 2	—	175	—	mA
	I_{DDA}		—	120	—	mA
Output Buffer Supply Current	I_{DDO}	LVPECL Output[3] @ 156.25 MHz	—	21	25	mA
		LVDS Output[3] @ 156.25 MHz	—	15	18	mA
		3.3 V LVCMOS[4] Output @ 156.25 MHz	—	21	25	mA
		2.5 V LVCMOS[4] Output @ 156.25 MHz	—	16	18	mA
		1.8 V LVCMOS[4] Output @ 156.25 MHz	—	12	13	mA
Total Power Dissipation	P_d	Note 1,5	—	1125	—	mW

(V_DD = 1.8 V ±5%, V_DDA = 3.3 V ±5%, V_DDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**

Note:

1. Si5386 test configuration: 8 clock outputs enabled (2 x 983.04 MHz, 2 x 491.52 MHz, 1 x 245.76 MHz, 3 x 122.88 MHz; 2.5 LVDS). Excludes power in termination resistors.
2. VDDO0 supplies power to both OUT0 and OUT0A buffers. Similarly, VDDO9 supplies power to both OUT9 and OUT9A buffers.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 6-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, which is the strongest driver setting.
5. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Differential Output Test Configuration
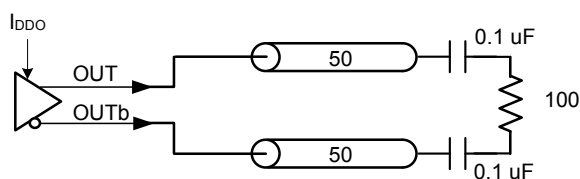
LVCMOS Output Test Configuration
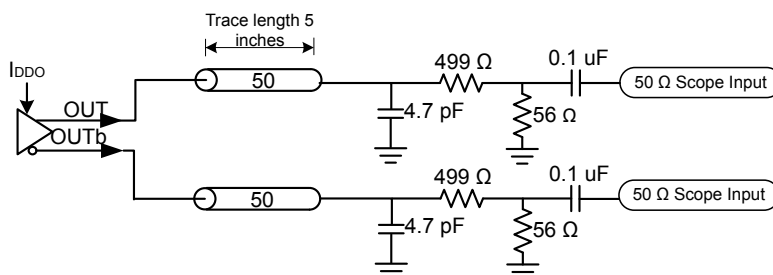
Table 5.3. Input Clock Specifications

(V_DD = 1.8 V ±5%, V_DDA = 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Standard Differential or Single-Ended/LVCMOS — AC-coupled (IN0, IN1, IN2, IN3)						
Input Frequency Range	f_{IN_DIFF}	Differential	7.68	—	750	MHz
	f_{IN_SE}	Single-ended/ LVCMOS	7.68	—	250	
Input Voltage Amplitude	V_{IN_DIFF}	f_{IN_DIFF} < 250 MHz	100	—	1800	mVpp_se
		250 MHz < f_{IN_DIFF} < 750 MHz	225	—	1800	mVpp_se
Single-Ended Input Swing	V_{IN_SE}	f_{IN_SE} < 250 MHz	100	—	3600	mVpp_se
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2	—	pF
Pulsed CMOS — DC-coupled (IN0, IN1, IN2, IN3)[3]						
Input Frequency	f_{IN_CMOS}		7.68	—	250	MHz
Input Voltage	V_{IL}		–0.2	—	0.33	V
	V_{IH}		0.49	—	—	V
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC	Clock Input	40	—	60	%

(V$_{DD}$ = 1.8 V ±5%, V$_{DDA}$ = 3.3 V ±5%, T$_A$ = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R$_{IN}$		—	8	—	kΩ
REFCLK (applied to XA/XB, Grade A only)[4]						
REFCLK	f$_{IN\_REF}$	4G/LTE	—	54	—	MHz
Total Frequency Tolerance	f$_{RANGE}$		-100	—	+100	ppm
Input Voltage Swing	V$_{IN\_SE}$		365	—	2000	mVpp_se
	V$_{IN\_DIFF}$		365	—	2500	mVpp_diff
Slew Rate[1, 2]	SR	Imposed for phase noise performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%
Integrated Crystal REFCLK (Grade E)						
Crystal Frequency	f$_{INT\_XTAL}$			48.0231		MHz
Frequency Stability	f$_{STABLE}$	Includes 10 year aging		TBD		ppm
Frequency Perturbation	f$_{PERT}$		—	—	TBD	

Note:
1. Imposed for phase noise performance.
2. Rise and fall times can be estimated using the following simplified equation: tr/tf80-20 = ((0.8 - 0.2) * VIN_Vpp_se) / SR.
3. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks <1 MHz, which must be dc-coupled, having a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. Since the input thresholds (VIL, VIH) of this buffer are non-standard, refer to the input attenuator circuit for dc-coupled Pulsed LVCMOS in the Si5386 Reference Manual. Otherwise, for standard LVCMOS input clocks, use the "AC-coupled Singled-Ended" mode as shown in 3.5.6 Input Configuration and Terminations.
4. Refer to the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual for recommended 54 MHz crystals.

Table 5.4. Serial and Control Input Pin Specifications

(V$_{DD}$ = 1.8 V ±5%, V$_{DDA}$ = 3.3 V ±5%, V$_{DDS}$ = 3.3 V ±5%, 1.8 V ±5%, T$_A$ = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Serial and Control Input Pins (IN_SEL[1:0], RSTb, OEb, PDNb, A1/SDO, SCLK, A0/CSb, SDA/SDIO)						
Input Voltage Thresholds	V$_{IL}$		—	—	0.3 x V$_{DDIO}$[1]	V
	V$_{IH}$		0.7 x V$_{DDIO}$[1]	—	—	V
Input Capacitance	C$_{IN}$		—	2	—	pF
Input Resistance	I$_L$		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb, PDNb	100	—	—	ns

Note:
1. V$_{DDIO}$ is determined by the IO_VDD_SEL bit. It is selectable as V$_{DDA}$ or V$_{DD}$. See the Si5386 Reference Manual for more details on the register settings.

Table 5.5. Differential Clock Output Specifications

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)							
Output Frequency[6]	f_{OUT}			0.0001	—	2949.12	MHz
Duty Cycle	DC	f_{OUT} < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 800 MHz		45	—	55	%
		800 MHz < fOUT < 1474.56 MHz		40	—	60	%
		f > 1474.56 MHz		35	—	65	%
Output-Output Skew	T_{SK}	Differential output. Specified for outputs using the same MultiSynth		—	20	50	ps
OUT-OUTb Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	0	100	ps
Output Voltage Amplitude[1]		**Normal Mode**					
	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	350	470	550	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	660	810	1000	
Common Mode Voltage [1,2,3]		**Normal Mode**					
	VCM	V_{DDO} = 3.3 V	LVDS	1.10	1.25	1.35	V
			LVPECL	1.90	2.05	2.15	
		V_{DDO} = 2.5 V	LVPECL, LVDS	1.15	1.25	1.35	
		V_{DDO} = 1.8 V	sub-LVDS	0.87	0.93	1.00	
Rise and Fall Times (20% to 80%)	t_R/t_F	Normal Mode		—	170	240	ps
Differential Output Impedance[2]	Z_O	Normal Mode		—	100	—	Ω
Power Supply Noise Rejection[4]	PSRR	**Normal Mode**					
		10 kHz sinusoidal noise		—	–93	—	dBc
		100 kHz sinusoidal noise		—	–93	—	
		500 kHz sinusoidal noise		—	–84	—	
		1 MHz sinusoidal noise		—	–79	—	
Output-output Crosstalk[5]	XTALK	Differential		—	–75	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
(V$_{DD}$ = 1.8 V ±5%, V$_{DDA}$ = 3.3 V ±5%, V$_{DDO}$ = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T$_A$ = –40 to 85 °C)						

Note:

1. Output amplitude and common mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. Refer to the Si5386 Reference Manual for recommended output settings.

2. Not all combinations of voltage amplitude and common mode voltages settings are possible.

3. Driver output impedance depends on selected output mode (Normal, Low Power). Refer to the Si5386 Reference Manual for more information.

4. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.

5. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems", guidance on crosstalk minimization. Note that all active outputs must be terminated when measuring crosstalk.

6. VDDO = 2.5 V or 3.3 V required for fOUT > 1474.56 MHz

OUTx

OUTxb

Vcm — Vpp_se
Vcm — Vpp_se

Vpp_diff = 2*Vpp_se

Table 5.6. LVCMOS Clock Output Specifications

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
(V$_{DD}$ = 1.8 V ±5%, V$_{DDA}$ = 3.3 V ±5%, V$_{DDO}$ = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T$_A$ = –40 to 85 °C)							
Output Frequency	f$_{OUT}$			0.0001	—	250	MHz
Duty Cycle	DC	fOUT <100 MHz		47	—	53	%
		100 MHz < fOUT < 250 MHz		44	—	55	
Output-to-Output Skew	T$_{SK}$	LVCMOS, integer related from the same Multi-Synth		—	—	100	ps
Output Voltage High[1, 2, 3]	V$_{OH}$	VDDO = 3.3 V					
		OUTx_CMOS_DRV=1	IOH = –10 mA	VDDO x 0.75	—	—	V
		OUTx_CMOS_DRV=2	IOH = –12 mA		—	—	
		OUTx_CMOS_DRV=3	IOH = –17 mA		—	—	
		VDDO = 2.5 V					
		OUTx_CMOS_DRV=1	IOH = –6 mA	VDDO x 0.75	—	—	V
		OUTx_CMOS_DRV=2	IOH = –8 mA		—	—	
		OUTx_CMOS_DRV=3	IOH = –11 mA		—	—	
		VDDO = 1.8 V					
		OUTx_CMOS_DRV=2	IOH = –4 mA	VDDO x 0.75	—	—	V
		OUTx_CMOS_DRV=3	IOH = –5 mA		—	—	

(V$_{DD}$ = 1.8 V ±5%, V$_{DDA}$ = 3.3 V ±5%, V$_{DDO}$ = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T$_A$ = –40 to 85 °C)							
Parameter	**Symbol**	**Test Condition**		**Min**	**Typ**	**Max**	**Unit**
Output Voltage Low[1, 2, 3]	V$_{OL}$	VDDO = 3.3 V					
		OUTx_CMOS_DRV=1	IOL = 10 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=2	IOL = 12 mA	—	—		
		OUTx_CMOS_DRV=3	IOL = 17 mA	—	—		
		VDDO = 2.5 V					
		OUTx_CMOS_DRV=1	IOL = 6 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=2	IOL = 8 mA	—	—		
		OUTx_CMOS_DRV=3	IOL = 11 mA	—	—		
		VDDO = 1.8 V					
		OUTx_CMOS_DRV=2	IOL = 4 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=3	IOL = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3 V		—	420	550	ps
		VDDO = 2.5 V		—	475	625	ps
		VDDO = 1.8 V		—	525	705	ps

Note:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5386 Reference Manual for more details on register settings.
2. IOL/IOH is measured at VOL/VOH as shown in the dc test configuration.
3. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

DC Test Configuration
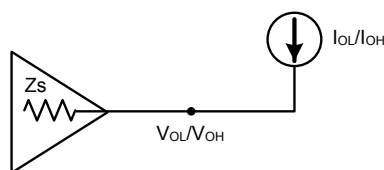
AC Output Test Configuration
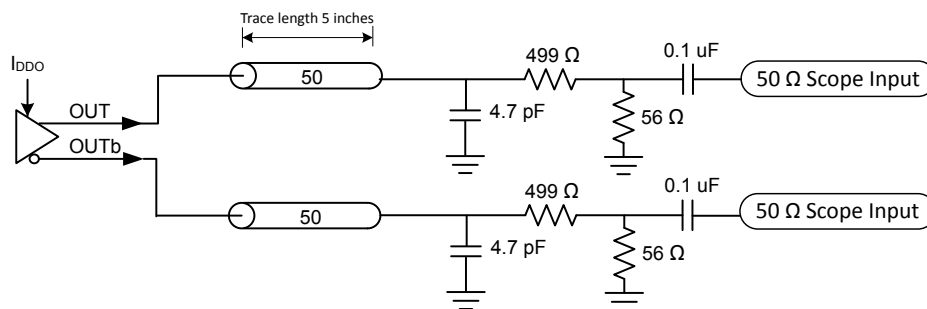
Table 5.7. Output Serial and Status Pin Specifications

(V$_{DD}$ = 1.8 V ±5%, V$_{DDA}$ = 3.3 V ±5%, V$_{DDS}$ = 3.3 V ±5%, 1.8 V ±5%, T$_A$ = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Serial and Status Output Pins (INTRb, LOLb, SDA/SDIO[2], A1/SDO)						
Output Voltage	V$_{OH}$	IOH = –2 mA	V$_{DDIO}$[1] x 0.75	—	—	V
	V$_{OL}$	IOL = 2 mA	—	—	V$_{DDIO}$[1] x 0.15	V

(V_DD = 1.8 V ±5%, V_DDA = 3.3 V ±5%, V_DDS = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. V_DDIO is determined by the IO_VDD_SEL bit. It is selectable as VDDA or VDD. Users normally select this option in the Clock-Builder Pro GUI. Alternatively, refer to the Si5386 Reference Manual for more details on register settings.

2. The V_OH specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I2C mode or is unused with I2C_SEL pulled high internally. V_OL remains valid in all cases.

Table 5.8. Performance Characteristics

(V_DD = 1.8 V ±5%, or 3.3 V ±5%, V_DDA = 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range[1]	f_{BW}		1	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up or de-assertion of PDNb to when the device generates free-running clocks	—	30	45	ms
PLL Lock Time	t_{ACQ}	Fastlock enabled, fIN = 19.44 MHz[2]	—	500	600	ms
POR to Serial Interface Ready[3]	t_{RDY}		—	15	—	ms
Jitter Peaking	J_{PK}	25 MHz input, 25 MHz output, loop bandwidth of 4 Hz	—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1&2 Carrier Frequency = 10.3125 GHz Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient	t_{SWITCH}	Automatic Hitless Switch	—	—	TBD	ns
Pull-in Range	ω_P	Internal crystal reference	—	20	—	ppm
RMS Jitter Generation[4]	J_{GEN}	12 kHz to 20 MHz	—	80	—	fs RMS
Phase Noise Performance[4] (122.88 MHz Carrier Frequency)	PN	10 Hz	—	TBD	—	dBc/Hz
		100 Hz	—	TBD	—	dBc/Hz
		1 kHz	—	TBD	—	dBc/Hz
		10 kHz	—	TBD	—	dBc/Hz
		100 kHz	—	TBD	—	dBc/Hz
		1 MHz	—	TBD	—	dBc/Hz
		10 MHz	—	TBD	—	dBc/Hz
Spur Performance (122.88 MHz Carrier Frequency)	SPUR	Up to 1 MHz offset	—	-103	—	dBc
		From 1 MHz to 30 MHz offset	—	-95	—	dBc

(V$_{DD}$ = 1.8 V ±5%, or 3.3 V ±5%, V$_{DDA}$ = 3.3 V ±5%, T$_A$ = –40 to 85 °C)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Actual loop bandwidth may be lower; please refer to CBPro for actual value on your frequency plan.

2. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal and fastlock bandwidths, both set to 100 Hz, LOL set/clear thresholds of 3/0.3 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator de-assertion.

3. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.

4. Jitter generation test conditions: fIN = 30.72 MHz, 3.3V LVPECL, DSPLL LBW = 100 Hz. Jitter integrated from 12 kHz to 20 MHz offset. Does not include jitter from PLL input reference.

5. Measured between a common 2 MHz input and 2 MHz output with different N-dividers on the same unit and a loop bandwidth of 4 kHz. These output frequencies are generated using non-production engineering modes only for test.

6. Delay between reference and feedback input both clocks at 10 MHz and same slew rate. Ref clock rise time must be < 200 ps. These output frequencies are generated using non-production engineering modes only for test.

Table 5.9. I2C Timing Specifications (SCL,SDA)

| Parameter	Symbol	Test Condition	Min	Max	Min	Max	Unit
			Standard Mode 100 kbps		Fast Mode 400 kbps		
SCL Clock Frequency	f$_{SCL}$		—	100	—	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold Time (Repeated) START Condition	t$_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t$_{LOW}$		4.7	—	1.3	—	µs
HIGH Period of the SCL Clock	t$_{HIGH}$		4.0	—	0.6	—	µs
Set-up Time for a Repeated START Condition	t$_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time	t$_{HD:DAT}$		100	—	100	—	ns
Data Set-up Time	t$_{SU:DAT}$		250	—	100	—	ns
Rise Time of Both SDA and SCL Signals	t$_r$		—	1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t$_f$		—	300	—	300	ns
Set-up Time for STOP Condition	t$_{SU:STO}$		4.0	—	0.6	—	µs
Bus Free Time between a STOP and START Condition	t$_{BUF}$		4.7	—	1.3	—	µs
Data Valid Time	t$_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	t$_{VD:ACK}$		—	3.45	—	0.9	µs
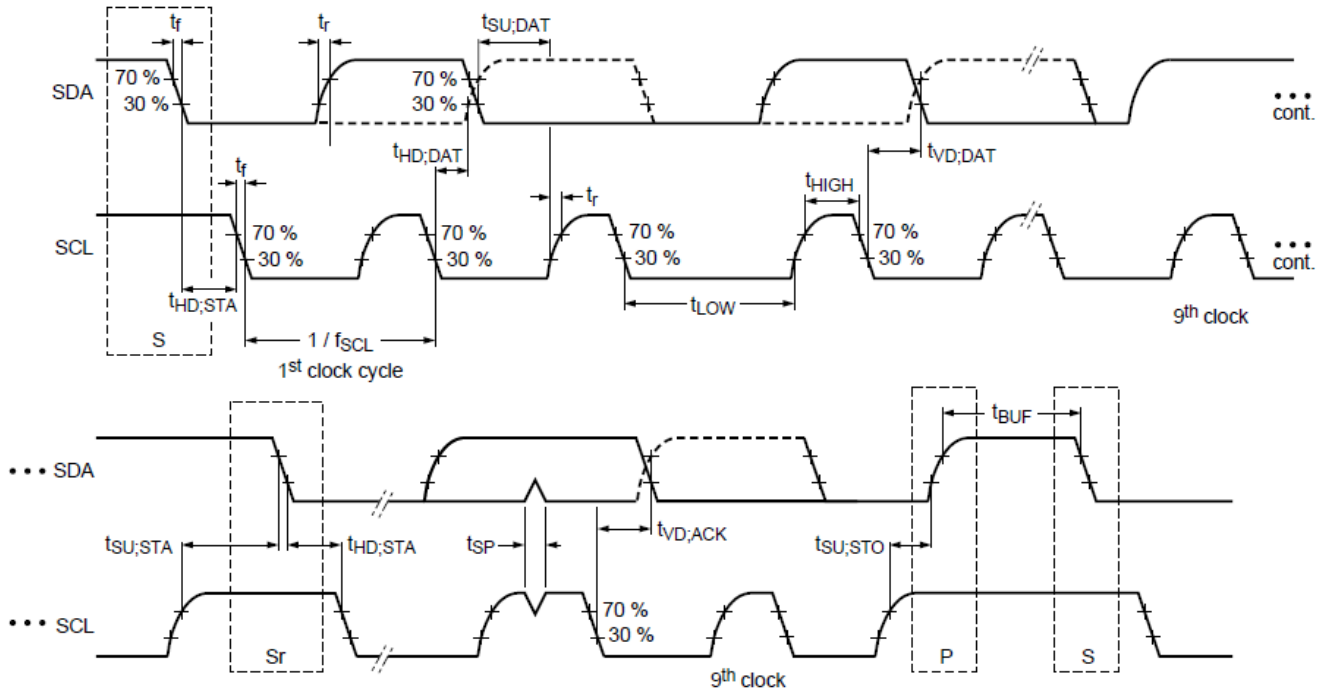
Figure 5.1. I²C Serial Port Timing Standard and Fast Modes

Table 5.10. SPI Timing Specifications (4-Wire)

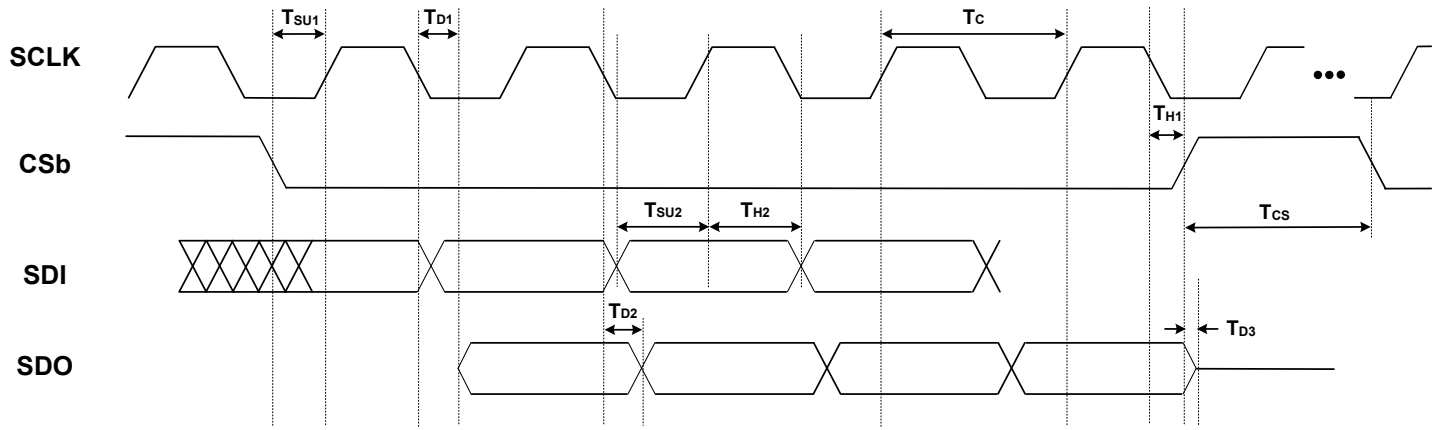| Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	—	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDO Tri-State	T_{D3}	—	—	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_c

Figure 5.2. 4-Wire SPI Serial Interface Timing

Table 5.11. SPI Timing Specifications (3-Wire)

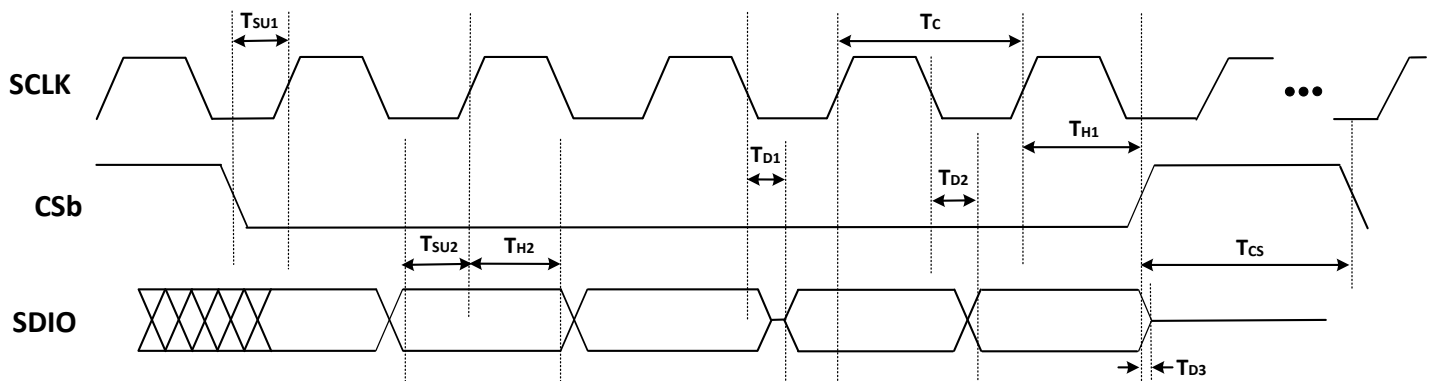| Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	—	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	—	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_C

Figure 5.3. 3-Wire SPI Serial Interface Timing

Table 5.12. External Crystal Specifications (Grade A only)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency[1]	f_{XTAL}		—	54	—	MHz
Total Frequency Tolerance[2]	f_{RANGE}		-100	—	+100	ppm
Load Capacitance	C_L		—	8	—	pF
Crystal Output Capacitance	C_O		—	—	2	pF
Crystal Drive Level	d_L		—	—	350	µW
Equivalent Series Resistance	r_{ESR}	Refer to the Si5386 Reference Manual.				

Note:
1. The Si5386 is designed to work with crystals that meet the frequencies and specifications in Table 12.
2. Refer to the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual for recommended 54 MHz crystals.

Table 5.13. Thermal Characteristics (Grade A, QFN-64)

Parameter	Symbol	Test Condition1	Value	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	Θ_{JC}		9.5	
Thermal Resistance Junction to Board	Θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	

Note:
1. Based on PCB Dimension: 3" x 4.5", PCB Thickness: 1.6 mm, PCB Land/Via under GNP pad: 36, Number of Cu Layers: 4

Table 5.14. Table 5.14 Thermal Characteristics (Grade E, LGA-64)

Parameter	Symbol	Test Condition1	Value	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	TBD	°C/W
		Air Flow 1 m/s	TBD	
		Air Flow 2 m/s	TBD	
Thermal Resistance Junction to Case	Θ_{JC}		TBD	
Thermal Resistance Junction to Board	Θ_{JB}		TBD	
	Ψ_{JB}		TBD	
Thermal Resistance Junction to Top Center	Ψ_{JT}		TBD	

Note:
1. Based on PCB Dimension: 3" x 4.5", PCB Thickness: 1.6 mm, PCB Land/Via under GNP pad: 36, Number of Cu Layers: 4

Table 5.15. Absolute Maximum[1, 2, 3]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	VDD		–0.5 to 3.8	V
	VDDA		–0.5 to 3.8	V
	VDDO		–0.5 to 3.8	V
Input Voltage Range	VI1	IN0 – IN3	–0.85 to 3.8	V
	VI2	IN_SEL[1:0], RSTb, PDNb, OEb, I2C_SEL, SYNC SDA/SDIO, A1/SDO, SCLK, A0/CSb	–0.5 to 3.8	V
	VI3	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Junction Temperature	T_{JCT}		–55 to 125	°C
Storage Temperature Range	T_{STG}		–55 to +150	°C
Soldering Temperature (Pb-free profile)[3]	T_{PEAK}		260	°C
Soldering Temperature Time at TPEAK(Pb-free profile)[4]	T_P		20–40	sec

Parameter	Symbol	Test Condition	Value	Unit

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-LGA (grade E) is RoHS-6 compliant.
3. For detailed MSL and packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. The device is compliant with JEDEC J-STD-020.
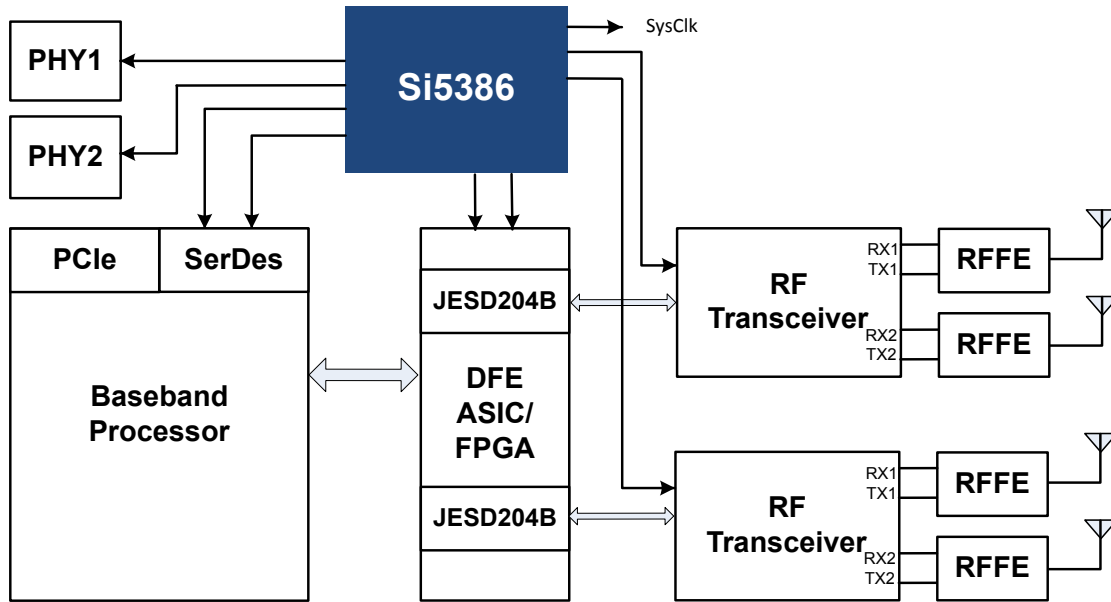
6. Typical Application Schematic

Figure 6.1. Application Block Diagram

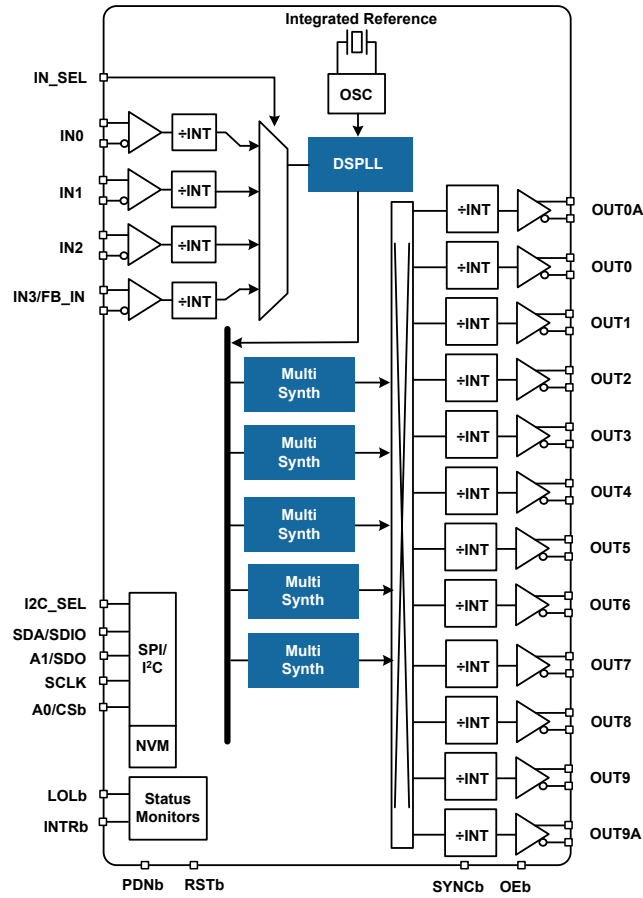# 7. Detailed Block Diagrams

Figure 7.1. Si5386 Block Diagram

8. Typical Operating Characteristics

The phase noise plots below were taken under the following conditions: V_{DD} = 1.8 V; V_{DDA} = 3.3 V; V_{DDS} = 3.3 V, 1.8 V; T_A = 25 °C.

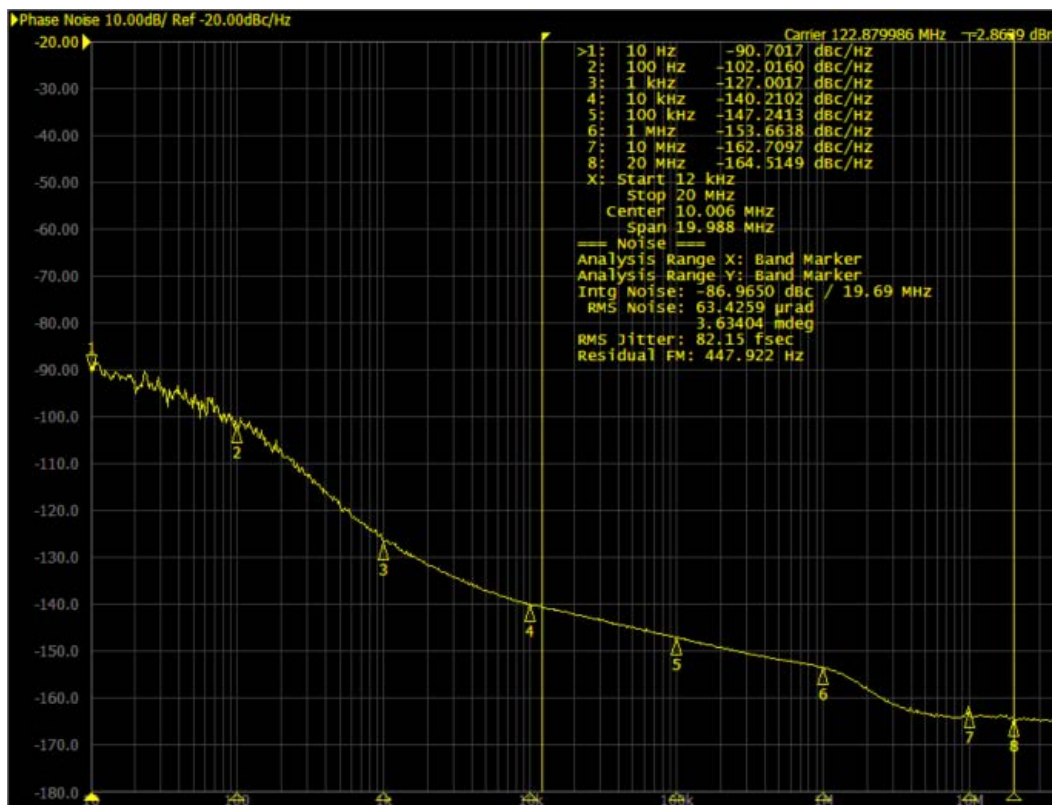**Figure 8.1. Si5386E Phase Noise, Fc = 122.88MHz**
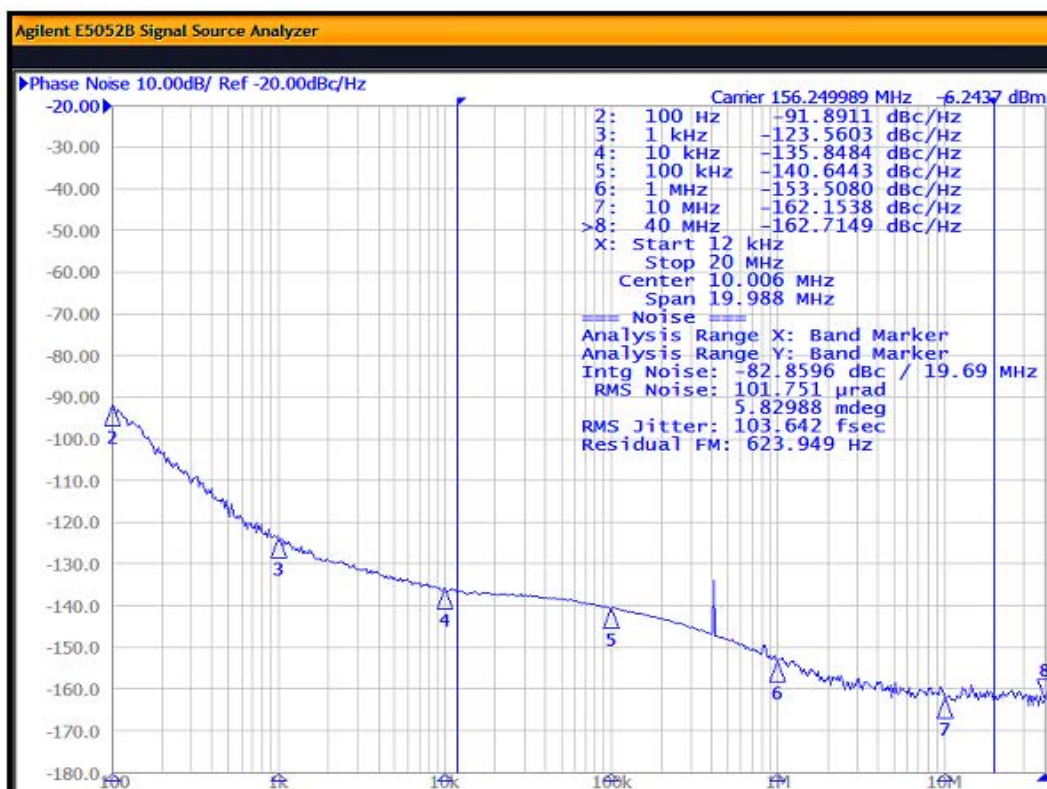
Figure 8.2. Input = 25 MHz; Output = 156.25 MHz, 2.5 V LVDS

9. Pin Descriptions

Top View (Grade E)

Top pins (left to right, 64–49): IN0b, IN0, IN3/FB_INb, IN3/FB_IN, VDD, OUT9A, OUT9Ab, VDDO9, OUT9, OUT9b, OUT8, OUT8b, VDDO8, OUT7, OUT7b, VDDO7

Left pins (top to bottom, 1–16):
IN1	1
IN1b	2
IN_SEL0	3
IN_SEL1	4
PDNb	5
RSTb	6
RSVD	7
RSVD	8
RSVD	9
RSVD	10
OEb	11
INTRb	12
VDDA	13
IN2	14
IN2b	15
SCLK	16

GND Pad

Right pins (top to bottom, 48–33):
48	SYNCb
47	LOLb
46	VDD
45	OUT6
44	OUT6b
43	VDDO6
42	OUT5
41	OUT5b
40	VDDO5
39	I2C_SEL
38	OUT4
37	OUT4b
36	VDDO4
35	OUT3
34	OUT3b
33	VDDO3

Bottom pins (left to right, 17–32): A1/SDO, SDA/SDIO, A0/CSb, OUT0Ab, OUT0A, VDDO0, OUT0b, OUT0, RSVD, VDDO1, OUT1b, OUT1, VDDO2, OUT2b, OUT2, VDD

Top View (Grade A)

Top pins (left to right, 64–49): IN0, IN0, IN3/FB_IN, IN3/FB_IN, VDD, OUT9A, OUT9A, VDDO9, OUT9, OUT9, OUT8, OUT8, VDDO8, OUT7, OUT7, VDDO7

Left pins (top to bottom, 1–16):
IN1	1
IN1	2
IN_SEL0	3
IN_SEL1	4
PDN	5
RST	6
X1	7
XA	8
XB	9
X2	10
OE	11
INTR	12
VDDA	13
IN2	14
IN2	15
SCLK	16

GND Pad

Right pins (top to bottom, 48–33):
48	SYNC
47	LOL
46	VDD
45	OUT6
44	OUT6
43	VDDO6
42	OUT5
41	OUT5
40	VDDO5
39	I2C_SEL
38	OUT4
37	OUT4
36	VDDO4
35	OUT3
34	OUT3
33	VDDO3

Bottom pins (left to right, 17–32): A1/SDO, SDA/SDIO, A0/CS, OUT0A, OUT0A, VDDO0, OUT0, OUT0, RSVD, VDDO1, OUT1, OUT1, VDDO2, OUT2, OUT2, VDD

Table 9.1. Si5386 Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
Inputs			
IN0	63	I	Clock Inputs. These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to section 3.5 Inputs (IN0, IN1, IN2, IN3) for input termination options. These pins are high-impedance and must be terminated externally, when being used. The negative side of the differential input must be ac-grounded when accepting a single-ended clock. Unused inputs may be left unconnected.
IN0b	64	I	
IN1	1	I	
IN1b	2	I	
IN2	14	I	
IN2b	15	I	
IN3/FB_IN	61	I	Clock Input 3/External Feedback Input. By default, these pins are used as the 4th clock input (IN3/IN3). They can also be used as the external feedback input (FB_IN/FB_IN) for the optional zero delay mode. See section 3.5.1 Manual Input Switching (IN0, IN1, IN2, IN3) for details on the optional zero delay mode.
IN3/FB_INb	62	I	
Outputs			

Pin Name	Pin Number	Pin Type[1]	Function
OUT0A	21	O	Output Clocks. These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in section 3.7.3 Differential Output Terminations and section 3.7.6 LVCMOS Output Impedance Selection. Unused outputs should be left unconnected.
OUT0Ab	20	O	
OUT0	24	O	
OUT0b	23	O	
OUT1	28	O	
OUT1b	27	O	
OUT2	31	O	
OUT2b	30	O	
OUT3	35	O	
OUT3b	34	O	
OUT4	38	O	
OUT4b	37	O	
OUT5	42	O	
OUT5b	41	O	
OUT6	45	O	
OUT6b	44	O	
OUT7	51	O	
OUT7b	50	O	
OUT8	54	O	
OUT8b	53	O	
OUT9	56	O	
OUT9b	55	O	
OUT9A	59	O	
OUT9Ab	58	O	
Serial Interface			
I2C_SEL	39	I	**I2C Select.** This pin selects the serial interface mode as I**2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high.**
SDA/SDIO	18	I/O	**Serial Data Interface.** This is the bidirectional data pin (SDA) for the I**2C mode, the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 k**W. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.**

Pin Name	Pin Number	Pin Type[1]	Function
A1/SDO	17	I/O	**Address Select 1/Serial Data Output.** In I2C mode this pin functions as the A1 address input pin. In 4-wire SPI mode, this is the serial data output (SDO) pin. This pin is 3.3 V tolerant.
SCLK	16	I	**Serial Clock Input.** This pin functions as the serial clock input for both I**2C and SPI modes. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 k**W**. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.**
A0/CSb	19	I	Address Select 0/Chip Select. This pin functions as the hardware controlled address A0 in I2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up. This pin is 3.3 V tolerant.
Control/Status			
INTRb	12	O	**Interrupt**[2]. This pin is asserted low when a change in device status has occurred. This pin must be pulled-up using an external resistor of at least 1 kW. It should be left unconnected when not in use.
PDNb	5	I	**Power Down**[2]. The device enters into a low power mode when this pin is pulled low. This pin is internally pulled-up. This pin is 3.3 V tolerant. It can be left unconnected when not in use.
RSTb	6	I	**Device Reset.**[2] Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up. This pin is 3.3 V tolerant.
OEb	11	I	**Output Enable**[2]. This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. This pin is 3.3 V tolerant.

Pin Name	Pin Number	Pin Type[1]	Function
LOLb	47	O	**Loss Of Lock**[2]. This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use.
SYNC	48	I	**Output Clock Synchronization**[2]. An active low signal on this pin resets the output dividers for the purpose of re-aligning the output clocks. This pin is internally pulled-up and can be left unconnected when not in use.
IN_SEL0	3	I	**Input Reference Select**[2]. The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in Table 3.1 Manual Input Selection Using IN_SEL[1:0] Pins on page 9
IN_SEL1	4	I	
RSVD	7	NC	**Reserved.** Leave disconnected.
	8	NC	
	9	NC	
	10	NC	
	25	NC	
Power			
VDD	32	P	Core Supply Voltage. The device operates from a 1.8 V supply. A 1 uF bypass capacitor should be placed very close to each pin.
VDD	46	P	
VDD	60	P	
VDDA	13	P	Core Supply Voltage 3.3 V. This core supply pin requires a 3.3 V power source. A 1 uF bypass capacitor should be placed very close to this pin.
VDDO0	22	P	Output Clock Supply Voltage. Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTn outputs. Note that VDDO0 supplies power to OUT0 and OUT0A; VDDO9 supplies power to OUT9 and OUT9A. Leave VDDO pins of unused output drivers unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	26	P	
VDDO2	29	P	
VDDO3	33	P	
VDDO4	36	P	
VDDO5	40	P	
VDDO6	43	P	
VDDO7	49	P	
VDDO8	52	P	
VDDO9	57	P	

Pin Name	Pin Number	Pin Type[1]	Function
GND PAD		P	Ground Pad. This pad provides connection to ground and must be connected for proper operation.

Note:

1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.

10. Package Outlines

10.1 Si5386 9x9 mm 64-LGA Package Diagram

The following figure illustrates the package details for the Si5386. The table lists the values for the dimensions shown in the illustration.
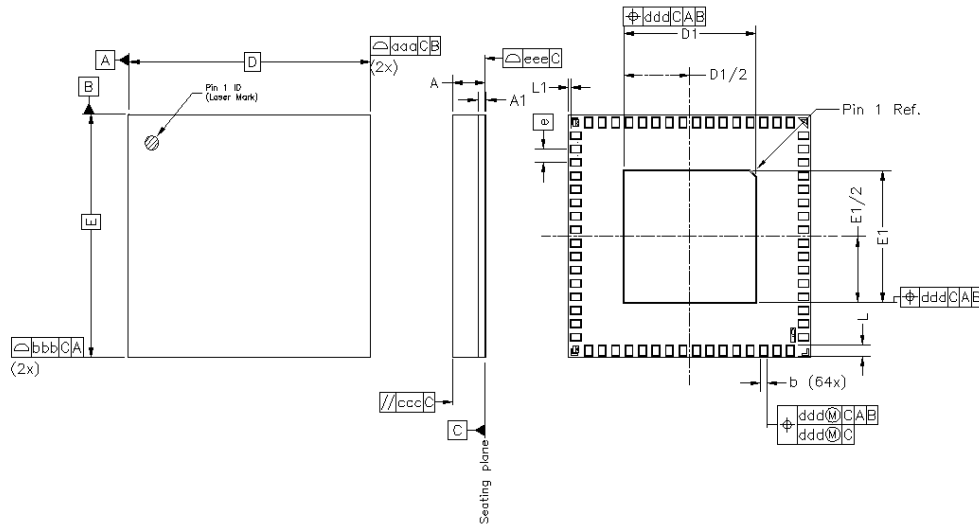
Figure 10.1. 64-Pin Land Grid Array (LGA)

Table 10.1. Package Dimensions

Dimension	MIN	NOM	MAX
A	1	1.1	1.2
A1	0.26 REF		
b	0.20	0.25	0.30
D	9.00 BSC.		
D1	5.5 BSC.		
e	0.50 BSC.		
E	9.00 BSC.		
E1	5.5 BSC.		
L	0.315	0.365	0.415
L1	0.03	0.08	0.13
aaa	--	--	0.10
bbb	--	--	0.10
ccc	--	--	0.2
ddd	--	--	0.10
eee	--	--	0.08

Dimension	MIN	NOM	MAX

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 Si5386 9x9 mm 64-QFN Package Diagram

Figure 10.2. Si5380 9x9 mm 64-QFN Package Diagram

Table 10.2. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	9.00 BSC		
D2	5.10	5.20	5.30
e	0.50 BSC		
E	9.00 BSC		
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern

The following figure illustrates the PCB land pattern details for the devices. The table lists the values for the dimensions shown in the illustration.
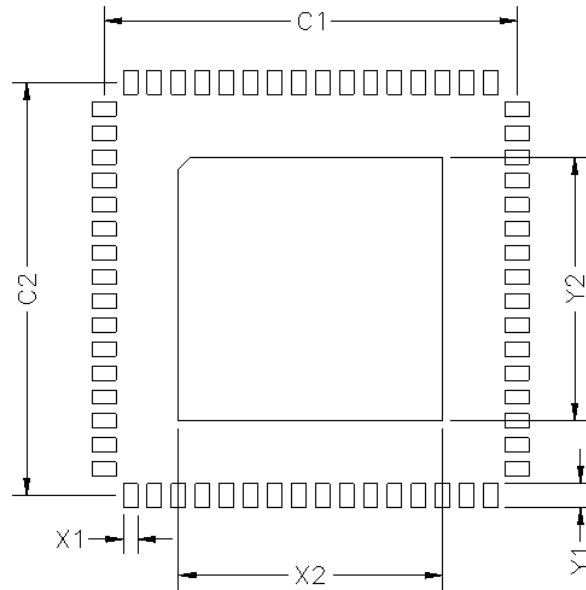
Figure 11.1. PCB Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Dimension	Si5386 (Max)
C1	8.6
C2	8.6
E	0.50
X1	0.30
Y1	0.50
X2	5.5
Y2	5.5

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electropolished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 0.65mm square openings on a 0.90mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Marking
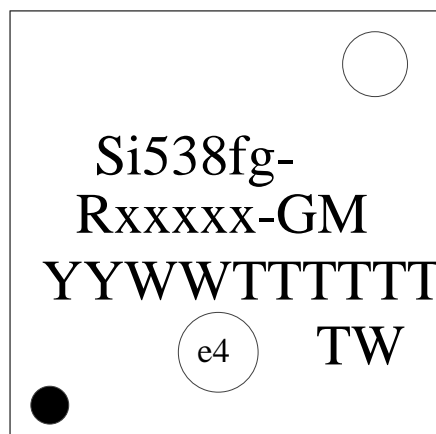
Figure 12.1. Si5386 Top Marking

Table 12.1. Top Marking Explanation

Line	Characters	Description
1	Si538fg-	Base part number and Device Grade for Any-frequency, Any-output, Jitter Cleaning Clock (single PLL): f = 6, 12-Output LTE + Ethernet Clock g = Grade (internal versus external crystal oscillator option) Si5386A = Grade A, 12-ouput wireless clock with external XO/Crystal Si5386E = Grade E, 12-output wireless clock with internal crystal oscillator
2	Rxxxxx-GM	R = Product revision. (Refer to 2. Ordering Guide for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See 2. Ordering Guide for more information. -GM = Package (LGA) and temperature range (–40 to +85 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm (64-QFN) diameter	Pin 1 indicator; left-justified
	e4	Pb-free symbol; Center-Justified
	TW	TW = Taiwan; Country of Origin (ISO Abbreviation)

13. Device Errata

Log in or register at https://www.silabs.com/support/resources.ct-errata.p-timing_clocks to access the device errata document.

14. Document Change List

14.1 Revision 0.9

September 2017
- Initial release.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

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