User's Guide
SPRUIE6–April 2017

AMIC110 Industrial Communications Engine (AMIC110 ICE)

This user's guide details the hardware architecture of the AMIC110 Industrial Communications Engine (AMIC110 ICE). The AMIC110 is a Sitara™ AMIC110 ARM® Cortex®-A8 processor System-on-Chip (SoC).

Contents

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1 Introduction

1.1 Key Features

The AMIC110 ICE is a high-performance, low-power platform that enables users to evaluate and develop industrial communications applications for the Sitara AMIC110 ARM Cortex-A8 processor SoC from Texas Instruments™. The AMIC110 SoC has the following key features:

- Sitara ARM Cortex-A8 32-bit RISC processor (up to 300 MHz)
- Two programmable real-time unit and industrial communication subsystems (PRU-ICSS)
- 64KB of general-purpose, on-chip memory controller (OCMC) RAM (shared L3 RAM)
- Supports protocols such as EtherCAT®, PROFIBUS, PROFINET, and Ethernet/IP™
- Two multichannel audio serial port (McASP) peripherals
- Two master and slave McASPI serial interfaces
- Three I^2C master and slave interfaces and six UART interfaces
- Eight 32-bit general-purpose timers
- Three enhanced high-resolution PWM modules (eHRPWMs)
- Three external DMA event inputs that can be used as interrupt inputs
- Three MMC, SD, and SDIO ports
- Two USB 2.0 high-speed OTG ports with integrated PHY
- 324-pin, S-PBGA-N324 package with 0.80-mm ball pitch

The AMIC110 ICE has the following key features:

- AMIC110 is based on the Sitara ARM Cortex-A8 32-bit RISC processor at 300 MHz
- 512MB of DDR3
- 8MB of SPI Flash
- 32KB of I^2C EEPROM
- Two 10/100 industrial Ethernet connectors with external magnetics
- RoHS compliant design
- 20-pin JTAG header to support all types of external emulators
- EMC compliant, industrial temperature dual-port EtherCAT slave with an SPI interface
- 5-V input supply, single-chip power management IC (TPS650250) to power the entire board
- AMIC110 can be configured to boot EtherCAT firmware from SPI Flash and also supports boot through the SPI host processor
- No DDR or other external RAM required when the EtherCAT slave stack runs on an external host processor (such as the C2000™)
- Texas Instruments™ LaunchPad™ compatible BoosterPack™ format
- 3.3-V SPI interface to C2000 F28069M LaunchPad

The AMIC110 ICE featured applications are:

- Industrial drivers
- Industrial sensors
- Factory automation and control

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1.2 Functional Block Diagram

Figure 1 shows the functional block diagram of the AMIC110 ICE device.

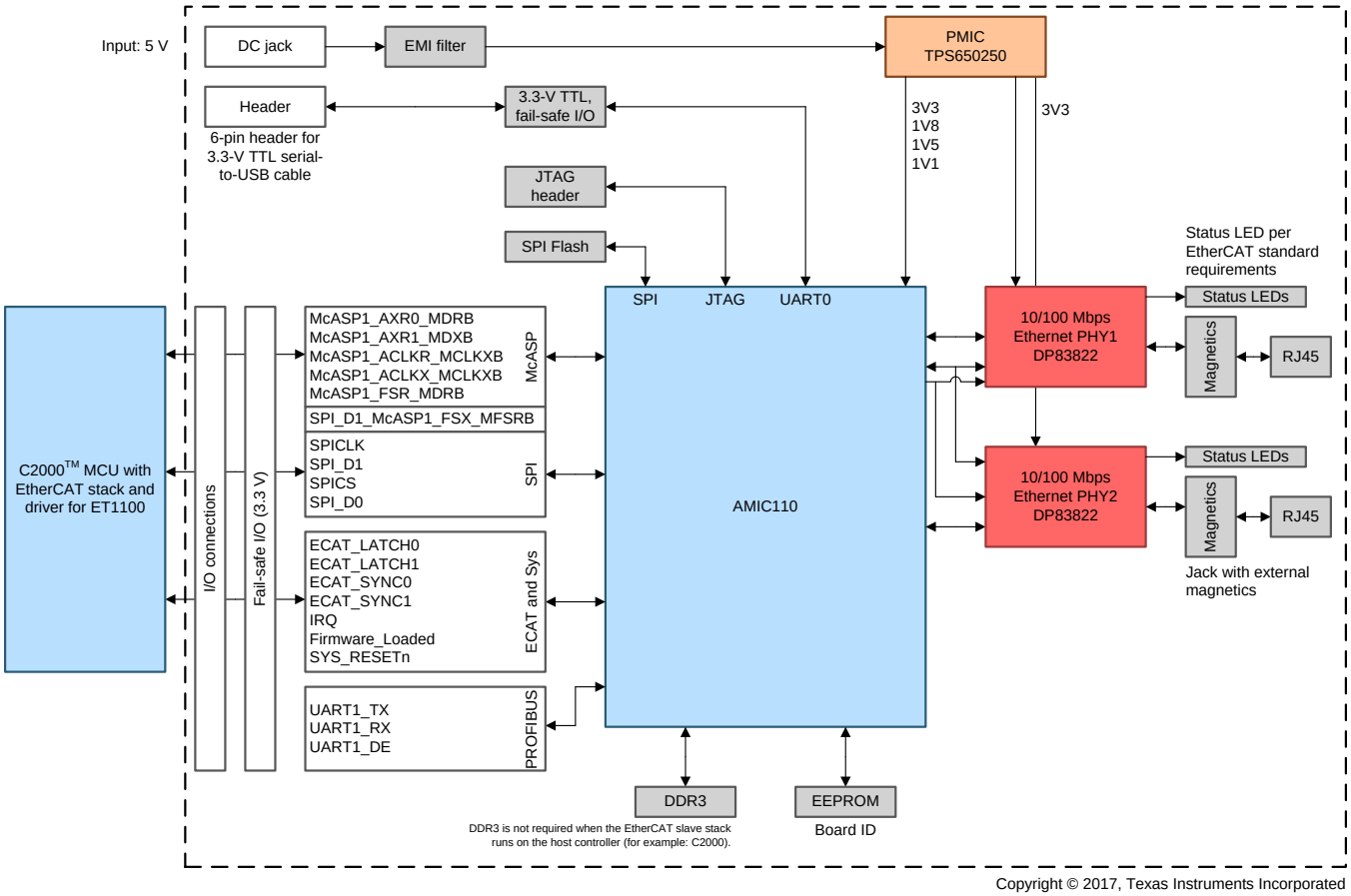

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Figure 1. AMIC110 ICE Functional Block Diagram

1.3 Basic Operation

For detailed information and resources on the AMIC110 ICE, see *TMDXICE110*.

Follow the steps in Section 1.3.1 and Section 1.3.2 to quickly get started with the AMIC110 ICE.

1.3.1 Hardware Setup

See the following steps to set up the hardware of the AMIC110 ICE.

1. Unbox the AMIC110 ICE and identify the components and connectors detailed in Section 3.
2. Connect a 20-pin JTAG emulator to J1 on the AMIC110 ICE (see Figure 2) to download a bootable image to the onboard SPI Flash. For example, XDS100 or XDS200 emulators may be used for this purpose and are available at *XDS110* and *XDS200*.

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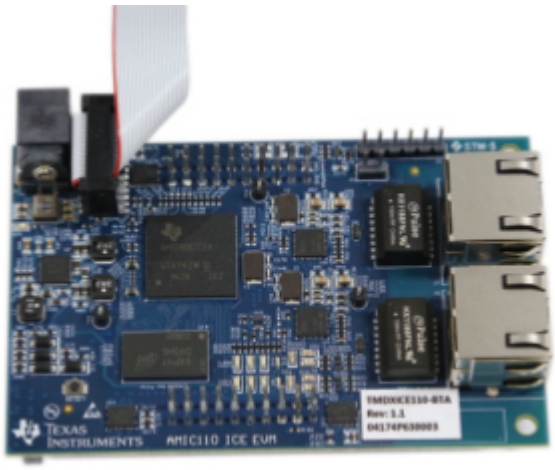

Figure 2. AMIC110 ICE JTAG Connection

3. Connect the pin header connector of the TTL-232R-3V3 serial cable to J3 on the AMIC110 ICE (see Figure 3). Ensure that pin 1 of the serial cable (black wire, marked with a triangle) is connected to pin 1 of J3 (indicated by a dot on the silk screen).

   See *TTL to USB Serial Converter Range of Cables Datasheet* for information about the TTL-232R-3V3 cable.
4. Connect the USB connector of the serial cable to a PC host port.
5. Connect a CAT5 Ethernet cable from a PC running TwinCAT software to PHY1 (J6 – ECAT IN) of the ICE board. If users have multiple ICE boards in a chain, connect another CAT5 Ethernet cable from PHY2 (J7 – ECAT OUT) to PHY1 of the next ICE board. PHY2 of the last ICE board in the chain is left open.

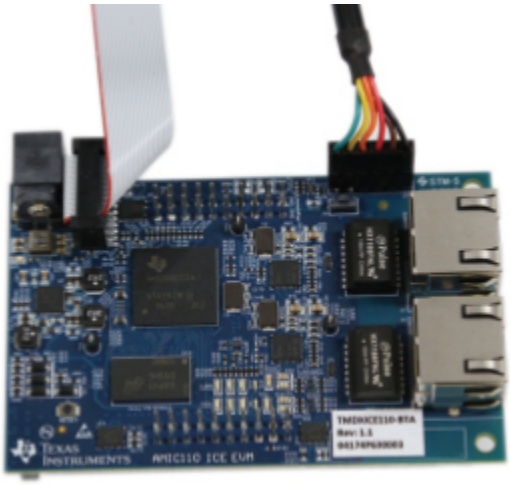

Figure 3. AMIC110 ICE Serial Port Connection

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6. Apply power to the power supply of the AMIC110 ICE as detailed in Section 1.4. Do not hot plug the 5-V supply into the ICE board.

Figure 4. AMIC110 ICE Power Supply Connection

1.3.2 Software Setup

See *AMIC110SW* for software setup.

1.4 Power Supply

Use the recommended power supply (*CUI Inc. SMI18-5-V-P5*) or an equivalent (output voltage and current: 5 V, DC ±10% at 1.2 A; output connector: 2.1-mm ID, 5.5-mm OD barrel plug, center positive) power supply to connect to J8 on the ICE board.

To apply power to the AMIC110 ICE, insert the DC plug of the power supply into the AMIC110 ICE. Then, connect the AC plug of the power supply to the AC power source. Hot plugging the AMIC110 ICE (connecting the AC plug before the DC plug) may damage the board.

To remove power from the AMIC110 ICE, disconnect the AC plug of the power supply from the AC power source. Then, disconnect the DC plug of the power supply from the AMIC110 ICE.

2 Interface Details

2.1 Boot Configuration

Various boot configurations can be set by using pullup and pulldown resistor combinations on the SYSBOOT inputs (LCD_DATA[15:0] pins). Boot configuration inputs are latched upon de-assertion of the PORz input (PWRONRSTn pin).

The default SYSBOOT settings for the AMIC110 ICE are 1000_0000_0001_1000b. These settings correspond to a boot sequence of SPI0, MMC0, USB0, and UART0.

See the SYSBOOT configuration pins section in *AM335x and AMIC110 Sitara™ Processors Technical Reference Manual* and the pin attributes table in *AMIC110 Sitara™ SoC* for the definitions of each SYSBOOT input.

Table 1 lists the AMIC110 ICE boot configuration pins. PD indicates a pulldown resistor is used to hold the respective SYSBOOT input low during reset. PU indicates a pullup resistor is used to hold the respective SYSBOOT input high during reset.

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Table 1. Boot Configuration Pins

SYSBOOT Input	Resistor
15	PU
14	PD
13	PD
12	PD
11	PD
10	PD
9	PD
8	PD
7	PD
6	PD
5	PD
4	PU
3	PU
2	PD
1	PD
0	PD

2.1.1 AMIC110 Bootstrap Hardware

Several Ethernet PHY1 (U3) signals are connected to AMIC110 pins that operate as SYSBOOT inputs. Two of the PHY1 signals must be isolated from AMIC110 SYSBOOT inputs during power on. A dual FET switch (U10) performs this task. The switch control inputs are connected to the MII1_RXD3 pin operating as GPIO2_18, which defaults to a high-z input with an internal pull-down after power is applied. The internal pull-down along with an external pull-down ensures the switch is off as soon as power is applied.

The SYSBOOT buffers (U8 and U9) have an active low enable controlled by the MII1_RXD2 pin operating as GPIO2_19, which defaults to a high-z input with an internal pull-down after power is applied. The internal pull-down along with an external pull-down ensures the buffer is enabled as soon as power is applied. The buffer over-drives any internal pull resistors in the Ethernet PHYs to ensure the SYSBOOT inputs are the value defined by the SYSBOOT resistor array.

The LCD_DATA[15:0] pins are the AMIC110 SYSBOOT inputs. These pins default to high-z inputs without any internal pull resistors turned on after power is applied. The value driven by SYSBOOT buffers will be sampled on the rising edge of the PWRONRSTn input. These values determine the boot mode of the AMIC110.

See the *AMIC110 ICE Schematic Files* for more details related to bootstrap hardware.

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2.2 Clock Distribution

Figure 5 shows the clock distribution circuit. Three 25-MHz crystals are used onboard. One 25-MHz crystal is connected to the AMIC110, the second crystal is connected to PHY1, and the third crystal is connected to PHY2.

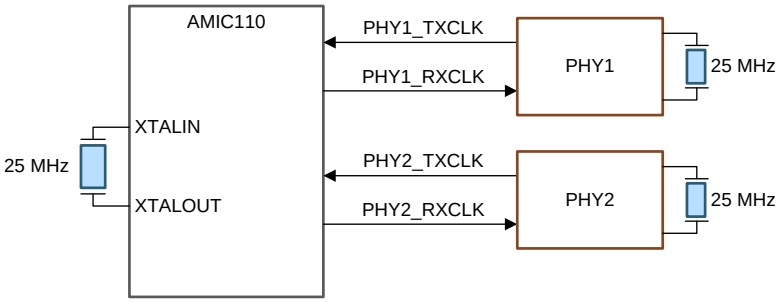

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Figure 5. Clock Distribution

2.3 Reset Circuit Distribution

Figure 6 shows the reset distribution. All devices on the AMIC110 ICE can be reset by the following:

- ICE onboard RESET button (SW1)
- Power ON reset signal from the PMIC

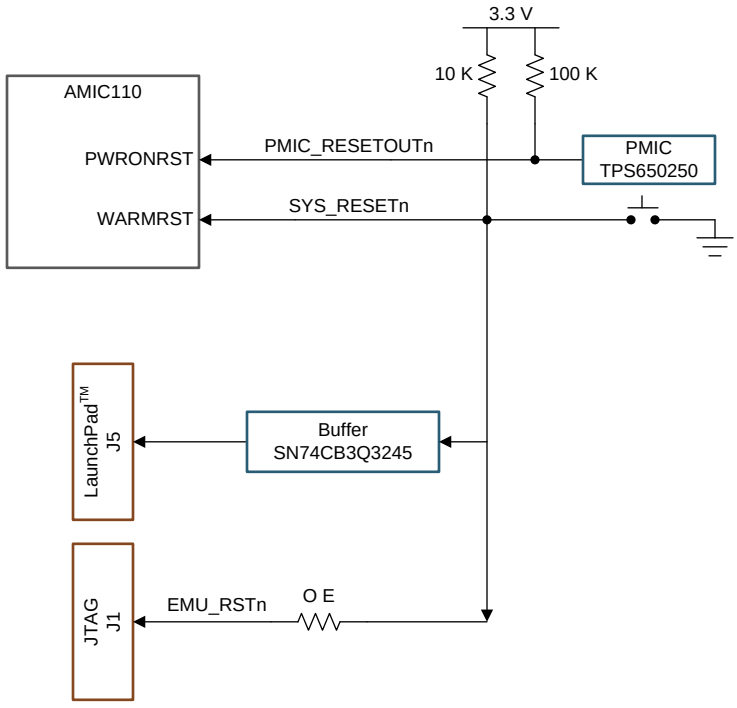

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Figure 6. Reset Distribution

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2.4 DP83822 – 10/100 Ethernet PHY

The AMIC110 includes two PRU-ICSSs, which can be configured to support numerous industrial protocols. The PRU subsystem supports two IEEE 802.3 Standard Media Independent Interface (MII) interfaces, which can be connected to 10/100 Ethernet PHYs. The AMIC110 ICE includes two DP83822 10/100 Ethernet PHYs, which provide two Ethernet connections (see Figure 7). The PHYs are implemented to support dual EtherCAT slave ports.

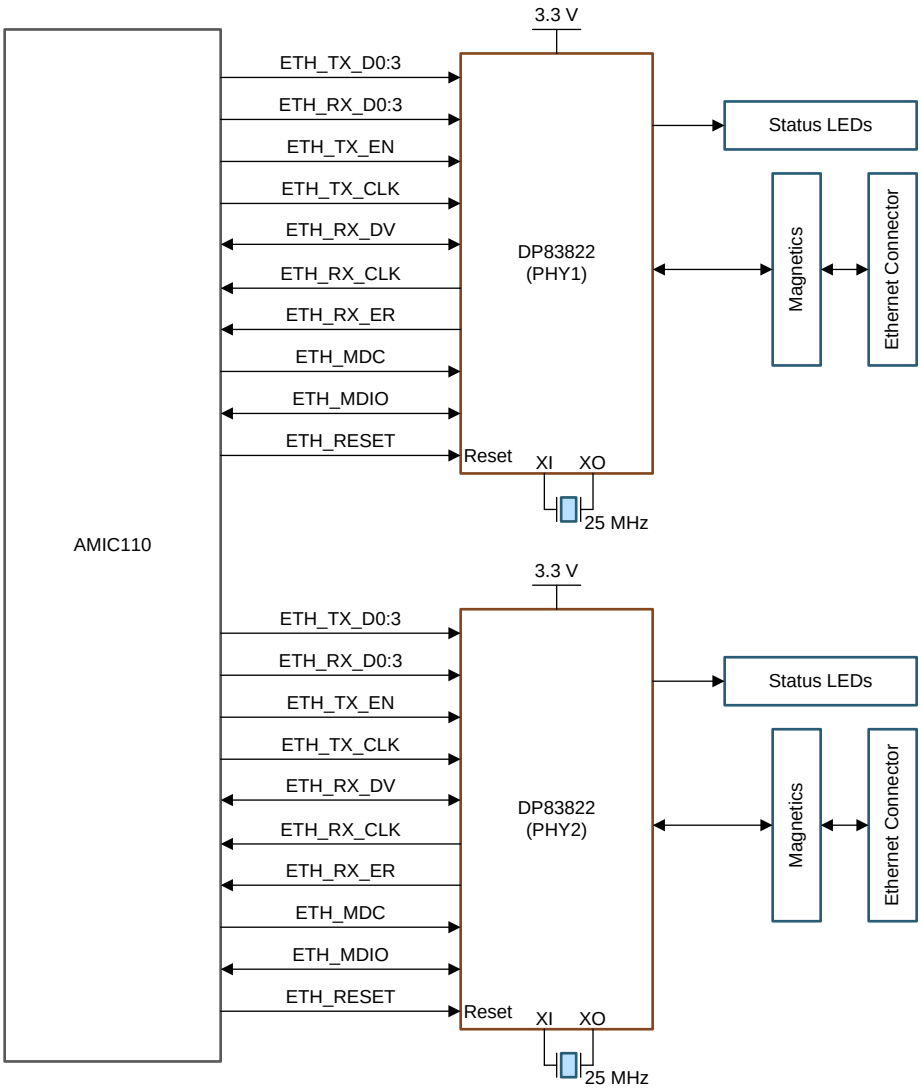

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Figure 7. Ethernet Interface Without Bootstrap Hardware

2.4.1 Industrial Ethernet PHY Default Configuration

The default configuration of the DP83822 is determined using a number of resistor pullup and pulldown values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes. A configuration pin or groups of configuration pins are used to set the configuration of the PHY after it is released from reset. Configuration settings differ depending on the package type selected for the PHY.

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2.4.2 Industrial Ethernet Resistor Strapping

The DP83822 PHY uses a four-level configuration based on resistor strappings, which generate four distinct voltages ranges. These resistors are connected to the RX data and control pins that are normally driven by the PHY and are inputs to the AMIC. The voltage ranges follow:

- Mode 1 – 0 V to 0.3234 V
- Mode 2 – 0.4884 V to 0.5973 V
- Mode 3 – 0.7491 V to 0.9141 V
- Mode 4 – 2.2902 V to 3.3 V

Mid-level voltages can result in high leakage currents and are detrimental to the long-term reliability of the AMIC 110 I/O cells connected to the strapping resistor. To avoid this situation, only pullup and pulldown resistors are used to pull the I/O cells as close as possible to 0 V or 3.3 V; this limits the selection of configurations to those that can be selected by using Mode 1 or Mode 4. The DP83822 device and the AMIC110 include internal pulling resistors. The values of the external pull resistors are selected to provide a voltage at the pins of the AMIC110 as close to ground or 3.3 V as possible.

2.4.3 Software Steps for Industrial Ethernet Resistor Strapping

The following steps should be performed before the AMIC110 pins are configured to operate in their intended application.

Software should maintain the power on default state for LCD_DATA[15:0] pins (except LCD_DATA6 and LCD_DATA7). LCD_DATA6 and LCD_DATA7 should have their internal pulldown resistors turned on; this holds the LCD_DATA6 and LCD_DATA7 pins in a valid logic state once the SYSBOOT buffers are turned off.

The GPMC_AD9 and LCD_PCLK pins should be in their power-on default configuration operating in their respective GPIO mode with internal pullown resistors turned on. Software should turn off the internal pull resistors on these pins; this prevents AMIC110 internal pull resistors from interfering with the bootstrapping of Ethernet PHY1.

The power on default state of the GPMC_A[11:0] and LCD_AC_BIAS_EN pins are configured to their respective GPIO mode with internal pulldown resistors turned on. The power-on default state of the GPMC_WPn and GPMC_WAIT0 pins are configured to their respective GPIO mode with internal pull-up resistors turned on. Software should turn off internal pull resistors on all of these pins to prevent AMIC110 internal pull resistors from interfering with the bootstrapping of Ethernet PHY2 (U5).

Next, software should configure GPIO2_19 to be an output that is driven high to turn off the SYSBOOT buffers. After a 100-µs delay, the GPMC_AD13 pin should be configured to operate as GPIO1_13 with its output enabled and driven high; this releases the reset to both Ethernet PHYs, allowing them to latch their bootstrap inputs.

After another delay of 100 µs, isolation switch U10 must be turned on by enabling the output of GPIO2_18 and driving it high.

The next step is to configure all AMIC110 pins to their intended application and execute the application code.

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Figure 8 shows the industrial Ethernet PHY1 strapping resistors.

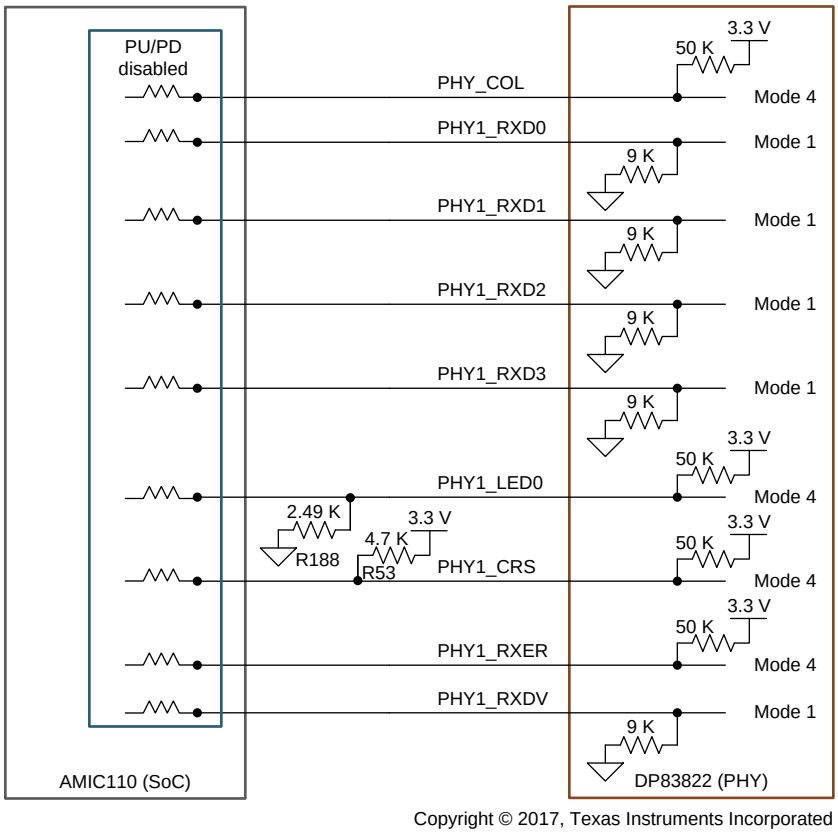

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Figure 8. Industrial Ethernet PHY1 Strapping Resistors

Table 2 lists the configurations for PHY1. See the hardware bootstrap configurations section of *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver* for more information.

Table 2. Ethernet PHY1 Strap Configuration

Strap Setting	Pin Name	Strap Function	Value of Strap Function	Description
Address	COL	PHY_AD0	1	1
	RX_D0	PHY_AD1	0	
	RX_D1	PHY_AD2	0	
	RX_D3	PHY_AD3	0	
Modes of operation	COL	FX_EN	0	10BASE-Te, half duplex 100BASE-TX, half duplex
	RX_D3	AN_EN	1	
	RX_D0	AN_1	1	
	LED_0	AN_0	0	
EEE operation	RX_D1	EEE_EN	0	Disabled
Fast link drop	RX_D2	FLD_EN	0	Disabled
Auto MDIX	RX_ER	AMDIX_EN	1	Disabled
MAC interface	RX_ER	RGMII_EN	0	MII, 24-MHz reference clock
	RX_DV	RMII_EN	0	
	RX_DV	XI_50	0	
LED_0	CRS	LED_CFG	1	ON for good link, OFF for no link
LED_1	CRS	LED_SPEED	0	Tri-state condition

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Figure 9 shows the industrial Ethernet PHY2 strapping resistors. As shown in Figure 9, PHY2 has an address of 13. All other PHY2 bootstrap settings are the same as PHY1.

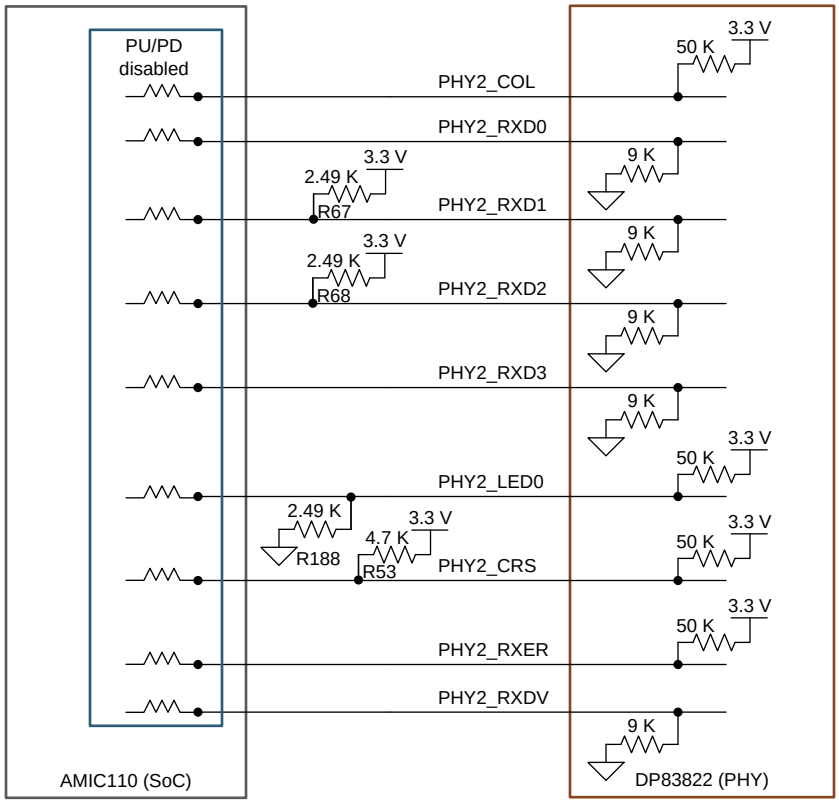

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Figure 9. Industrial Ethernet PHY2 Strapping Resistors

2.5 Ethernet Protocol Specific Indicator LEDs

The AMIC110 ICE was built with a focus on EtherCAT. The indicator LEDs enable multiprotocol operation. The following protocols were chosen to be included for potential updates for other RT Ethernet protocols.

- EtherCAT
- SERCOS-III
- PROFINET
- Ethernet/IP
- Powerlink

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Table 3 lists a summary of the required indicator LEDs for the five protocols.

Table 3. RT Ethernet Indicator LED Summary

LED		Powerlink	EtherCAT	Ethernet/IP	SERCOS-III	PROFINET
Link and activity LED	Color	Green (per port)	Green (per port)	Green (per port)	Green (per port)	Green (per port)
	Behavior	Solid on link; blink on activity	Solid on link; blink on activity	Solid on link; blink on activity (optional)	Solid on link	Solid on link; blink on command from PLC (not on activity)
Activity LED	Color	–	–	Orange (per port)	Orange (per port)	–
	Behavior	–	–	Blink on activity	Blink on activity	–
Status and error LED	Color	Bicolor: green and red	–	–	–	–
	Behavior	–	–	–	–	–
RUN LED	Color	–	Green	–	–	–
ERROR LED		–	Red	–	–	–
Module status		–	–	Bicolor: green and red	–	–
Network status		–	–	Bicolor: green and red	–	–
S LED		–	–	–	Tricolor: orange, green, and red	–
SD1 LED		–	–	–	Tricolor: orange, green, and red	–
ON	Color	–	–	–	–	Green
	Behavior	–	–	–	–	Device is on
BF	Color	–	–	–	–	Red
SF		–	–	–	–	Red
MT		–	–	–	–	Yellow

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Figure 10 shows the LED configuration on the AMIC110 ICE. To attain REACH compliance, the multicolor LEDs were separated to three single LEDs. This shows the LED functionality but must be combined with a lens or changed to a multicolor LED to comply with standards such as SERCOS-III, Ethernet/IP, and Powerlink. The parallel resistors R188, R189, R235, and R236 are required for the boot-time configuration of the PHY.

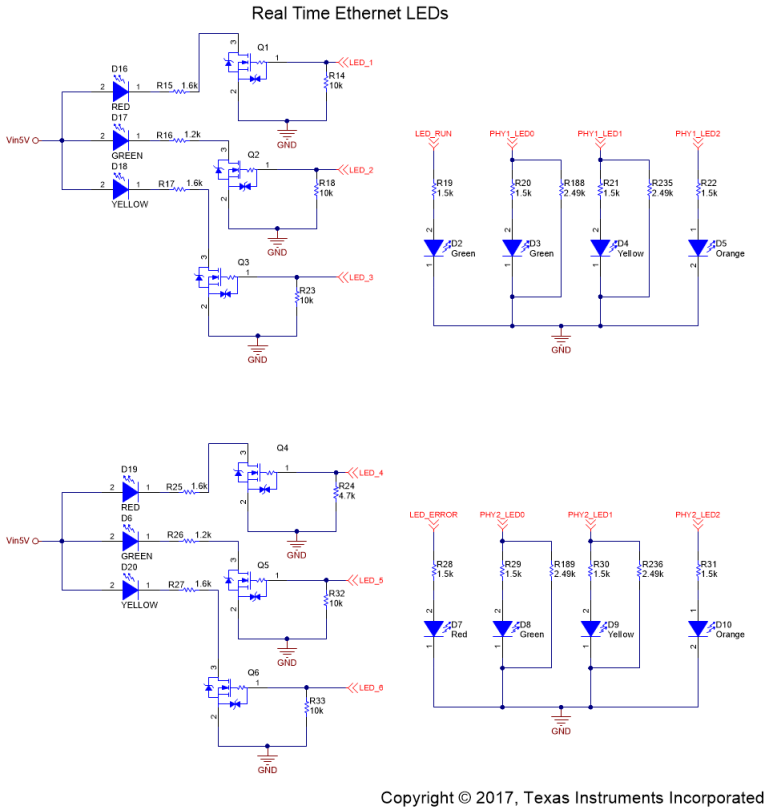

Figure 10. AMIC110 ICE Indicator LEDs

2.6 JTAG Emulation Circuit

The AMIC110 ICE supports a compact TI 20-pin connector in the design. An external emulator and debugger pod, such as the *XDS100* or the *XDS200*, may be connected to the 20-pin connector for JTAG connectivity. For more information on JTAG connections, see *JTAG Connectors*.

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2.7 Memory Interfaces

2.7.1 DDR3 Interface

The AMIC110 ICE supports one 4-Gb (256Mx16) DDR3 chip (MT41K256M16TW-107 from Micron) to obtain a memory size of 512MB. Figure 11 shows the DDR3 circuit.

NOTE: No DDR or other external RAM is required when the EtherCAT slave stack runs on an external host processor (such as the C2000).

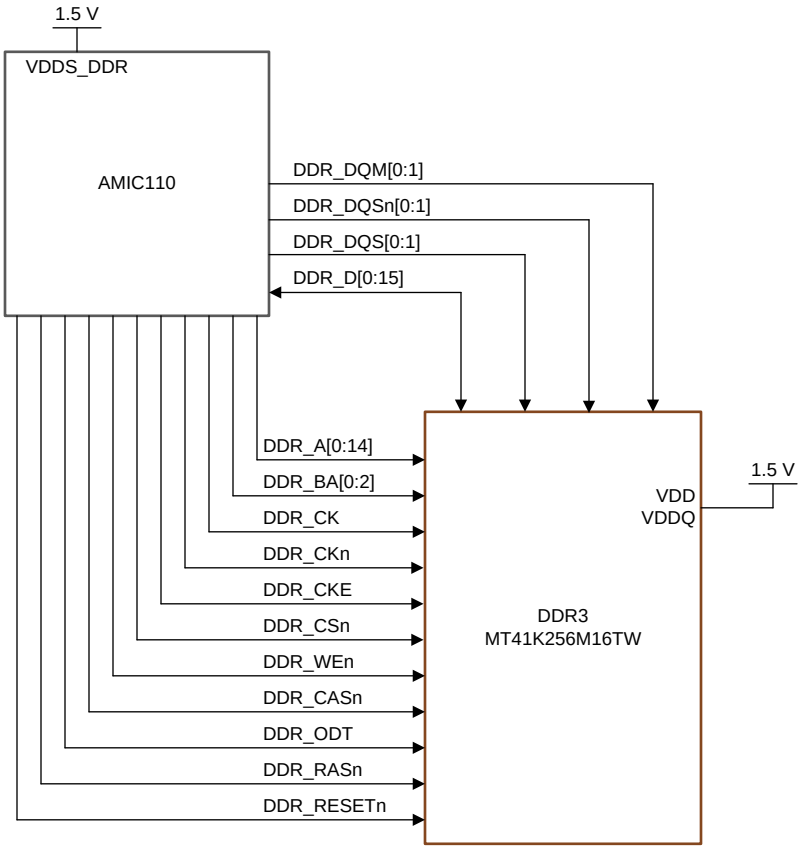

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Figure 11. DDR3 Interface

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2.7.2 DDR Timing Control and Software Leveling

See *AM335x DDR PHY register configuration for DDR3 using Software Leveling* for more information about software leveling.

Table 4 lists the seed values used as inputs to the Code Composer Studio™ (CCS) based application.

Table 4. Seed Values

Parameters		
DDR3 clock frequency	400	MHz
Invert Clkout	0	
Trace length (inches)		
	Byte 0	Byte 1
CK trace	0.94463	0.94463
DQS trace	0.915736	0.797452
Seed values (per byte lane)		
WR DQS	0	2
RD DQS	34	34
RD DQS GATE	67	62
Seed values to input to program		
WR DQS	0	
RD DQS	1A	
RD DQS GATE	32	

The following code snippet shows the optimum values obtained after running the DDR3_slave_ratio_search_auto.out file in CCS.

```
**************************************************
    The Slave Ratio Search Program Values are...
**************************************************************
PARAMETER                       MAX   |   MIN   | OPTIMUM |   RANGE
**************************************************************
    0x06d | 0x007 |  0x03a  | 0x066
DATA_PHY_FIFO_WE_SLAVE_RATIO   0x12c | 0x000 |  0x096  | 0x12c
DATA_PHY_WR_DQS_SLAVE_RATIO    0x070 | 0x003 |  0x039  | 0x06d
DATA_PHY_WR_DATA_SLAVE_RATIO   0x0a8 | 0x03b |  0x071  | 0x06d
**************************************************************
```


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2.7.3 SPI Flash

The AMIC110 ICE includes an 8-MB serial Flash (W25Q64FV from Winbond) that is interfaced to the AMIC110 (see Figure 12). The SPI port of the ICE is shared with the SPI Flash and the LaunchPad that is selected through chip select SPI0_CS0 and SPI1_CS0.

The hold function (to pause the serial communication without deselecting the device) is disabled with a pullup resistor attached to the HOLD# pin. Pullup options are provided for the write protect signal that is enabled in the default configuration.

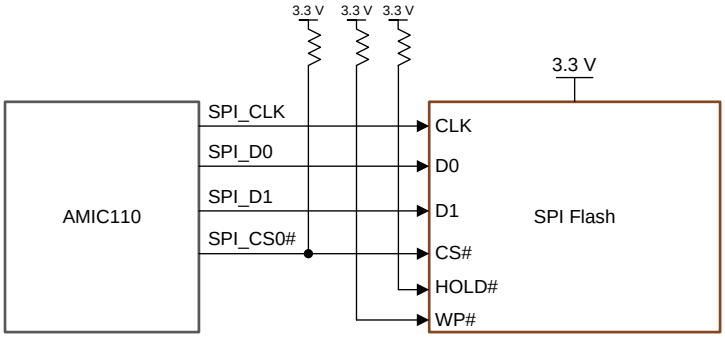

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Figure 12. SPI Flash Interface

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2.7.4 CAT24C256 EEPROM Board ID Memory

The AMIC110 ICE is identified by its version and serial number, which are stored in the onboard EEPROM. The EEPROM is accessible on the address 0x50.

The AMIC110 ICE includes a CAT24C256W I^2C EEPROM ID memory. The first 72 bytes of addressable EEPROM memory are preprogrammed with identification information for each board. The remaining 32696 bytes are available to the user for data or code storage.

NOTE: The first 72 bytes of addressable EEPROM memory should never be overwritten.

Table 5 lists the ID memory header information.

Table 5. ID Memory Header Information

Name	Size (Bytes)	Contents	Description
Header	4	MSB 0xEE3355AA LSB	Start code
Board name	8	ICE110	Board name in ASCII
Version	4	1.1	Hardware revision code in ASCII
Serial number	12	WWYY4P63nnnn	WW – week of production YY – year of production 4P63 – AMIC110 ICE code nnnn – serial number
Configuration option	32		Reserved for board configuration codes.
Available	32696		Available space for user data or code.

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3 AMIC110 ICE Physical Specifications

3.1 Board Layout

The ICE board has dimensions of 2.204 inches × 3.464 inches (56 mm × 88 mm), and is an 8-layer board fabricated with epoxy fiberglass FR4 grade material. Figure 13 shows the top view of the AMIC110 ICE.

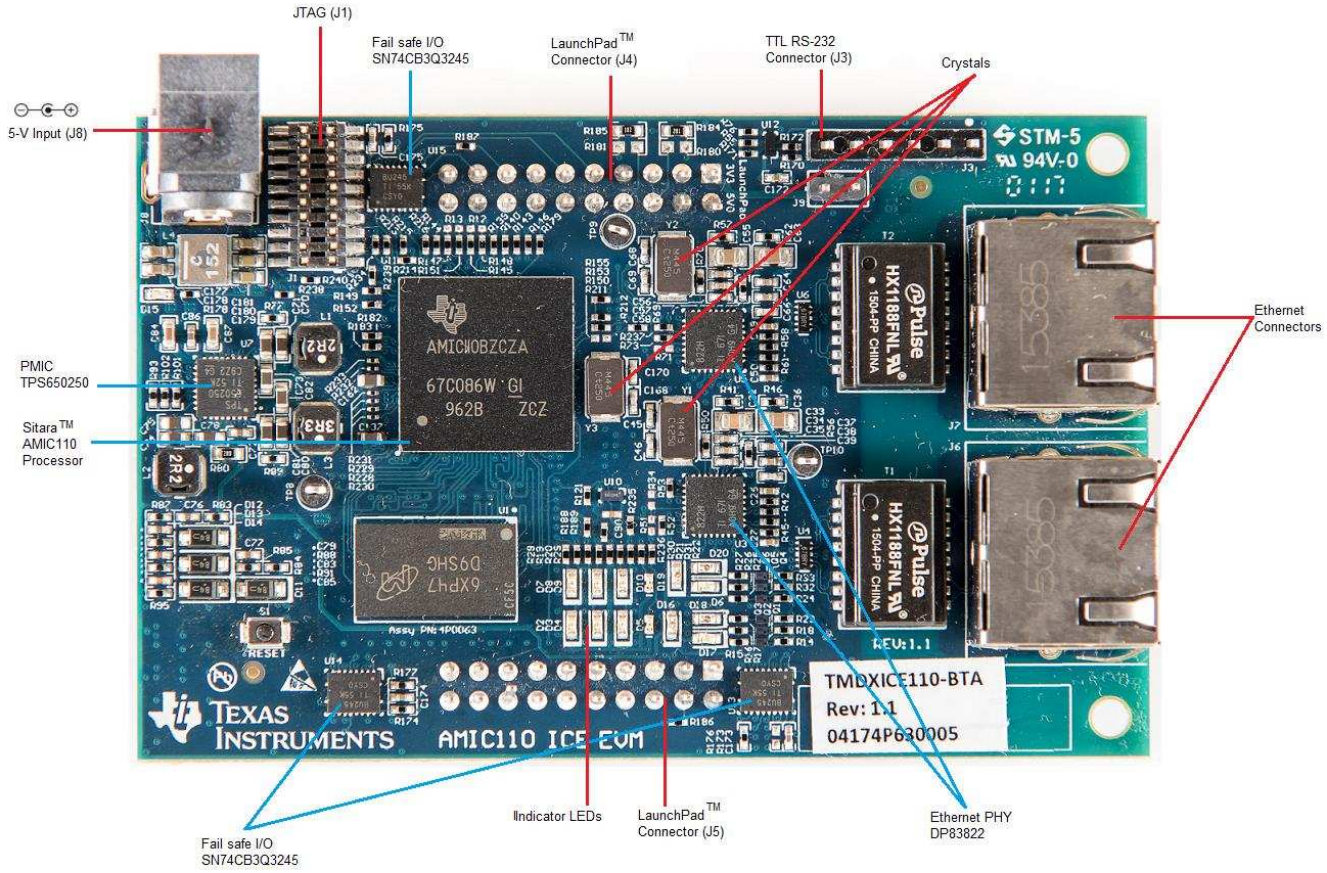

Figure 13. AMIC110 ICE (Top)

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Figure 14 shows the bottom view of the AMIC110 board.

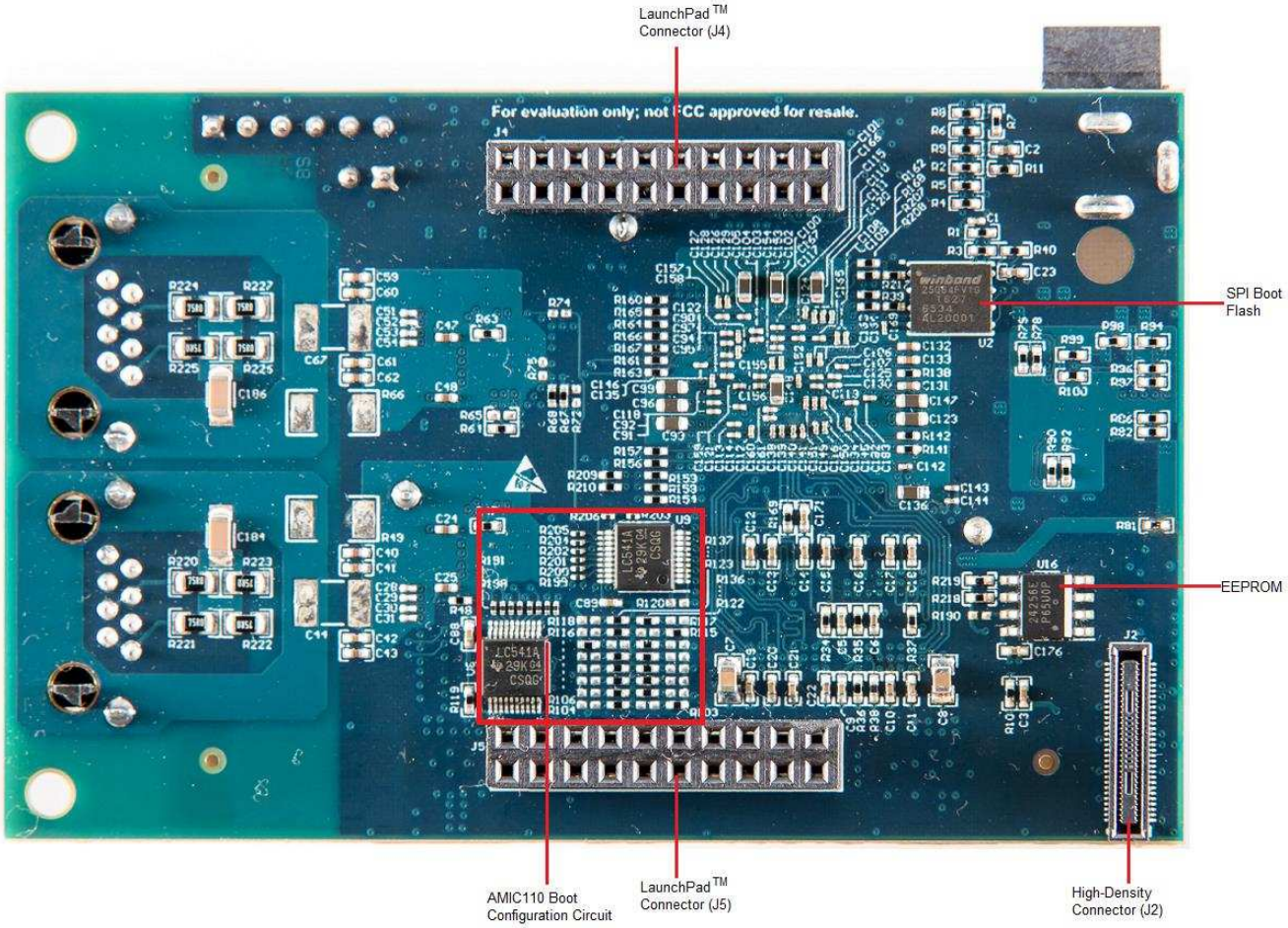

Figure 14. AMIC110 ICE (Bottom)

3.2 Connector Index

The AMIC110 ICE has several connectors that provide access to various interfaces on the board; Table 6 lists these connectors.

Table 6. AMIC110 ICE Connectors

Connector	Part Number	Pins	Function
J1	FTR-110-51-S-D-06	20	JTAG Header
J2	DF40HC(4.0)-60DS-0.4V(51)	60	High Density Interface Connector
J3	PEC06SAAN	6	UART Header
J4,J5	SSW-110-23-F-D	20	LaunchPad Headers
J7, J8	1-406541-1	8	Ethernet Connectors

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3.2.1 JTAG Header

Table 7 lists the JTAG header pinout information.

Table 7. JTAG Header Pinout

Pin Number	Description	Pin Number	Description
1	JTAG test mode select	2	Reset
3	JTAG test data input	4	JTAG test data select
5	Power supply	6	NC
7	JTAG test data output	8	Ground
9	Return Clock	10	Ground
11	Clock into the core	12	Ground
13	Emulation 0	14	Emulation 1
15	Emulation Reset	16	JTAG test data output
17	Emulation 2	18	Emulation 3
19	Emulation 4	20	Ground

3.2.2 UART Header

Table 8 lists the UART header pinout information.

Table 8. UART Header Pinout

Pin Number	Description
1	Ground
2	NC
3	NC
4	UART receive
5	UART transmit
6	NC

3.2.3 High Density Interface Connector

Table 9 lists the high density interface connector pinout information.

Table 9. High Density Interface Connector Pinout

Pin Number	Description	Pin Number	Description
1	NC	2	Ground
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	Ground	10	NC
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	EtherCAT ready signal	20	Ground
21	NC	22	NC
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	Chip-select signal; active low	30	Ground

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Table 9. High Density Interface Connector Pinout (continued)

Pin Number	Description	Pin Number	Description
31	Data output for serial communication	32	Clock for serial communication
33	NC	34	Data input for serial communication
35	NC	36	NC
37	NC	38	NC
39	NC	40	NC
41	Ground	42	NC
43	EtherCAT clock latch for PHY2	44	EtherCAT clock latch for PHY1
45	NC	46	NC
47	EtherCAT clock synchronization for PHY2	48	EtherCAT clock synchronization for PHY1
49	NC	50	EtherCAT interrupt signal
51	Power supply	52	Ground
53	NC	54	Power supply
55	Power supply	56	NC
57	NC	58	Power supply
59	Input to reset LP	60	NC

3.2.4 LaunchPad Headers

Table 10 lists the LaunchPad header pinout for J4.

Table 10. J4 LaunchPad Header Pinout

Pin Number	Description	Pin Number	Description
1	Power supply	2	Power supply
3	NC	4	Ground
5	EtherCAT Clock synchronization for PHY1	6	Analog input 0
7	EtherCAT Clock synchronization for PHY2	8	Analog input 1
9	UART 1 Receive	10	NC
11	GPIO	12	NC
13	Clock for serial communication	14	NC
15	Chip-select signal; active low	16	NC
17	UART1 data enable	18	NC
19	UART 1 Transmit	20	NC

Table 11 lists the LaunchPad header pinout for J5.

Table 11. J5 LaunchPad Header Pinout

Pin Number	Description	Pin Number	Description
1	Data transmit and receive	2	Ground
3	Data transmit and receive	4	Chip-select signal; active low
5	Clock receive for serial communication	6	GPIO
7	Frame synch for receive	8	NC
9	EtherCAT clock latch for PHY1	10	NC
11	EtherCAT clock latch for PHY2	12	Data output for serial communication
13	EtherCAT ready signal	14	Data input for serial communication

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Table 11. J5 LaunchPad Header Pinout (continued)

Pin Number	Description	Pin Number	Description
15	NC	16	NC
17	NC	18	Reset
19	NC	20	EtherCAT interrupt signal

4 Power Supply

The AMIC110 ICE can be powered from a single +5-V DC adapter. Do not hot plug the +5-V supply into the AMIC ICE; follow the instructions in Section 1.4 for plugging and unplugging the power supply. The +5-V input is converted into the required supply voltages using a PMIC.

The TPS650250RHBR PMIC (U7) provides the required voltages and currents for all power rails of the AMIC110 processor (see Table 12).

Table 12. TPS650250 Power Rail Split to AMIC110

Rail	TPS650250	AMIC110
1.1 V	DCDC1	VDD_CORE, VDD_MPU, VDD_RTC
1.5 V	DCDC2	VDDS_DDR
1.8 V	VLDO1	VDDS_SRAM_MPU_BB, VDDS_SRAM_CORE_BG, VDDA_ADC, VDDS_PLL_DDR, VDDS_PLL_MPU, VDDS_PLL_CORE_LCD,VDDS_OSC, VDDA1P8V_USB0, VDDA1P8V_USB1
1.8 V	VLDO2	VDDS,VDDS_RTC
3.3 V	DCDC3	VDDA3P3V_USB0, VDDA3P3V_USB1, VDDSHVx

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4.1 Power Distribution

Figure 15 shows the power distribution diagram.

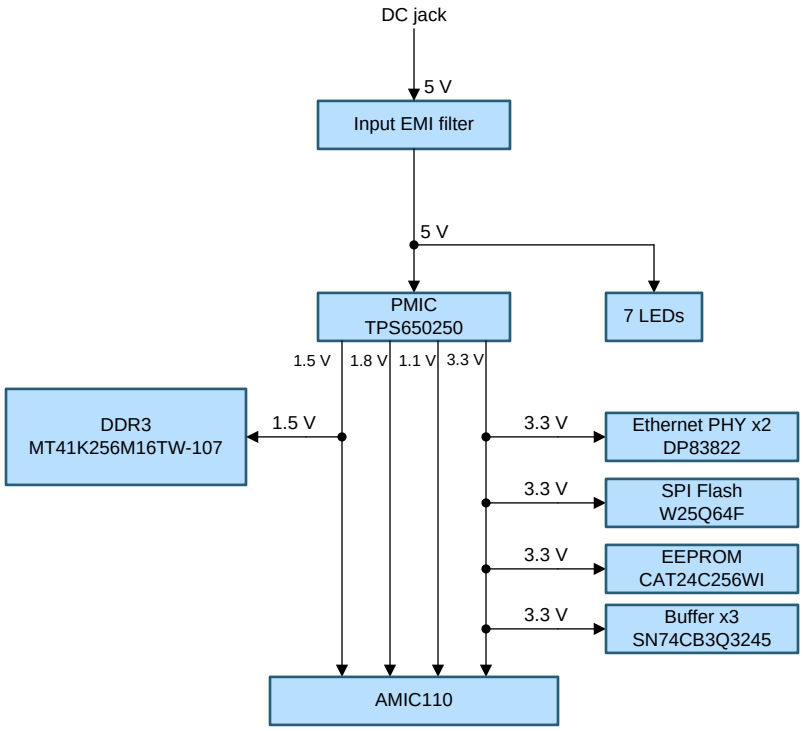

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Figure 15. Power Distribution Diagram

4.2 Sitara AMIC110 Current Consumption

AM335x Power Consumption Summary was used for the worst-case estimates of the AMIC110 power requirements. The power requirements from the *3D Chameleon Man* example were used because that was the example with the highest power consumption.

Table 13 lists the current consumption requirements of the AMIC110 including DDR3.

Table 13. Current Consumption Requirements of AMIC110 (Including DDR3)

Rail	Sitara AMIC110	DDR3
1.1 V	≈ 420 mA	
1.5 V(1)	≈ 120 mA	≈ 140 mA
1.8 V	≈ 33 mA	
3.3 V	≈ 34 mA	

(1) DDR3 interface using 1.5 V.

4.3 Additional Components – Current Consumption

Several additional components must be calculated to evaluate the power consumption of the 3.3-V rail. These components include:

- Glue logic between AMIC110 and DP83822
- Status LEDs for EtherCAT
- SPI Flash for booting the AMIC110
- Switching losses on I/O lines

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The glue logic is required to ensure the functionality of the AMIC110 boot sequence and to ensure that two outputs are not driving against each other at startup (the SN74LVC541AD buffer and SN74LVC2G66 dual switch provide this functionality).

Approximately 10 LEDs are used as the status LEDs of the real-time Ethernet protocols. Each LED draws 2 mA of current.

The Flash used is the W25Q64 from Winbond. The worst case current consumption of the W25Q64 is 25 mA according to the device datasheet.

Equation 1 was used to calculate the I/O switching loss of a line connected to a single AMIC110 pin.

$$P_{I/Oout} = (C_{OUT} \times (V_{I/O})^2 \times f) = 25\ MHz \times 3.3\ V^2 \times 20\ pF = 5.4\ mW \quad (1)$$

The I/O capacitance is approximated as the typical load capacitance of the PRU pins of the AMIC110, as specified in the *AMIC110 Sitara™ SoC* data sheet. The MII signals have a 25-MHz clock frequency. There is approximately 1.67 mA of drive current per 3.3-V I/O pin. Approximately 50 pins are used in this design.

Table 14 lists the current consumption requirements of the external circuit and estimated I/O switching losses.

Table 14. Current Consumption Requirement of External Circuit and I/O Switching Losses

Rail	Flash	Glue Logic	LEDs	I/O Switching Losses
3.3 V	≈ 25 mA	≈ 10 mA	≈ 20 mA	≈ 83 mA

4.4 Overall System Current Consumption

Table 15 lists the system current requirements.

Table 15. System Current Requirements

Rail	Sitara	DDR3	DP83822	External Circuit
1.1 V	≈ 420 mA			
1.5 V(1)	≈ 120 mA	≈ 140 mA		
1.8 V	≈ 33 mA			
3.3 V	≈ 34 mA		≈159 mA	≈ 138 mA

(1) DDR3 interface using 1.5 V.

Table 16 lists the summary of overall current requirements.

Table 16. Overall Current Requirements Summary

Rail	Current
1.1 V	≈ 420 mA
1.5 V(1)	≈ 260 mA
1.8 V	≈ 33 mA
3.3 V	≈ 331 mA

(1) DDR3 interface using 1.5 V.

4.5 TPS650250 Power Dissipation

The TPS650250 PMIC is designed to provide the required voltages and currents for all power rails of the AMIC110 processor (see *Powering the AM335x With the TPS650250*).

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For the power dissipation calculations in Table 17, Equation 2 was used for the switch mode power supplies (SMPS) and Equation 3 for the LDOs.

$$P_{SMPS} = ((V_{OUT} \times I_{OUT}) / \eta) - V_{OUT} \times I_{OUT} \quad (2)$$

$$P_{LDO} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

Table 17. PMIC Power Dissipation

Rail	TPS650250 Maximum Current	Topology	Current	Power Dissipation
1.1 V	1600 mA	SMPS	≈ 420 mA	0.12 W
1.5 V	800 mA	SMPS	≈ 260 mA	0.1 W
1.8 V	400 mA	LDO	≈ 33 mA	0.1 W
3.3 V	800 mA	SMPS	≈ 331 mA	0.28 W

For the calculations in Table 17, SMPS efficiency was assumed to be 80%.

The total power dissipation of the TPS650250 is 0.6 W.

4.6 Measured Power Consumption of System

The measured power consumption test was performed while running the EtherCAT slave firmware on the AMIC110 ICE connected to a TwinCAT3 terminal on the PC. Table 18 lists the measured system power consumption.

Table 18. Measured System Power Consumption

Rail	Current Consumption	Power Consumption
1.1 V	349 mA	0.384 W
1.5 V	35.8 mA	0.054 W
1.8 W	26.23 mA	0.047 W
3.3 V	128 mA	0.422 W

The power consumption was measured by removing the 0-Ω resistors attached to each power rail and measuring with a multimeter over the removed resistor. See the *AMIC110 ICE Schematic Files* for resistor details.

A multimeter was connected at the 5-V input to measure the input current.

The total power consumption of the board is 0.907 W. The total supply current from the 5-V system power supply is 248 mA, giving an input power of 1.240 W from the 5-V rail; this means that the overall efficiency of the TPS650250 is around 78% for the complete system, with 0.333 W of power dissipation in the TPS650250 package.

Using the given package thermal performance from the datasheet, use Equation 4 to calculate the expected temperature increase of the part.

$$T_{TPS650250} = R_{\theta JA} \times P_{Dissipation} = 34°C/W \times 0.333\ W \approx 11.7°C \quad (4)$$

At 85°C ambient, the estimated junction temperature is 96.7°C.

The maximum operating junction temperature of the TPPS650250 is 125°C. If running the TPS650250 at 85°C ambient temperature, the device could dissipate 1.18 W without forced cooling.

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4.7 Thermal Test

A thermal image was taken of the board while running the EtherCAT slave (see Figure 16). This image is used see if there are thermal hot spots on the design.

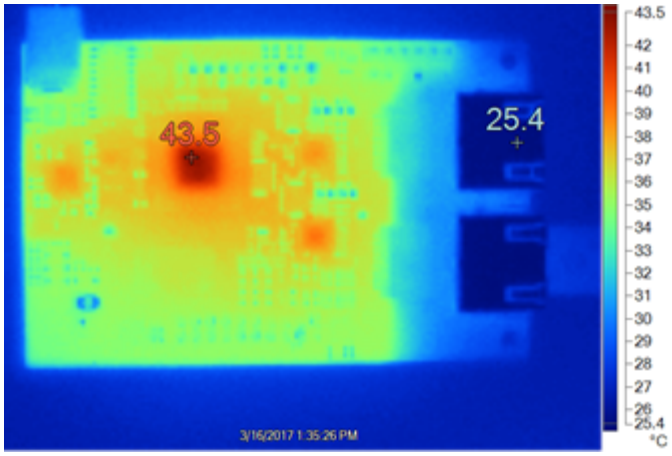

Figure 16. Thermal Image of AMIC110 ICE

The power supply heats up to approximately 37°C (shown in Figure 16). The hottest spot on the board is the AMIC110 device, which has a temperature rise of 18.1°C.

4.8 Power-Up Sequence

Figure 17 shows the required power-up sequence for the processor.

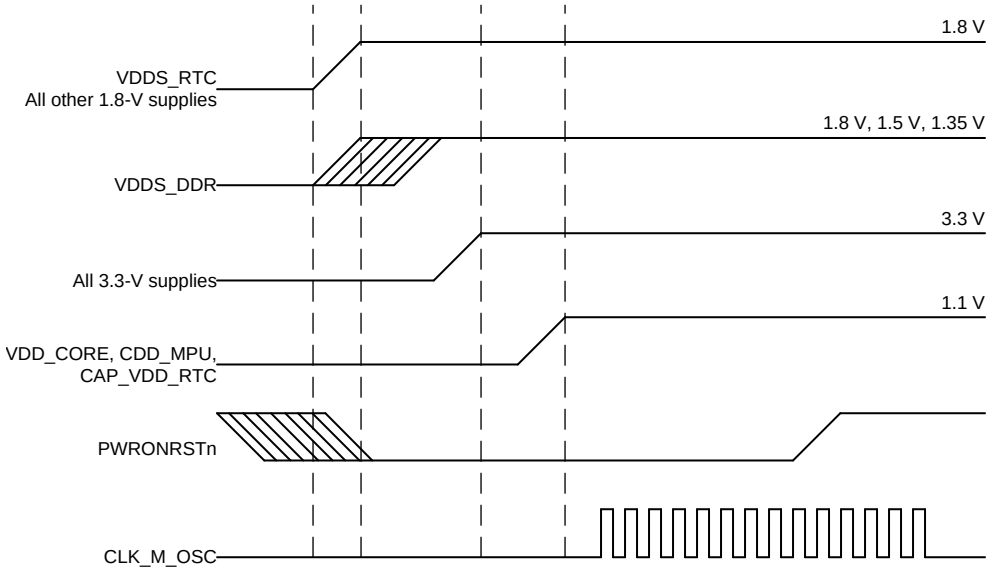

Figure 17. Power-Up Sequence

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4.9 Power-Up Behavior of Onboard Supply Rails

Figure 18 shows the power-up sequence with the reset signal and the 1v1, 1v5, and 3v3 rails.

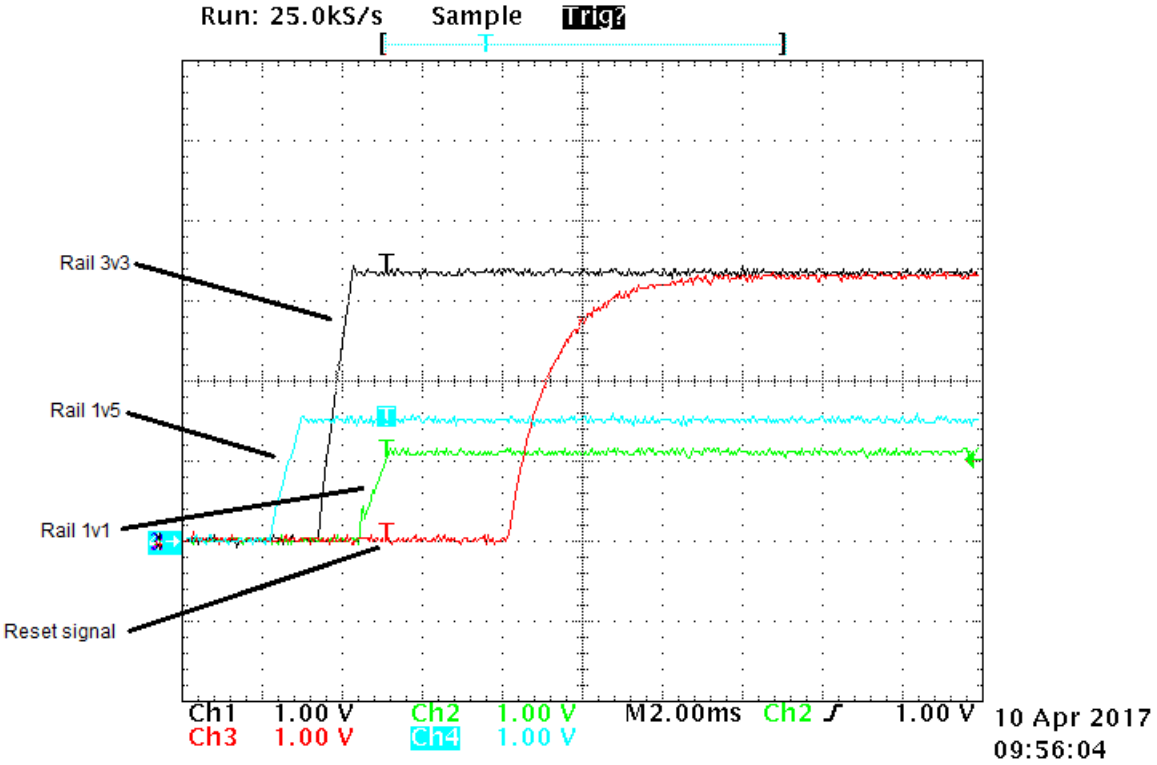

Figure 18. Power-Up Sequence (Reset and 1v1, 1v5, and 3v3 Rails)

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Figure 19 shows the power-up sequence with the reset signal and 1v5, 1v8_x, and 3v3 rails. Rails 1v8_1 and 1v8_2 were measured at the same time. They are identical for both the power-up and power-down sequences. Thus, the 1v8 rails are denoted as 1v8_x in Figure 19 through Figure 21.

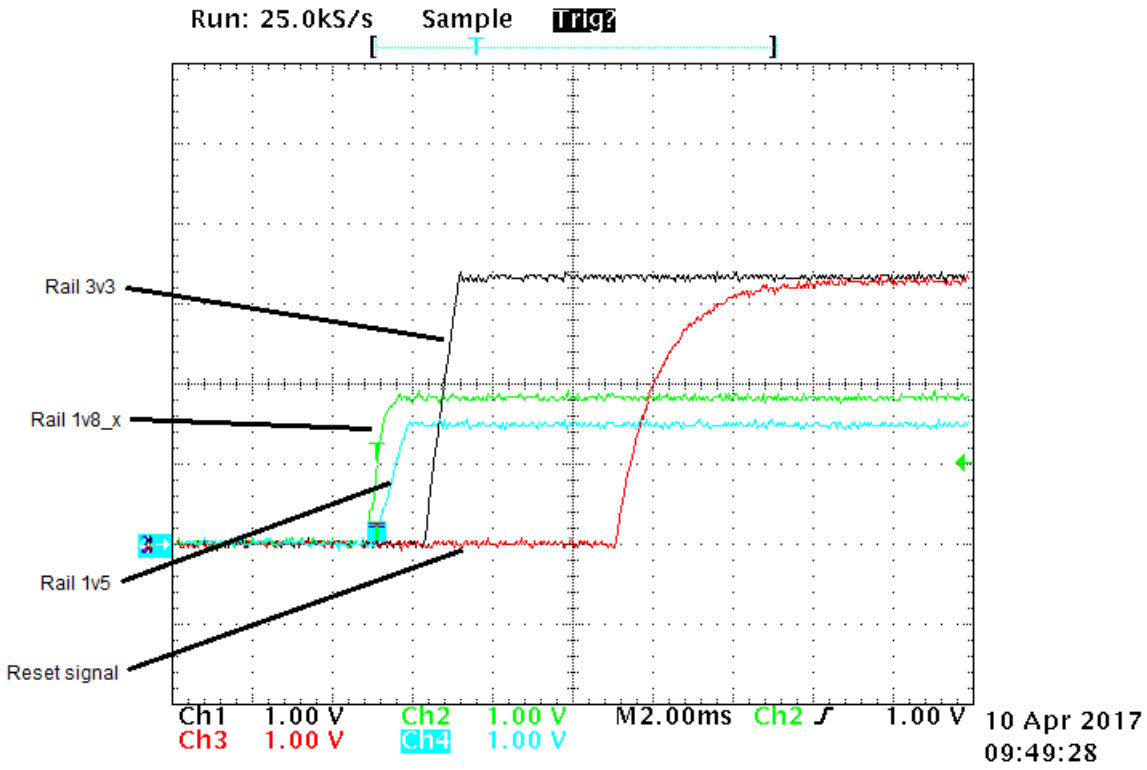

Figure 19. Power-Up Sequence (Reset and 1v5, 1v8_x, and 3v3 Rails)

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4.10 Power-Down Behavior of Onboard Supply Rails

Figure 20 shows the power-down sequence with the reset signal and the 1v1, 1v8_x, and 3v3 rails.

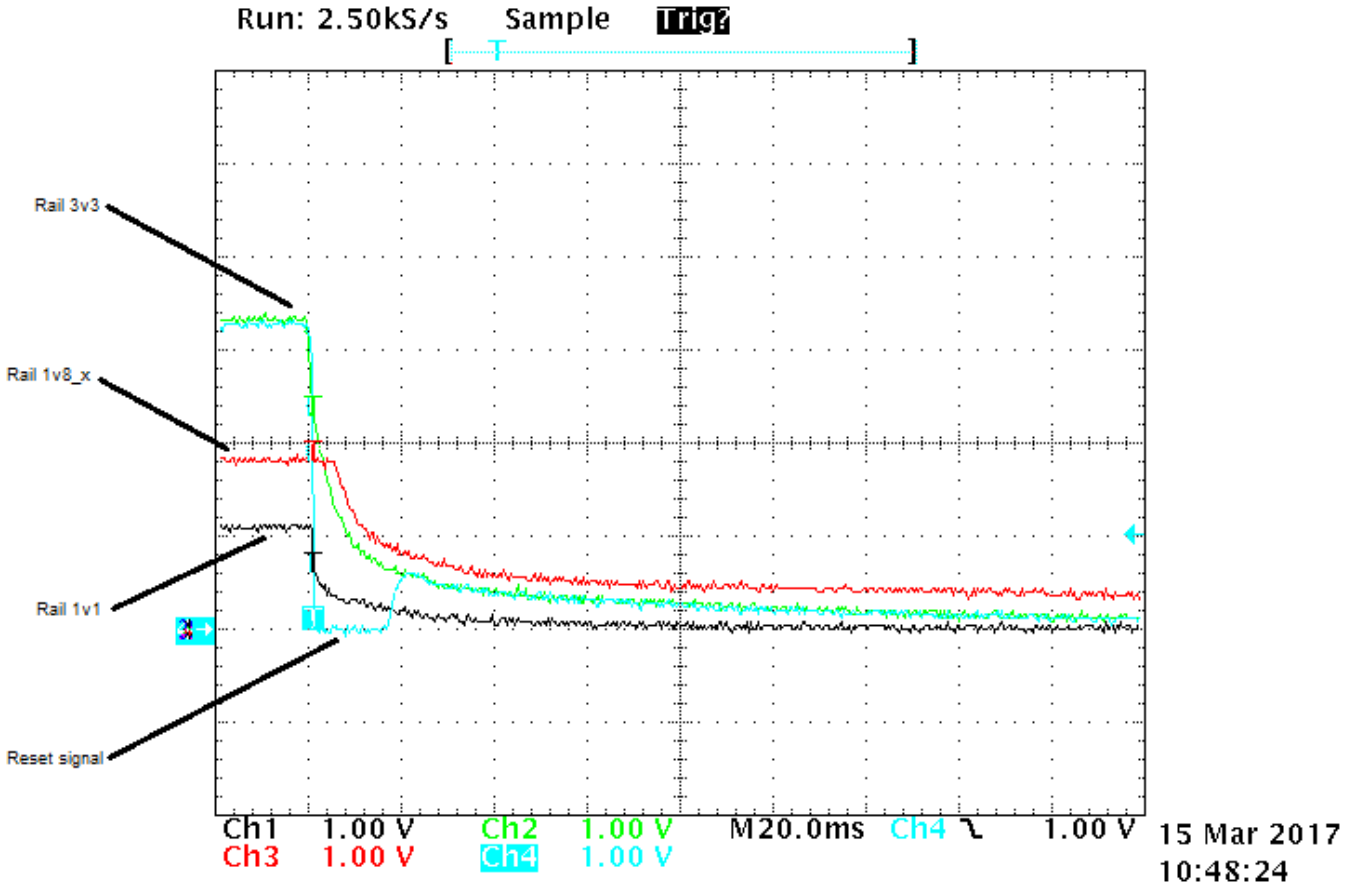

Figure 20. Power-Down Sequence (Reset and 1v1, 1v8_x, and 3v3 Rails)

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Figure 21 shows the power-down sequence with the reset signal and the 1v5, 1v8_x, and 3v3 rails.

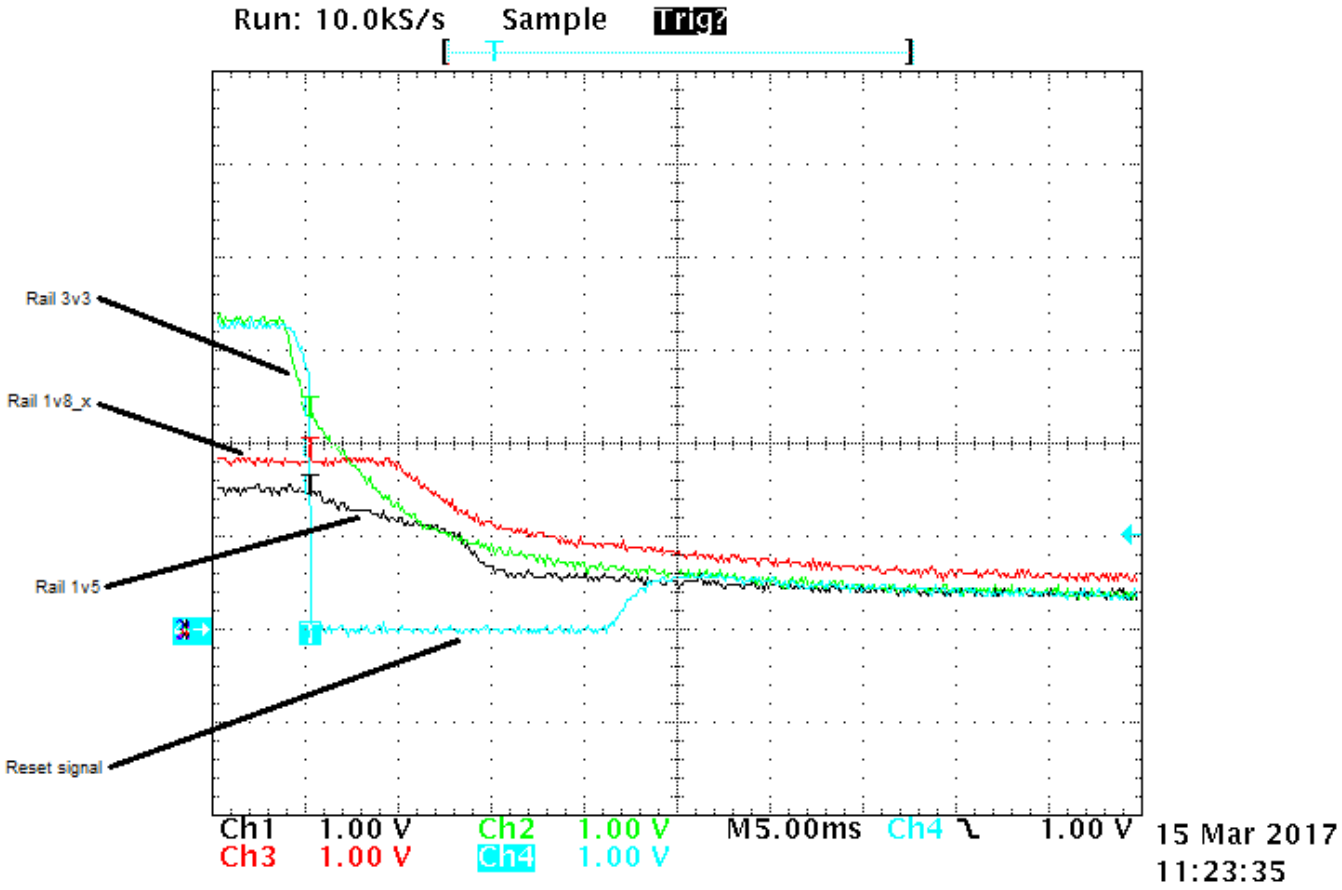

Figure 21. Power-Down Sequence (Reset and 1v5, 1v8_x, and 3v3 Rails)

5 Known Issues

There are no known issues for the AMIC110 ICE.

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A.1 Connecting AMIC110 ICE to LaunchPad Devices

Two 2 × 10, 2.54-mm headers are provided to connect to LaunchPad boards. The following instructions detail connecting the AMIC110 ICE to the F28069M LaunchPad.

1. Insert the AMIC110 ICE headers (J4 and J5) to the F28069M LaunchPad headers (J1, J3, J2, and J4). See Figure 22.

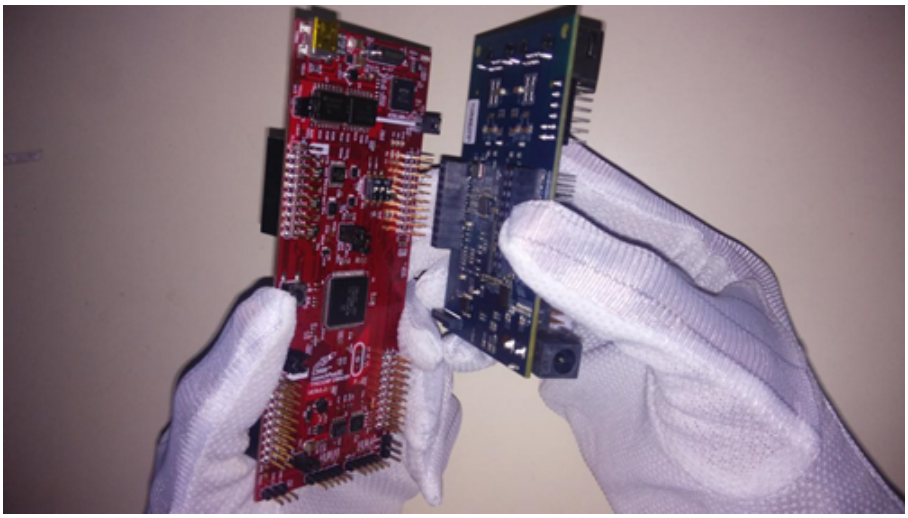

Figure 22. AMIC110 ICE and F28069M LaunchPad Connection (1 of 2)

2. Press the boards together gently to avoid PCB warping issues (see Figure 23).

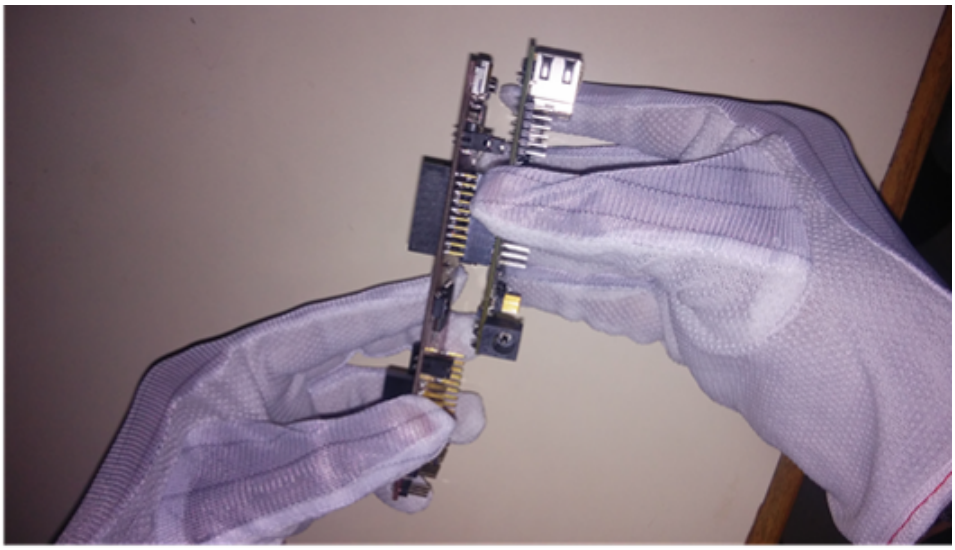

Figure 23. AMIC110 ICE and F28069M LaunchPad Connection (2 of 2)

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Figure 24 shows the connected AMIC110 ICE and F28069M LaunchPad boards.

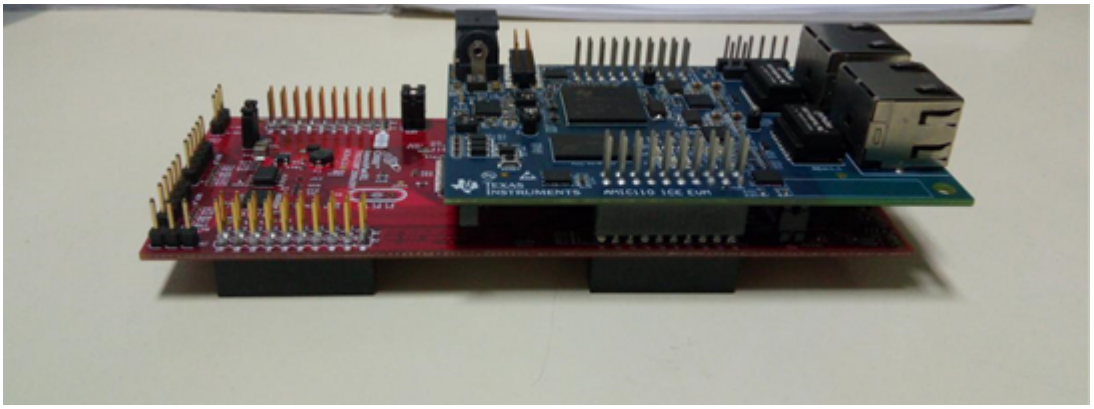

Figure 24. Connected Devices

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Date	Revision	Description
April 2017	*	Initial release

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